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This is to certify that **Aravinth. T. S, Sundar. R, Felix Muthu** have published a research paper entitled ***'Design of CMOS 8-Bit Parallel Adder Energy Efficient Structure using SR-CPL Logic Style '*** in the International Journal of Scientific Research in Science and Technology (IJSRST), Volume 3, Issue 5, May-June-2017.

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