

# Vedic Multiplier Using Efficient Compressor to Reduce Delay for Vedic Multiplier : A Review

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## ABSTRACT

With the coming of new innovation in the space of VLSI, correspondence and flag handling, there is a perpetually going interest for the rapid preparing and low territory design. The speed of a processor enormously relies on upon its time rather than a full snake and equipped for playing out this current multiplier's execution. This thusly builds the interest for fast multipliers, in the meantime remembering low territory and direct power utilization . In the course of recent decades, a few new structures of multipliers have been composed and investigated. Multipliers in view of the Booth's and changed Booth's calculation is very well known in present day VLSI configuration however joined their own arrangement of drawbacks. In these calculations, the increase procedure, includes a few middle of the road operation before touching base at the last answer.

**Keywords:** R High Speed Multiplier, 4:2 Compressors, 7:2 Compressor, Modified Architecture, Vedic Mathematics, Array Multiplier, FPGA.

## I. INTRODUCTION

In these multiplier calculations, the duplication procedure, includes a few transitional operations before gotten at the completing answer. The middle of the road stages incorporate a few increments, subtractions and correlations which lessen the speed exponentially with the aggregate number of bits present in the multiplier and the multiplicand. Since the speed is significant concern, using such kind of models is bad approach since it includes a few tedious operations. Vedic arithmetic calculation to get the consummation item. This thus signs to a rapid way to deal with accomplish augmentation. In this paper, investigate a novel strategy to further upgrade in speed of a Vedic multiplier by supplanting the current full adders and half adders of the Vedic science based multipliers with compressors based adders. A full viper and fit for acting with a lesser door include and higher speed correlation with an identical full snake circuit.

## II. VEDIC MATHEMATICS

### A. Urdhwa Tiryakbhyam Sutra for binary number system

Vedic arithmetic is separated into 16 unique sutras to perform to perform scientific estimations. Among these sutras Urdhwa Tiryakbhyam is the most ideal and adequate calculation to perform augmentation of whole numbers and in addition paired numbers. The expression "Urdhwa Tiryakbhyam" begun from 2 Sanskrit words Urdhwa and Tiryakbhyam which implies that "vertically" and "transversely" separately. Give us a chance to consider the two 8 bit numbers X7-X0 and Y7-Y0,

$$P_0 = A_0 * B_0 \quad (1)$$

$$C_1 P_1 = (A_1 * B_0) + (A_0 * B_1) \quad (2)$$

$$C_3 C_2 P_2 = (A_2 * B_0) + (A_0 * B_2) + (A_1 * B_1) + C_1 \quad (3)$$

$$C_5 C_4 P_3 = (A_3 * B_0) + (A_2 * B_1) + (A_1 * B_2) + (A_0 * B_3) + C_2 \quad (4)$$

$$C7C6P4=(A4*B0)+(A3*B1)+(A2*B2)+(A1*B3) \\ +(A0*B4)+C3+C4$$

(5)

$$C10C9C8P5=(A5*B0)+(A4*B1)+(A3*B2)+(A2*B3) \\ +(A1*B4)+(A0*B5)+C5+C6$$

(6)

$$C13C12C11P6=(A6*B0)+(A5*B1)+(A4*B2)+(A3*B3) \\ +(A2*B4)+(A1*B5)+(A0*B6)+C7+C8$$

(7)

$$C16C15C14P7=(A7*B0)+(A6*B1)+(A5*B2)+(A4*B3) \\ +(A2*B5)+(A1*B6)+(A0*B7)+C9+C11$$

(8)

$$C19C18C17P8=(A7*B1)+(A6*B)+(A5*B3)+(A4*B4) \\ + \\ (A3*B5)+(A2*B6)+(A1*B7)+C10+C12+ \quad C14$$

(9)

$$C22C21C20P9=(A7*B2)+(A*B3)+(A5*B4)+(A4*B5)+ \\ (A3*B6)+(A2*B7)+C13+C15+C17$$

(10)

$$C25C24C23P10=(A7*B3)+(A6*B4)+(A5*B5)+(A4*B6) \\ )+ \\ (A3*B7)+C16+C18+C20$$

(11)

$$C27C26P11=(A7*B4)+(A6*B5)+(A5*B6)+(A4*B7)+ \\ C19+C21 +C23$$

(12)

$$C29C28P12=(A7*B5)+(A5*B6)+(A5*B7)+C22+ C24+ \\ C26$$

(13)

$$C30P13=(A7*B6)+(A6*B7)+C25+C27+C28$$

(14)

$$P14=(A7*B7)+C29+C30$$

(15)

$$P15=(A7*B7)$$

(16)

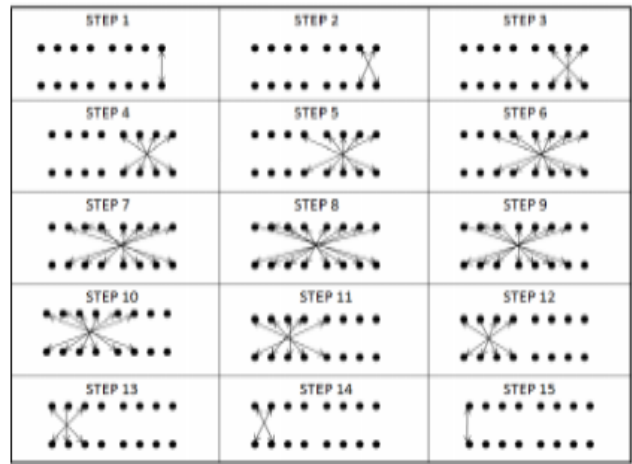


Figure 1. Line diagram for 8 bit Urdhwa multiplier

### B. Urdhwa Tiryakbhyam Sutra for decimal number system

Urdhva tiryakbhyam Sutra is a general duplication recipe appropriate to all instances of augmentation. It actually signifies "Vertically and Crosswise". To delineate this increase plot, let us consider the augmentation of two decimal numbers ( $5498 \times 2314$ ). The customary strategies definitely know to us will require 16 augmentations and 15 increases.

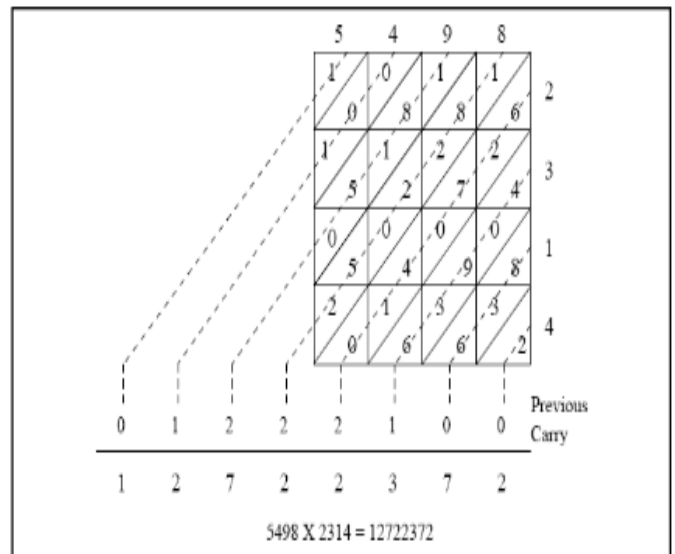


Figure 2. Alternative way of multiplication by Urdhva tiryakbhyam Sutra.

### C. Nikhilam Sutra

Nikhilam Sutra truly signifies "all from 9 and last from 10". In spite of the fact that it is appropriate to all instances of increase, it is more productive when the numbers included are vast. It discovers the compliment of the vast number from its closest base to play out the duplication operation on it, thus bigger the first number,

lesser the multifaceted nature of the increase. We initially show this Sutra by considering the augmentation of two decimal numbers ( $96 \times 93$ ) where the picked base is 100 which is closest to and more prominent than both these two numbers.

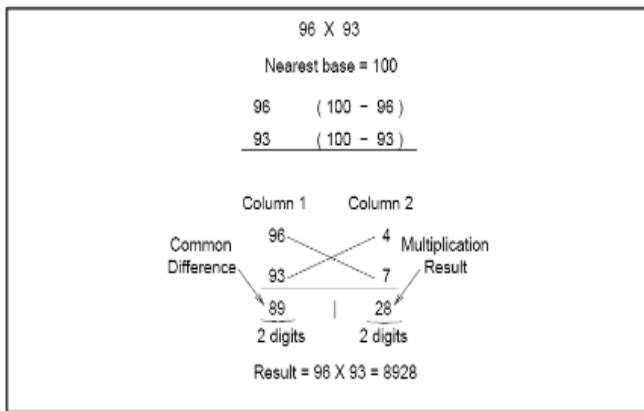


Figure 3. Line diagram for multiplication of two 4-bit numbers

### III. COMPRESSOR BASED ADDER

#### A. 3:2 compressor

The 3:2 compressors can add 3 inputs having a single bit and produces 2 bit output.

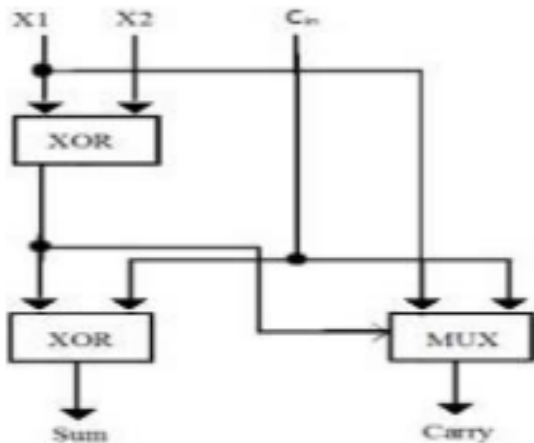


Figure 4. Gate level structure of 3:2 compressor.

#### B. 4:2 compressor

4:2 compressor can add 4 single bit inputs and one carry input bit, which intern produces 3 bit output

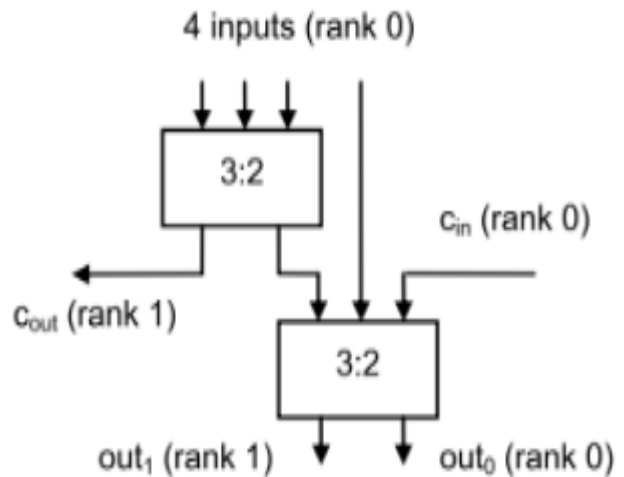


Figure 5. 4:2 compressor architecture by using 3:2 compressor.

#### C. 7:2 compressor

Similar to 4:2 compressors, the 7:2 compressors is having the capability of adding 7 single bit inputs and two carry inputs from previous stage at a time, which intern produces 4 bit output.

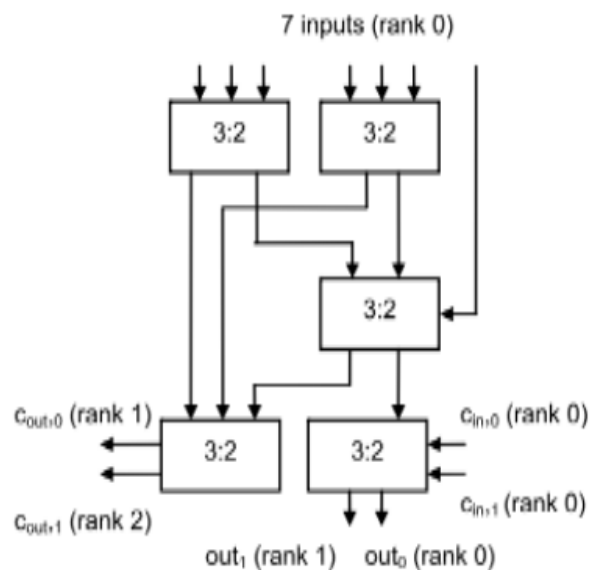


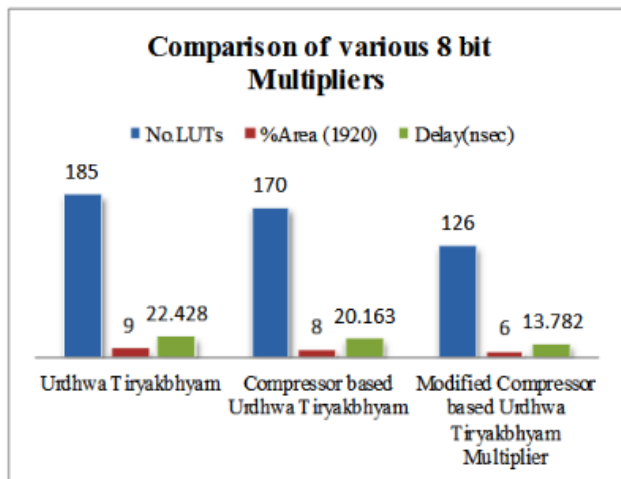
Figure 6. 7:2 compressor architecture by utilizing 3:2 compressors.

### IV. RESULT

To play out the examination in the middle of different multipliers, for example, Urdhwa multiplier, compressor based Urdhwa multiplier and changed compressor based Urdhwa multiplier were outlined and executed on a XILINX Spartan 3E-XC3S100E FPGA by utilizing

Verilog HDL. Endless supply of the region involved by the multiplier and furthermore its speed, with two other mainstream multipliers, we can presume that the compressor based Vedic maths multiplier ends up being a superior choice over regular multipliers utilized as a part of a few quick and complex VLSI circuits.

Graph I. Comparison Of Speed Area Occupied Of Various Multiplier Architectures



From the Graph I, it is observe that the speed the modified compressor based architecture performs well and is faster than that of existing Urdhwa multiplier and compressor based multipliers.

#### IV. CONCLUSION

This is a noteworthy change as for rapid multiplier design. Also, it can be seen that, a considerable lot of the stages have now been lessened to a negligible legitimate XOR operation, with an activity to decrease area. Hence from the vedic arithmetic, augmentation of two 8 bit numbers was created. At long last it is inferred that, the altered structure gives the better execution as far as speed and range. All these multiplier plans are planned utilizing Verilog HDL. Reenactment and union is done utilizing Xilinx 13.2 instrument for Spartan 3E arrangement FPGA.

#### VI. REFERENCES

[1] L. Sriraman, T.N. Prabakar, "Design and Implementation of Two Variable Multiplier Using KCM and Vedic Mathematics," 1st Int.Conf.on

Recent Advances in Information Technology, Dhanbad,India 2012,IEEE Proc., pp. 782-787.

[2] M. Ramalatha, K. Deena Dayalan, S. Deborah Priya, "High Speed Energy Efficient ALU Design using Multiplication Techniques," Advances in Computational Tools for Engineering Applications, 2009, IEEE Proc., pp 600-603.

[3] Tiwari, Honey Durga, et al., "Multiplier design based on ancient Indian Vedic Mathematics," Int. SoC Design Conf., 2008, vol. 2. IEEE Proc.,pp. II-65 - II-68.

[4] Sushma R. Huddar Sudhir Rao , Kalpana M and Surabhi Mohan,"Novel High Speed Vedic Mathematics Multiplier using Compressors" IEEE Conf.VLSI, pp.465-469, 2013.

[5] Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, "Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda," pp. 5-45, MotilalBanarasida Publishers, Delhi, 2009.

[6] HimanshuThapliyal and M. B. Srinivas, "An efficient method of ellipticcurve encryption using Ancient Indian Vedic Mathematics," 48th IEEE PInt. Midwest Symp. On Circuits and Systems, 2005, vol. 1, pp. 826-828.

[7] Hsiao, Shen-Fu, Ming-Roun Jiang, and Jia-Sien Yeh, "Design of high speed low-power 3-2 counter and 4-2 compressor for fast multipliers". IEEE Electronics Letters, vol. 34, no.4, pp. 341-343, Feb. 1998.