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Review on Design Approach for FPGA Implementation of 16-Bit Vedic Multiplier

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ABSTRACT

In this paper, a high speed and low power 16x16 Vedic Multiplier is designed by using low power and high speed modified carry select adder. Modified Carry Select Adder employs a newly incremented circuit in the intermediate stages of the Carry Select Adder (CSA) which is known to be the fastest adder among the conventional adder structures. A Novel technique for digit multiplication namely Vedic multiplication has been introduced which is quite different from normal multiplication by shift and addition operations. Normally a multiplier is a key block in almost all the processors and also introduces high delay block and also a major power dissipation source. This paper presents a new design methodology for less delay and less power efficient Vedic Multiplier based up on ancient Vedic Mathematic techniques. This paper presents a technique for N×N multiplication is implemented and gives very less delay for calculating multiplication results for 16×16 Vedic multiplier. In this paper, the main goal is to design the high speed and low power and area efficient Vedic multiplier based on the crosswise and vertical algorithm. Comparisons with existing conventional fast adder architectures have been made to prove its efficiency. The performance analysis shows that the proposed architecture achieves three fold advantages in terms of delay-area-power. The synthesis results of the Vedic multiplier has compared with the booth, array multiplier by different technologies. Booth multipliers are generally used for multiplication purposes. Booth Encoder, Wallace Tree, Binary Adders and Partial Product Generator are the main components used for Booth multiplier architecture. Booth multiplier is mainly used for 2 applications are to increase the speed by reduction of the partial products and also by the way that the partial products to be added. The Vedic mathematics mainly reduces the complex typical calculations in to simpler by applying sutras as stated above. These Vedic mathematic techniques are very efficient and take very less hardware to implement. These sutras are mainly used for multiplication of two decimal numbers and we extend these sutras for binary multiplications. Multiplexer is also called Universal element or Data Selector. A Multiplexer has of 2^n inputs have n select lines Basically MUX operation based on the select lines. Depending upon the select line the input is Send to the output. Multiplexers used to increase the amount of data that can be sent over the network. The values of 4 bit can be taken and remaining can be obtained from the next blocks. Like that we will obtain totally sixteen outputs and those are outputs of the sixteen bit addition.

Keywords: Vedic Mathematics, FPGA, Vedic Multiplier, MAC Unit

I. INTRODUCTION

Multiplication is one of the fundamental block in almost all the arithmetic logic units. This Vedic multiplication is mainly used in the fields of the Digital Signal Processing (DSP) and also in so many applications like Fast Fourier Transform, convolution, filtering and microprocessor applications. In most of the DSP algorithms multiplier is one of the key component and hence a high speed and area efficient multiplier is needed and multiplication time is also one of the predominant factor for DSP algorithms. The ancient mathematical techniques like Vedic mathematics used to reduce the computational time such that it can increases speed and also requires less hardware. There are sixteen sutras and sixteen sutras (sub formulae) constructed by

swahiji. Vedic is a word obtained from the word “Veda” and its meaning is “store house of all knowledge”. Vedic mathematics mainly consists of the 16 sutras which it can be related to the different branches of mathematics like algebra, arithmetic geometry. The Vedic mathematics mainly reduces the complex typical calculations in to simpler by applying sutras as stated above. These Vedic mathematic techniques are very efficient and take very less hardware to implement. These sutras are mainly used for multiplication of two decimal numbers and we extend these sutras for binary multiplications. Booth multipliers are generally used for multiplication purposes. Booth Encoder, Wallace Tree, Binary Adders and Partial Product Generator are the main components used for Booth multiplier architecture. Booth multiplier is mainly used for 2 applications are to increase the speed by reduction of the partial products and also by the way that the partial products to be added. Vedic multiplication technique called “Urdhva-Tiryakbhyam – Vertically and crosswise.” Which can be used not only for decimal multiplication but also used for binary multiplication? This technique mainly consists of generation of partial products parallel and then we have to perform the addition operation simultaneously. This algorithm can be used for 2x2, 4x4, 8x8....N×N bit multiplications. Since the sums and their partial products are calculated in parallel the Vedic multiplier does not depends upon the processor clock frequency. Hence there is no need of increasing the clock frequency and if the clock frequency increases it will automatically leads to the increase in the power dissipation. Hence by using this Vedic multiplier technique we can reduces the power dissipation. The main advantage of this Vedic multiplier is that it can reduces delay as well as area when compared with the other multipliers. Ripple Carry Adder: Ripple carry adder is designed using multiple full adders to add 8-bit numbers. Each full adder inputs a Cin, which is the Cout of the previous adder. The adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. The layout of a ripple-carry adder is simple, which allows for fast design time; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. Ripple adder is a combination of 4full adders in which output carry is used as input carry to the next full adder. RCA uses large number of AND, OR, NOT gates. It has the advantages of high speed and less delay. Binary to Excess-1 Code Converter: In Binary to Excess one converter we are using XOR, AND, NOT gates by implementing these gates we are reducing the area, time delay, power consumption because of reduction in number of gates when compared to normal ripple carry adder. The 4 Bit Binary to Excess-1 Code Converter is shown in figure 5. The addition is achieved. Using BEC together with a multiplexer (mux) one.

II. LITERATURE SURVEY

In this analytical study of subject it is required to search different existing cases and the available study material regarding that subject. In order to collect the necessary and valuable information, the literature survey is done. So the study of topic and the related literature published in different journals and papers are as follows.

[1] In the paper, multiplication is one of the main functions in a digital signal processing. The performance of the DSP system depends on the performance of the multiplier. Hence it is very important to develop an efficient and fast design to implement multiplier. Vedic mathematics can be used to transform tedious calculations into simpler and orally manageable operation. Vedic multiplication uses Urdhva Triyambakam multiplication algorithm. The vedic multiplication algorithm generates partial products in parallel. In this work, we prapose using Han-carison adder to improve the performance of vedic multiplier. We compare the performance of the proposed design with vedic multiplier that uses kogge-stone adder. A 24-bit vedic multiplier is implemented, which can be used for mantissa multiplication in single-precision floating-point multiplier. The proposed multiplier is coded in Verilog HDL.Xilinx ISE 8.2i ued to simulate and synthesis the design.

[2] In this paper, we propose a novel architecture to perform high speed Multiplier by using Kogge Stone Adders with Mux and Vedic Multiplication. The Adder employed in implementing the paper is Kogge Stone Adder by using MUX which is a parallel prefix form of Carry Look Ahead Adder & widely used adder in the industries of the present day. One of the most efficient sutra in vedic mathematics named as Urdhva Triyakbhyam strikes a difference in the actual multiplication process. Since the adder used generates the carry signal in O(logn) time, it is widely considered

to be the fastest adder design possible. Proposing Kogge Stone Adder by using MUX provides less components, less path delay and better speed compare to other existing Kogge Stone Adder and other Adders. In this research, we have implemented KSA with Mux and Vedic Multiplication. This work estimates the performance of proposed design in terms of Logic and route delay. The experimental results show that the performance of KSA with MUX and Vedic Multiplication is faster compared to other Adders. The proposed algorithm is developed using verilog HDL. Implementation has been done using Xilinx14.2, Spartan 6.

[3] This paper discusses about the implementation of Vedic multiplier in digital hardware. As the multiplier block has adder as the basic component, various generic adder architecture are considered for the implementation the combinational delay for various adder architecture is found. In this paper a 4×4, 8×8, and 16×16, bit multiplier circuit is designed with hierarchical structuring, it has been optimized using Vedic Multiplication "Urdhva Triyagbhyam" Sutra (Algorithm).Algorithm is implemented with Spartan xc2s200-5-pq208 device, Virtex2 Xc2V250FG256-5 device, Virtex5 Xc5VLX220-2ff1760 device, FPGA (Field Programmable Gate Array). The proposed multiplier implementation with Kogge-Stone Adder as a basic component yields a significant reduction in Combinational path delay. The combinatational path delay of the various Vedic multipliers is found with various adder architecture it is concluded that the Kogge-stone adder when used as the component while multiplication the combinatational paths delay reduces. In this work, some steps have been taken towards implementationof fast and efficient Arithmetic Logic Unit or a Math Co-processor, using Vedic Mathematics.

[4] In this paper, This paper aims at incorporating residue adder in the design of multiplier based on Nikhilam Sutra of Vedic mathematics. The residue adder employs residue number system (RNS). The performance is the proposition is compared with a Vedic multiplier employing carry save adder. The multiplier is coded in Very High Speed Integrated Circuits (VHSIC) Hardware Description Language (VHDL) while the simulation and synthesis is done using the Xilinx ISE Design Suite 14.2 software. An efficient Vedic multiplier based on Nikhilam sutra of Vedic mathematics and residue number system based residue adder is proposed. The functionality is verified through VHDL simulations and synthesis on Xilinx Spartan platform. The simulation results show that the proposed RNS based vedic multiplier has significant speed improvement over CSA based realization. The 8-bit multiplier presented here can easily be extended to 16 bits.

[5] In the paper, Multiplication is an operation much needed in Digital Signal Processing for various applications. This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryagbhyam, a sutra from Vedic Math for multiplication and Kogge Stone algorithm for performing addition of partial products and also compares it with the characteristics of existing algorithms. The below two algorithms aids to parallel generation of partial products and faster carry generation respectively, leading to better performance. The code is written in Verilog HDL and implemented on Xilinx Spartan 3 and Spartan 6 FPGA kit using Xilinx ISE 9.1i. The propagation delay of the implemented architecture is obtained to be 28.699ns and 15.752ns respectively. The proposed technique of multiplication using UrdhvaTiragbyam algorithm and Kogge Stone algorithm causes less latency when compared to available techniques in literature. The proposed technique when implemented for 8x8 bit multiplication, the delay is found to be 28.699ns on SPARTAN 3 and 15.752 ns on SPARTAN 6. The adoption of KSA algorithm for higher bit size multipliers will further show improvement in speed[9]. Further, higher speeds can be achieved by making use of pipelining and parallel processing techniques. This work will increase awareness of Vedic mathematics techniques in the field of engineering and delivers high performance in DSP Processors.

[6] In this paper, describes the implementation of an 8-bit Vedic multiplier using fast adder enhanced in terms of propagation delay when compared with conventional multiplier. In our design of 8 bit Vedic multiplier using fast adder, we have utilized 8-bit barrel shifter which requires only one clock cycle for 'n' number of shifts. The design of 8 bit Vedic multiplier using barrel shifter is implemented and verified using FPGA and ISE Simulator. The core used here was implemented on

Altera Cyclone® II 2C20 FPGA device software. The propagation delay between 8 bit Vedic multiplier using barrel shifter using barrel shifter and using fast adder comparison was extracted from the synthesis report and static timing report as well. The design which is implemented here could achieve propagation delay of 6.781ns using barrel shifter block in base selection module and multiplier of architecture used. In our project, we make a comparison between performance analysis of 8 bit Vedic multiplier using barrel shifter and using fast adder. The high speed implementation of such a multiplier has wide range of applications in image processing, arithmetic logic unit and VLSI signal processing The future scope of this particular work can be extended in design of ALU‟s in RISC processor.

III. PROBLEMS DEFINITIONS

Power consumption has always been an issue with digital circuits, and lower the consumption, the better is the circuit. Our motivation comes from this point, and we research to reduce the power consumption of the adder used in Vedic multipliers by developing a hybrid low power design.

A high speed and low power 16x16 Vedic Multiplier is designed by using low power and high speed modified carry select adder. Modified Carry Select Adder employs a newly incremented circuit in the intermediate stages of the Carry Select Adder (CSA) which is known to be the fastest adder among the conventional adder structures. A Novel technique for digit multiplication namely Vedic multiplication has been introduced which is quite different from normal multiplication by shift and addition operations. Normally a multiplier is a key block in almost all the processors and also introduces high delay block and also a major power dissipation source. This paper presents a new design methodology for less delay and less power efficient Vedic Multiplier based up on ancient Vedic Mathematic techniques. This paper presents a technique for N×N multiplication is implemented and gives very less delay for calculating multiplication results for 16×16 Vedic multiplier. In this paper, the main goal is to design the high speed and low power and area efficient Vedic multiplier based on the crosswise and vertical algorithm. Comparisons with existing conventional fast adder architectures have been made to prove its efficiency. The performance analysis shows that the proposed architecture achieves three fold advantages in terms of delayarea-power. The synthesis results of the Vedic multiplier has compared with the booth, array multiplier by different technologies. The problem with the existing circuit is that it is not completely optimized for power, we would be designing a circuit with lower power. I will try to endeavour a solution to these problems.

IV. CONCLUSION

There will be development of simple Ripple Carry adder then of carry save adder. Development of Vedic multiplier with the carry save adder. Improvement in the carry saves adder to reduce power .Using the new adder with the Vedic multiplier to get reduced power.

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