Review of CMOS based XOR/XNORs using Systematic Cell Design Methodology

Ashok Yadav*[1], Dr. Manish Jain[2]
*[1]Department of Electronics and Communication, RKDF Institute of Science & Technology, Bhopal, India
yadavashok101@gmail.com[1]
[2]Department of Electronics and Communication, RKDF Institute of Science & Technology, Bhopal, India
manish_jain18@rediffmail.com

ABSTRACT

The XOR and XNOR gates are the essential blocks of various digital arithmetic and logical units such as digital adder, digital parity generator/checker, digital comparator, and digital encryption processor. Many circuit topologies have been proposed till now of full adder and XOR/XNOR gate design that can be categorised in two categories. First one offers full swing output and second one offers partial swing output. The Systematic Cell Design Methodology is partial swing based logic design method which offers less delay and low power consumption at weak logic '0' and logic '1' generation at output. This paper concludes a partial swing and pass transistor based XOR/XNOR gate which gives less propagation delay and low power dissipation at a cost of poor driving capability as compared to existing full adder. In this work results are simulated at 1.2Volt and 130nm technology.
Keyword: Hybrid CMOS logic; XOR/XNOR gate; partial swing logic; full swing logic.

I. INTRODUCTION

In digital integrated circuits as the technology is getting advanced and innovative day by day, power consumption and delay is also increasing dramatically; saving power is high in demand as it will reduce the overall cost for mobile computing and higher integration density as well as reduction in delay offers higher computation speed. But poor voltage swing offered at output of logic block misguides or malfunction the next stage.

With the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, longer battery life, higher speed, and enhanced reliability is increases with technology scaling. As Technology scaling increases the transistor count and operating frequency, which push the market demand for more and more function in Integrated circuit. However scaling always increases leakage power dissipation. As channel length reduces which results in increase of power dissipation with respect to technology progresses. To reduce the power consumption different logic design techniques like CMOS complementary logic, Dynamic

CMOS, Pseudo NMOS, Dynamic CMOS, CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed [1-3]. Power dissipation depend on device structure property like gate oxide thickness, channel length, doping profile etc. as they are due to different physical phenomena Although Static CMOS Logic has been the most popular design approach for the past three decades [4, 5]. By scaling down the feature size of MOSFET devices in nano-meter, the supply voltage should be scaled down to avoid hot- carrier effects in CMOS circuits. To enhance the speed of the CMOS circuits, threshold voltage of the circuits has to be scaled down.

The dynamic XOR/XNOR logic gate is one of the most primary building blocks of arithmetic and logic unit (ALU) used in microprocessor. This plays an important role in silicon on chips (SoCs) to design ALU in small die area that reduce manufacturing cost. This system inbuilt ALU occupy more area on silicon chip that dissipate more heat and elevate the temperature of chip. This thing degrades the performance of system. In order to save the chip heat sink is needed that release the internal heat to external environment. As the operating

frequency of dynamic XOR improves, dynamic power consumption becomes dominant that introduce heating problem as mentioned above. To overcome this problem, dynamic XOR gate proposed with minimum delay and smaller power consumption.

II. PUBLISHED LITERATURE

The recently published novel work can be divided into two categories as they are extracted from the topic: 1) traditional three input XOR gate and 2) its operating methodologies. Cell design methodology (CDM) has been presented to design some limited functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style [5-7]. The predominant results persuade us to improve Cell Design Methodology (CDM) through two stages: 1) generating more complex functions and 2) rectifying some remaining flaws. The flaws in previously published CDM include containing some manual steps in the design flow and generating a large number of designs in which the predominant ones would be determined after the completion of simulations. Therefore, in the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits have been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power ground- free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability. The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches [8]. Power-ground-free main structure leads to power reduction.

The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low VDD operations and low static power dissipation. The methodology has high flexibility in target and systematically considers it in the three design steps. This can lead to efficient circuits in terms of performance, power, power delay product, energy delay product, layout area.

The fast evolution of microelectronics fabrication processes demands a new cell library generation or a library technology migration. The well-organized systematic methodology leads to automated flow, which can reduce design time and costs, provide consistency in the cell library generation process, increase the range of simulation capabilities at the characteristics step, as well as minimize the risk of errors [6, 9]. Recently published article on hybrid type systematic cell design methodology (SCDM) applied on three circuits as shown in Figure1, Figure2 and Figure3. The Three input XOR/XNOR based transmission gate using 16 transistors (TG16T)[10] shown in Figure1. Another three input XOR/XNOR based transmission gate and mirror circuit using 16 transistors (TGM16T)[10] shown in Figure2. next is three input XOR/XNOR based transmission gate and mirror circuit using 18 transistors (TGM18T)[10] shown in Figure3. All three circuit have

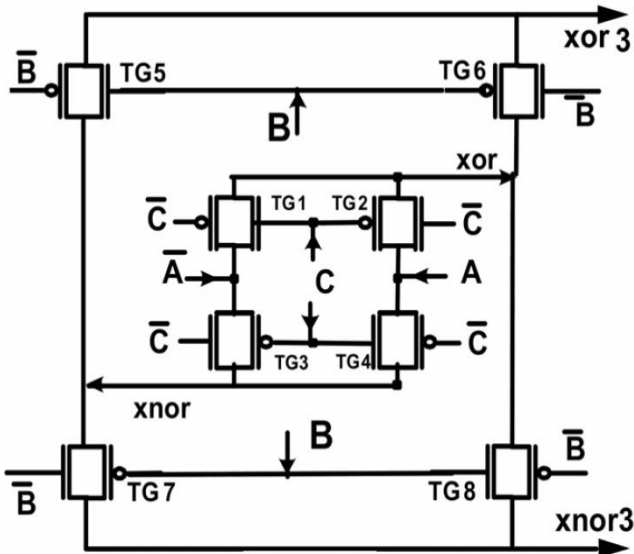six inputs (A, B, C and compliment of all three inputs) and two outputs (XOR and its compliment).

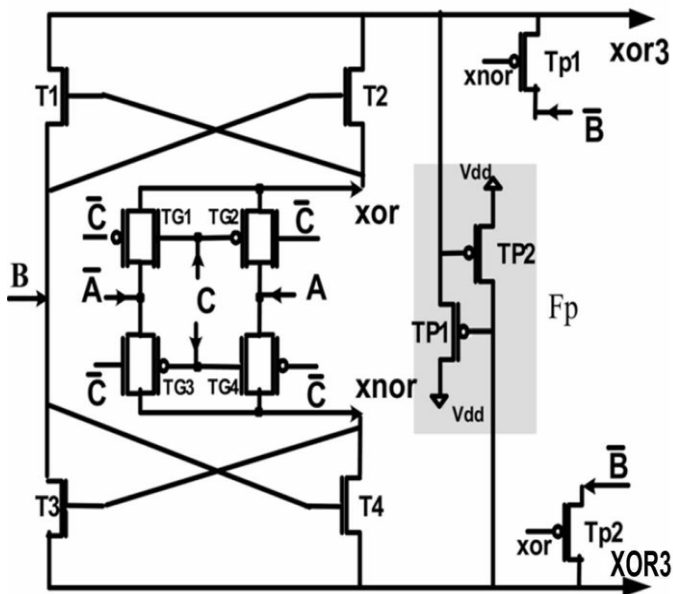**Figure 1** Three input XOR/XNOR using transmission gate(TG16T)[10]

Figure 2 Three input XOR/XNOR using transmission gate and mirror circuit (TGM16T)[10]
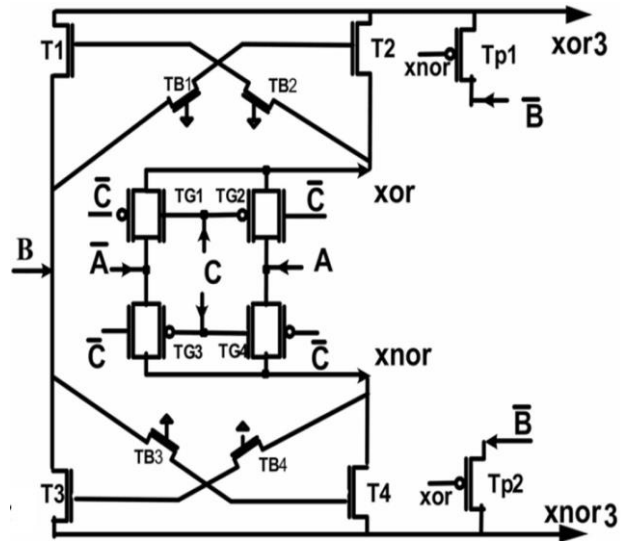

Figure 3 Three input XOR/XNOR using transmission gate and mirror circuit (TGM18T)[10]

III. RESULT ANALYSIS AND COMPARISON

To review the performance of three input XOR/XNOR gate, it is necessary to study the transient analysis and process variation. This comparison have been performed complete study using Hspice [11]. To investigate further several modules with complementary outputs of full adders (FAs), TFA, Hernandez1, Hernandez2, NEWHPSC, Hybrid, 18T_new_FS, and LPHS-FA have been analysed, whose excellence have been confirmed in [12] [13] and [14-16]. Therefore, an approximately fair comparison will take place by selecting them. Table-1 shows that TG16T[10], TGM16T[10] and TGM18T[10] technique have least PDP and delay than other existing conventional LPHS-FA and TF technique.
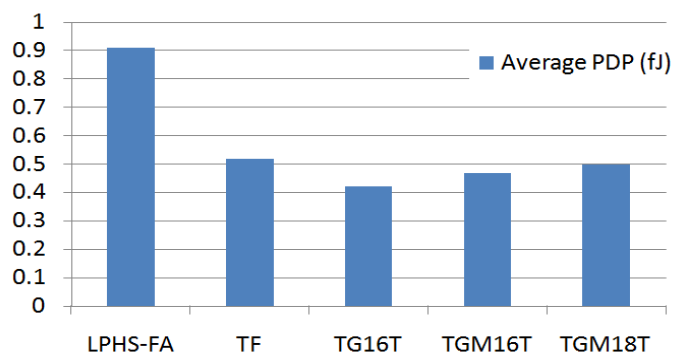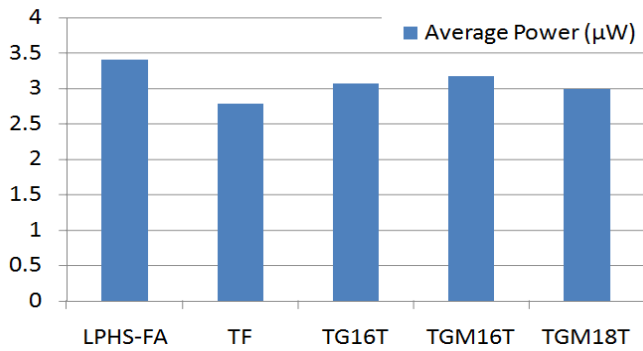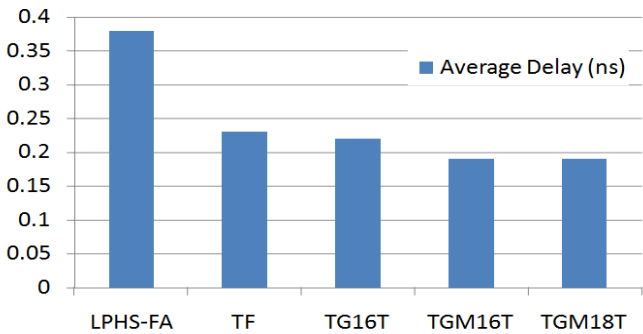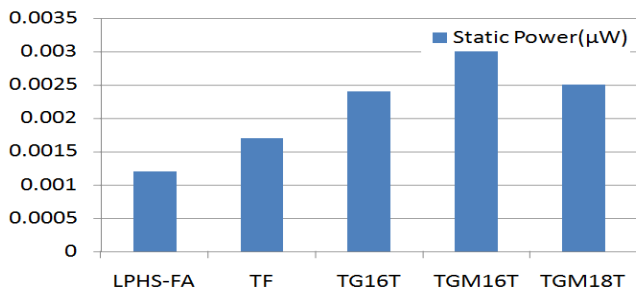

Figure 4. Comparison of average PDP (fJ) at 130nm technology

Figure 5. Comparison of average power (μW) at 130nm technology

Figure 6. Comparison of average delay (ns) at 130nm technology

Figure 7. Comparison of static power (μW) at 130nm technology

The comparison of Average PDP (fJ), Average Power (μW), Average Delay (ns) and Static Power (μW) are shown in Figure 4, Figure 5, Figure 6 and Figure 7 respectively. The layout area occupied by existing XOR/XNOR cells is shown in Table-1.

Table-1: Comparison of layout area at 130nm technology

Circuits	Area(μm²)
LPHS-FA	NA (too large)
TF	0.15
XRG1	0.13
XRG2	0.16
XRG3	0.13

IV. CONCLUSION

Logic gate XOR/XNOR gates are frequently used in high performance data processing units. Logic gate with high speed gates, low power static power and low dynamic power are most demanded in modern integrated circuit. In recently published work TG16T, TGM16T and TGM18T offers smaller delay and low dynamic power consumption due to reduction no. of switching node but offers higher static power consumption due to transmission technology as compared to existing technique LPHS-FA and TG. We will improve this fault in future research work.

V. REFERENCES

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