

Asymmetrical Multilevel Inverter for Electric Vehicles Application with Chopper Control

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ABSTRACT

This paper deals with cascade multilevel inverters. It focuses on asymmetrical topologies where the cell input voltages are of different values. These hybrid topologies might be used in several applications. The main advantage of asymmetrical multilevel inverters is the optimization of levels with a minimum number of power supplies. However, this optimized multilevel system still needs a large number of isolated and floating dc supplies, which makes these converters complicated to implement in Electric Vehicles (EVs), because the system will require many independent battery packs. In this work, a very simple scheme, based on a small and cheap High Frequency Link (HFL), allows the utilization of only one power supply for the complete multilevel inverter drive, with an inherent regulation of the voltages supplied among the H-bridges. It also allows voltage control with the full number of levels if the dc source is of a variable voltage characteristic. This is focused on a 27-level asymmetric inverter, but the strategy, using only one power supply, which can be applied to converters with any number of levels. In particular, an asymmetrical 27-level converter needs nine isolated power supplies, and the system reduces these nine sources to only one (the battery car). A new scheme of Multi Carrier Pulse Width Modulation (MCPWM) method for the control of a three-level inverter is proposed. Multi Carrier Pulse Width Modulation (MCPWM) works with a constant carrier frequency not synchronized with fundamental stator frequency. MCPWM gives an optimal utilization of switching frequency permitted, therefore PWM carrier frequency may be chosen to a value of two times the permitted switching frequency. The topology also permits full regenerative braking working as a three-level converter. The system is intended for application in EVs from power ratings up to 150 kW.

Keywords : AC motor drives, electric vehicles (EVs), hybrid EVs (HEVs), multilevel converters, power conversion.

I. INTRODUCTION

Multilevel inverter Since switching frequency is restricted by switching losses in high power and high voltage applications, multilevel inverters have found wide acceptance as they can achieve a low harmonic component with low switching frequency. Furthermore, low blocking voltage by switching devices is the other advantage of this type of converters as well as minimum harmonic distortion and switching losses. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. There are several ways to build multilevel inverters. The main topologies are the neutral point clamped inverters [1], the flying capacitors inverters [2] and the cascade inverters [3]. This paper investigates the latter inverters and focuses on

topologies where the input voltage values are different [4]. These topologies are known as asymmetrical or hybrid multilevel inverters, they may be divided in three categories by ascending order of hybridization: several inverters are series connected, all with the same topology but at least one with a different input voltage [5], [6], [7], several inverters are series connected, with different topologies and different input voltages [8], [9], [10], [11], several converters of different nature, with different topologies and input voltages are series connected.

B. Asymmetrical multilevel inverter basic principles

The cascade multilevel inverter consists of a set of series connected cells. An asymmetrical multilevel inverter is defined by its topology, i.e. the set of combined cells, and by the configuration of their input voltages. One

important feature is that the cells have to be insulated one from each other, this constitutes the major drawback of these structures. Four-switch H-bridge voltage source inverters might be chosen for the cells and they can be supplied by bidirectional DC-DC converter.

Possible benefits of the hybridation: Due to the different input voltages of the cells, high-voltage switches presenting low relative conduction losses are combined with low-voltage switches having low commutation time. Naturally, for most operating points, the switching frequency of low voltage cells is higher. Together with the switch characteristics, one can take advantage of this specificity. For applications which need a low switching frequency, the conduction losses are predominant and the hybrid inverter has higher losses than a conventional inverter, but above a given frequency it would theoretically allow lower losses. From the voltage resolution point of view, with the same number of cells, the asymmetrical multilevel inverter allows a higher resolution than symmetrical multilevel inverters. In the symmetrical case, the number of levels grows proportionally to the number of cells, in the asymmetrical case, it grows exponentially.

Supply issue: The main drawback of the cascade inverter is the need of insulated supplies. It increases the converter complexity (and cost) and reduces the energetic efficiency. For some asymmetrical configurations, some levels can only be generated by summing contributions of opposite signs. When generating such levels, the power is flowing from the DC supply to the load for some cells and from the load to the DC supply for the others. As a consequence, for many operating points, in addition to the effective load power, there is a circulation of power between the cells which increases dramatically the inverter losses. The benefit of the hybridation is wasted by these additional losses. Furthermore, the average circulation of power doesn't naturally cancel over a whole period. For some configuration and/or applications, it can be balanced. If it cannot, the supply must be bidirectional even if the load isn't. In [9] a solution to the supply issue has been presented. The low-voltage cells supplied are saved and the converter energetic efficiency is improved.

Simultaneous commutation issue: For some configurations and for some operating points (the same

as for the supply issue) there are many simultaneous commutations which increase the switching losses. By following adequate design rules and control strategy, this problem can be avoided [10]. So far, the configurations with the highest voltage-resolution were not considered as suitable to get a PWM output. Our goal is to get a bidirectional converter with high voltage resolution and high energetic-efficiency. For that purpose, we work on the optimization of the converter structure and on the cell association rules.

II. THE PROPOSED SYSTEM AND OPERATION

Today, cascade multilevel converters have become very popular, because they are able to generate voltage waveforms with negligible distortion when compared with conventional inverters based on two- or three-level topologies [12]– [13]. One step ahead was the asymmetrical multilevel converter, which allows the generation of many more levels of voltage with a minimum number of power supplies [14]–[15]. The increase in the number of voltage levels reduces the total harmonic distortion (THD), the common-mode voltages, the output filters, and the switching losses (the main bridges, which carry 80% of the total power, work at a very low frequency in asymmetrical cascaded multilevel inverters) [16], [17]. Despite this important improvement, these topologies have an important drawback: They need many independent power supplies that must be floating, isolated, and balanced. In addition, in some particular levels of voltage, bidirectional power Supplies are required, and the same happens when regenerative Braking needs to be applied. Another drawback is the direct relation between the number of levels and the voltage amplitude, which produce a loss of quality when the output voltage is reduced. For this reason, costly and complex topologies have to be implemented to get the nine isolated supplies [18], [19]. In applications with constant frequency operation, such as power rectifiers, active power filters, or flexible ac transmission systems, output power transformers are used to connect the load, allowing operation with only one dc supply [20]–[21]. However, this solution is not applicable in electric vehicles (EVs) because all H-bridges must be connected in parallel at the same dc supply, and the isolation and voltage scaling problems are solved with multi winding transformers: one winding for each auxiliary (Aux) bridge. Moreover, this solution

introduces heavy, bulky, and complicated transformers and does not work when a variable frequency is required, as is the case with EV or hybrid EVs (HEVs). An improvement for drive applications has permitted reducing the number of power supplies using floating capacitors, unidirectional power sources, and a special pulse width modulation (PWM) strategy, called still makes multilevel inverters a complicated solution, because the independent battery packs are only partially reduced (in the case of a 27-level inverters, the nine supplies are reduced to only four). Other solutions using cascaded multilevel inverters with a single power source and without transformers have been introduced recently [14]–[16]. However, these solutions use floating capacitors with complex balancing systems and many more semiconductors in relation to the number of levels produced. The objective of this paper is to develop a new dc-link topology for an asymmetrical multilevel inverter, based on a simple high-frequency link (HFL), which allows using only one power supply (battery pack, fuel cell, or others). This single dc-supply system is particularly suitable for EVs but can also be used for HEVs and industrial machine drives. The system has an inherent regulation of the voltages supplied among the H-bridges; thus, the full number of levels can be produced at any amplitude of voltage, depending only on the single dc-supply regulation, which can be controlled with a chopper. This proposed topology does not need floating capacitors or heavy-bulky transformers. The topology also allows full regenerative operation when the power supply accepts power reversal (batteries or active front-end rectifiers).

For Traction drives, only one dc supply will be required for the complete system. Each of the three phases of the traction motor (induction, permanent-magnet synchronous motor, or brushless dc machine) is separately connected, as shown in Fig.1 with this solution; the three MAIN bridges can be connected in parallel to just one dc supply. This solution perfectly matches the requirement for traction applications: only one power supply (just one battery pack). To keep the full number of levels for all output voltage amplitudes, a dc voltage controller (chopper) is included in the topology. However, the system also works without the chopper using direct modulation on the H-bridges, but in this case, the NLC (Nearest Level Control) produces a reduction of levels and, consequently, a bad THD (Total Harmonic Distortion). Another solution to avoid the

chopper, and keeping a good THD, is changing the PWM on the H-bridges, but due to the great increase of the switching frequency, the efficiency of the converter will diminish. All the auxiliary converters (six in total) are fed from the proposed High Frequency Link (HFL). The High Frequency Link (HFL) consists of a simple square-wave generator, implemented with an H-bridge working at a high frequency (10–100 kHz) and a small ferrite transformer to isolate the outputs of each auxiliary converter. The high-frequency operation is quite important because it allows an important reduction in size and weight of components, mainly the ferrite transformer. This square-wave H-bridge is fed from the adjustable dc source and the voltage generated is connected to the primary of the transformer, which has many secondary windings. In the case of the 27-level inverter, the transformer has six of these secondary windings: three of them with turn ratios 9:3 and three with ratios 9:1. Then, six square-wave voltages with reduced amplitude are generated. Each of these high-frequency voltages is rectified using simple diode bridges. The advantage of using diode rectifiers is that they do not need to be controlled. They will also keep the relation 9:3:1 at the corresponding dc-link voltages, avoiding additional voltage distortion when the adjustable dc source is modified.

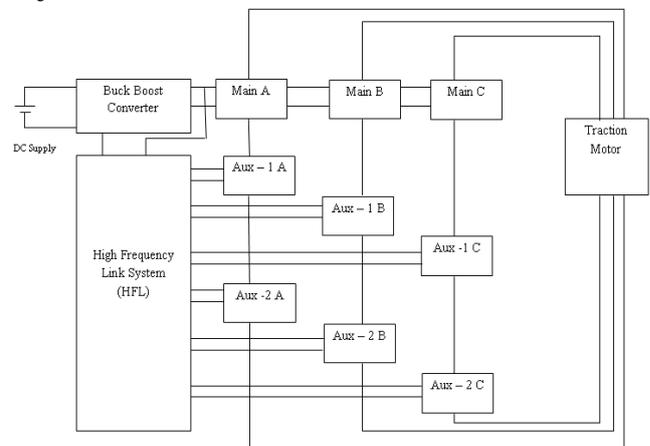


Figure 1. Proposed topology using only one power supply

The HFL feeds the auxiliary converters, as can be seen, the circuit is quite simple, because it only needs a high-frequency H-bridge rated at 20% full drive power, one multi winding ferrite transformer, and some bridge rectifiers made with simple fast recovery diodes. The H-bridge only needs to generate a square voltage waveform, and hence, no control is required for its operation. Transformer and some bridge rectifiers made with simple fast recovery diodes. The H-bridge only

needs to generate a square voltage waveform, and hence, no control is required for its operation. The number of turns of secondary and tertiary windings is scaled in power of 3 with respect to the dc-link voltage of the MAIN converters. These windings generate square waves that are rectified to feed each of the Aux bridges independently, keeping them isolated. This way, all H-bridges are fed from the adjustable dc supply, and the output voltage is modified by changing the voltage of this dc supply. When the dc supply is constant and then cannot be adjusted, the output voltage must be controlled by changing the switching pattern on the transistors of the H-bridges. In this case, at some particular levels of voltage, the power at some of the auxiliary bridges can become negative. As the low-power rectifiers connected at the auxiliary bridges are unidirectional, their dc capacitors will need to absorb small amounts of energy coming from the motor during those periods. For example, at 55% output power, the auxillary-1 bridge has 15% negative power, as shown in Fig.2. If this amount of energy is too large, the capacitor voltage can increase to undesired voltages, and in this case, a special MCPWM strategy, based on jumping those negative levels, is applied. This operation is only necessary when the dc supply cannot be adjusted. The HFL allows the reduction of floating dc supplies from three per phase to only one per phase. The “one per phase” reduction means three isolated sources for the complete system. However, with a small change in the wiring connection of the traction motor, only one dc supply will be required for the complete system. Each of the three phases of the traction motor (induction motor, permanent-magnet synchronous motor, or brushless dc machine). voltage level $5V_{dc}$, when T1, T2 switches in main bridge and T3, T4 switches in Aux-1and Aux-2 bridges are turned ON. The switching pattern for other levels is obtained accordingly. The switching pattern for negative sequences main, Aux-1, Aux-2 bridges are same as that of positive sequences

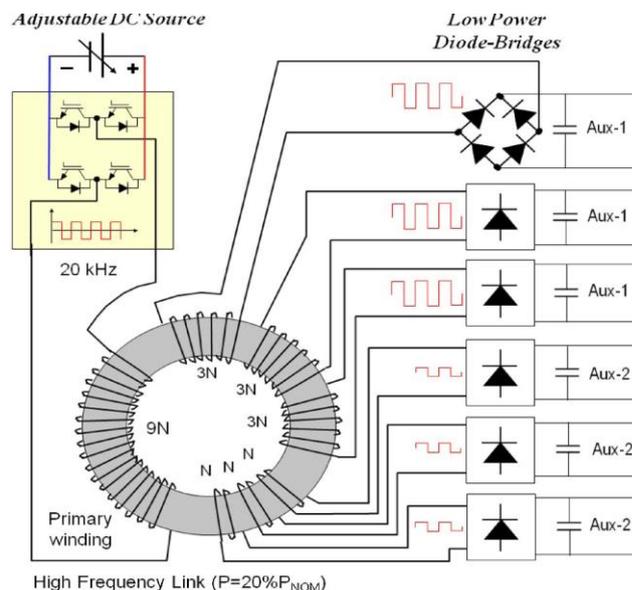


Figure 2. High Frequency Link

TABLE-I. SWITCHING STATES OF MLI (TRINARY LOGIC)

Main Bridge				Aux-1 Bridge				Aux-2 Bridge				Level
T1	T2	T3	T4	T1	T2	T3	T4	T1	T2	T3	T4	
1	0	1	0	1	0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0	0	0	1	1	2
1	0	1	0	1	1	0	0	1	0	1	0	3
1	0	1	0	1	1	0	0	1	1	0	0	4
1	1	0	0	0	0	1	1	0	0	1	1	5
1	1	0	0	0	0	1	1	1	0	1	0	6
1	1	0	0	0	0	1	1	1	1	0	0	7
1	1	0	0	1	0	1	0	0	0	1	1	8
1	1	0	0	1	0	1	0	1	0	1	0	9
1	1	0	0	1	0	1	0	1	1	0	0	10
1	1	0	0	1	1	0	0	0	0	1	1	11
1	1	0	0	1	1	0	0	1	0	1	0	12
1	1	0	0	1	1	0	0	1	1	0	0	13

The outputs voltage levels of the three rectifier bridges are in the ratio 9:3:1. The switching pattern for positive sequences of main, Aux-1, Aux-2 bridges up to 13 levels are shown in Table.1. For the voltage level of $1V_{dc}$, switches T1, T3 in main and auxillary-1 bridges and T1, T2 switches in auxillary-2 bridge are turned ON. For instance voltage level $2V_{dc}$, when switches T3, T4 in AUX-2 and T1, T2 switches in AUX-1bridges, and T1, T3 switches in main bridge are turned ON. For instance the voltage level $3V_{dc}$, when T1, T3 switches in Aux-2 and Main Bridge, T1, T2 switches in Aux-1bridge is turned ON. For instance the voltage level $4V_{dc}$, when T1,

T2 Switches in Aux-1 and Aux-2 bridges, T1, T3 switches in main bridges are turned ON.

III. SIMULATION RESULTS

To see the performance of the proposed system, some simulations were performed using the Mat lab. One particular characteristic of the proposed HFL is that all the single dc sources depend on the adjustable dc source.

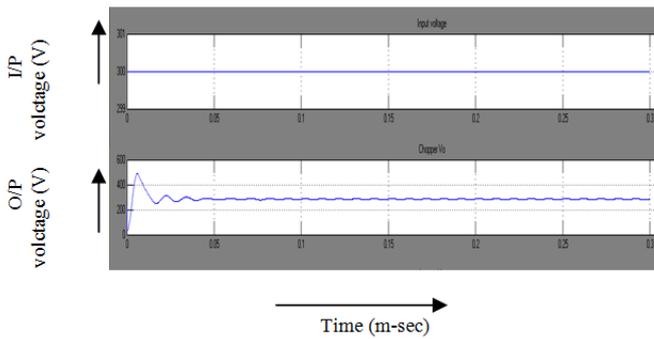


Figure 3. Simulation result of chopper

Fig.3. shows the waveform for input voltage is 300V and Chopper output voltage is 285V with 95% of Duty Cycle with respect to time.

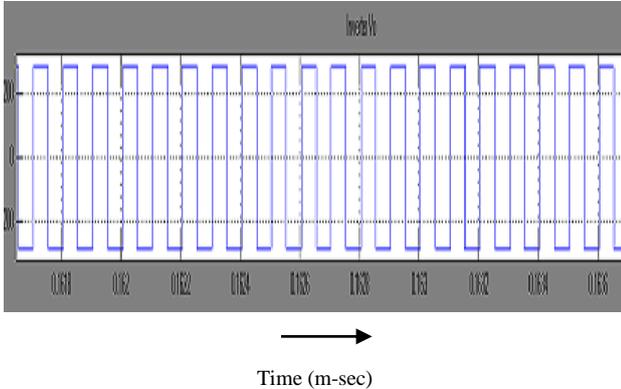


Figure 4. Simulation result of Inverter

Fig.4.shows the waveform for High Frequency Inverter output voltage is 285V with respect to time in m-sec. The gate pulses are given to the inverter with 50% of the duty cycle, frequency is 10 kHz.

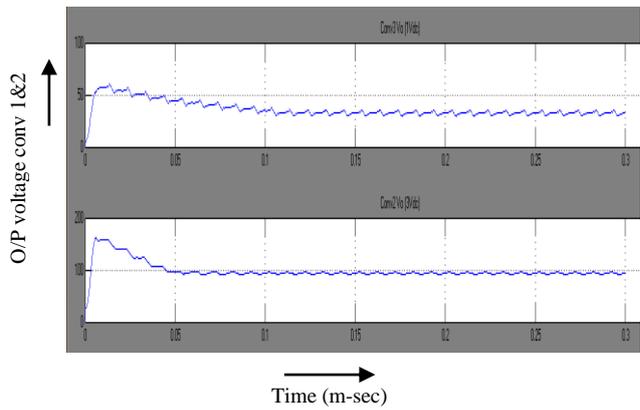


Figure 5. Simulation result of Converter 1&2

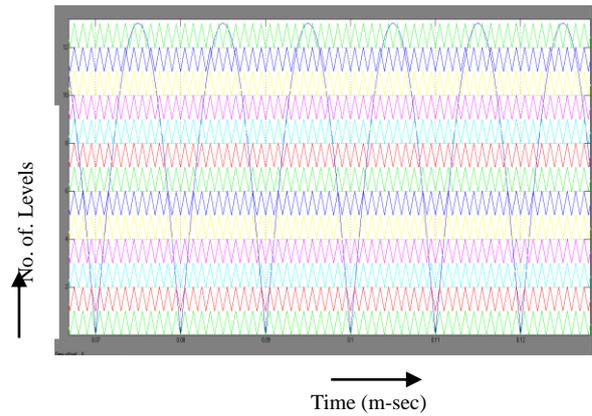


Figure 6. Simulation result of gate pulse

Having more than two voltage levels to build a sinusoidal shape it is intuitive that we can have reduction of the current harmonics in the load. Nevertheless, the actual improvement of the current spectrum depends on the control technique employed. The most popular control technique for traditional inverters is the sinusoidal or “sub harmonic” natural pulse width modulation (PWM) method. Its popularity is due to its simplicity and to the good results it guarantees in all the operating conditions, including “over modulation,” which allows first harmonic. A complete analysis of both bipolar (for two-level inverters) and unipolar (for three level inverters) methods has been widely performed. We now develop a analysis of the MCPWM method for multilevel inverters. We refer to the system outlined in Fig.6. For the proposed multilevel generalization of the PWM method; we take the unipolar technique as a starting point. The idea we follow is to use several triangular carrier signals, keeping only one modulating sinusoidal signal. If an N-level inverter is employed, N - 1 carrier will be needed.

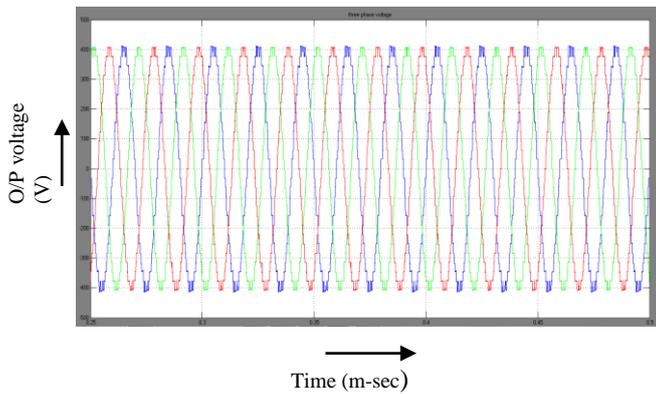


Figure 7. Simulation result of Buck converter with R-Load

The complete topology is modeled using MATLAB tool box and the control logic is tested. The regulated dc output obtained from the first stage converter (Buck) which ensures input voltage to the main bridge and also given to the HFI. The inverter output given to the transformer primary, which has turns ratio of 9N, and in second stage, transformer secondary is divided into 3N and 1N output of the transformer is connected to the bridge rectifiers. The 9:3:1 voltage ratios are input to the cascaded multilevel inverter. Resulting that 27 level output voltage is obtained which depends upon the gate pulse of switches. Multi carrier PWM technique is used in gating. Fig.7.shows the purely resistive load the shape of the current waveform is exactly similar to the voltage waveform. Total Harmonic Distortion is 5.05% for Buck converter with R Load.

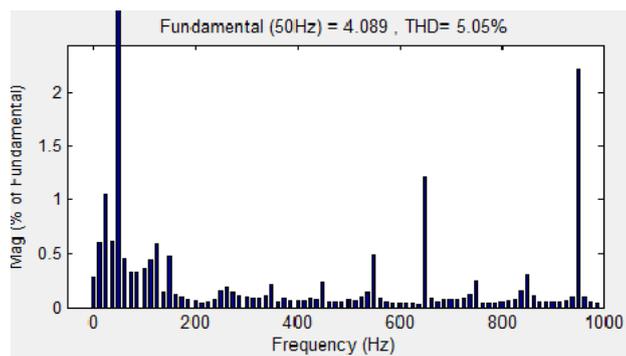


Figure 8. FFT analysis for buck converter

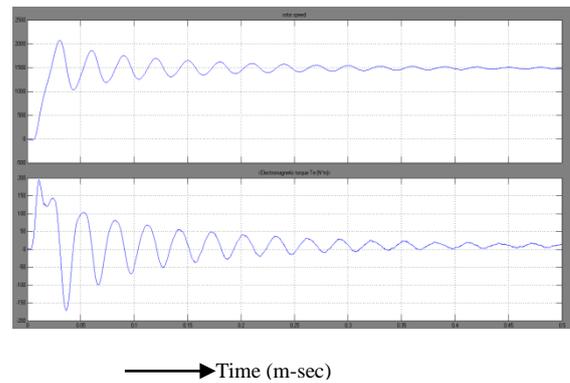


Figure 9. Simulation result of speed and Torque with Motor Load (using Buck converter)

The speed and Torque simulation waveform of buck converter with motor load as shown in fig 9. In which speed is 1500 rpm and the electromagnetic torque is 22.

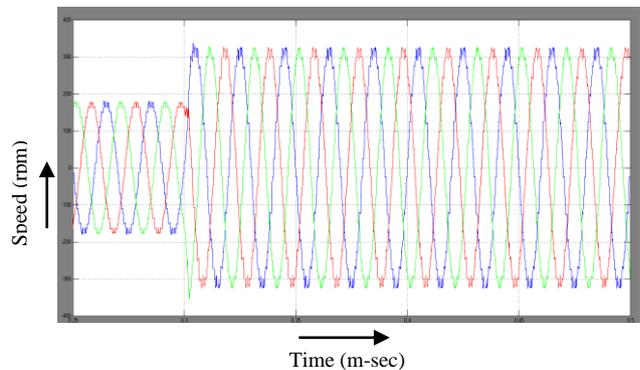


Figure 10. Simulation result of three phase Buck converter with Motor Load

Output voltage of buck converter with motor load as shown in fig 10. In Buck mode the output voltage is 145V and the Boost mode the output voltage is 230V.

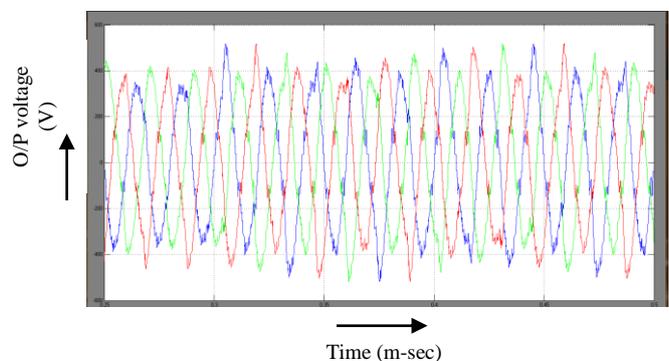


Figure 11. Simulation result of three phase Buck-Boost converter with Motor Load

Fig.11.shows the Output voltage waveform for three phase.Asymmetrical Multilevel Inverter (Buck-Boost) converter with motor load, range is 325V with respect to time m- sec.

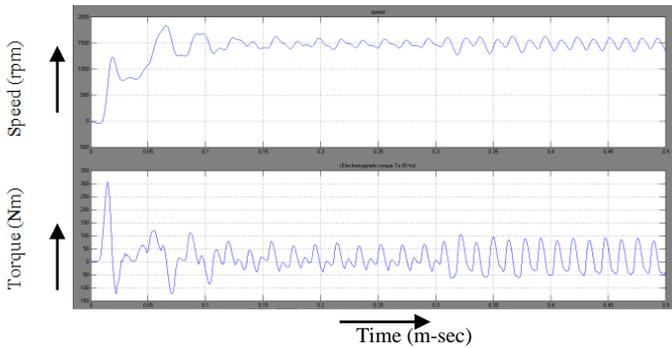


Figure 12. Simulation result of Torque & Speed three phase Buck-Boost converter with Motor Load

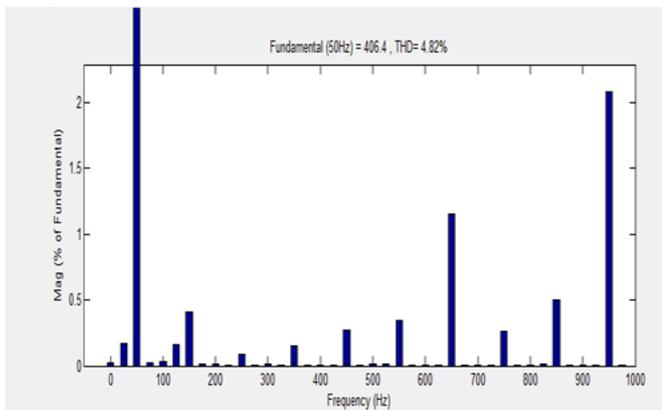


Figure 13. FFT Analysis for Buck-Boost

TABLE-II. VARIOUS OUTPUT VOLTAGES

Duty Cycle (%)	Main Bridge (O/P)	Auxiliary Bridge-1 (O/P)	Auxiliary Bridge-2 (O/P)	Total (O/P)
75	225	75	24.97	324.9
50	150	50	16.65	216.5
25	75	25	8.325	108.3
13	39	13	1.443	53.44

TABLE-III. PARAMETERS COMPARISON

Parameters	Existing method	Proposed method
Chopper	Buck converter	Buck-Boost converter
Input Voltage	300V	(150-300)V
Output Voltage	411.6V	325V
Output Current	4.33A	4.8A
THD	5.05%	4.82%

IV. CONCLUSION

An asymmetric cascaded multilevel inverter topology based on a small and cheap HFL has been implemented. In this technique, the required number of power supply is one instead of using large number of power supply, allowing their application in EVs. A 27-level type using Multicarrier Pulse Width Modulation Control was implemented to demonstrate some of its advantages: excellent voltage waveforms, THD reduces and and, hence, almost perfect current waveforms. It increases the efficiency of the inverter because of the MAIN converters, which manage more than 80% of the total power, work at the fundamental frequency instead of 10 – 20 kHz, which are normal switching frequencies which are used in two- or three – level converters. Only the HFL works at those frequencies, but it switches only four transistors and represents less than 20% of the full power. The HFL solution can also be used for many other purposes, such as machine drives for industry applications or high-power active front-end rectifiers. If the variable dc source is adjusted using a chopper, only one transistor needs to be controlled to drive the traction motor. A very simple scheme, based on a small and cheap HFL allows utilization of only one power supply for the complete multilevel inverter drive, with an inherent regulation of the voltages supplied among the H-bridges are implemented. This technique in multilevel inverters becomes a real solution for EV and HEV applications.

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