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Design and Implementation of Parallel Micro-programmed FIR Filter Using Efficient Multipliers on FPGA

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ABSTRACT

Impulse Response Filter plays an important part in digital signal processing applications such as video, audio and image processing. The performance of FIR filter is improved by using efficient multipliers and adders. In this paper 8 tap parallel microprogrammed FIR filter architecture is implemented using Wallace tree and Vedic multiplier. The designs are realized using Xilinx Virtex-5 FPGA. FPGA results are presented and analyzed. Implementation theresults are presented and analyzed. Based on the implementation results, parallel FIR filter using Wallace tree multiplier/carry skip adder combination proves to be more efficient as compared to other multiplier/adder combinations both Wallace tree and Vedic multiplier compared to the existing work. Hence proposed method is more efficient.

Keywords : FPGA, FIR filter, parallel micro programed, Multiplier.

I. INTRODUCTION

Digital filters are the discrete time systems that are used for filtering of arrays. The filtering operations performed in filtering operations are low pass, high pass, band pass and band reject. The basic building blocks for the implementation of digital filters are adders, multipliers and shift registers. The transfer function can be achieved by realizing the different architectures of digital filters. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) are the two digital filters used in many applications such as image, signal, audio and video processing. Frequency response characteristics of a FIR filter can be realized by varying the weights of the filter coefficients and number of filter taps. The FIR filter performance is better than analog filter techniques. FIR filters performs convolution on window of N data samples which can be expressed as follows

$$Y(n) = \sum_{i=0}^{N-1} H(i).X(n-i)$$

In general for N-tap or (N-1) th order FIR filter consists of N shifters, N multipliers and N-1 adders. The implementation of transposed form FIR filter is shown in Fig. The objective of this paper is to design parallel microprogrammed FIR filter architecture for 8 tap using Wallace and Vedic multipliers and implementation on FPGA.

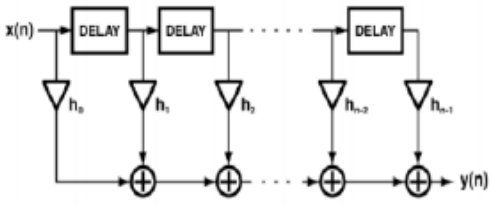


Figure 1: Transposed form FIR filter

II. MICROPROGRAMMED FIR FILTER

The microprogrammed FIR filter consists of micro program control unit and data path unit. The advantage of Microprogrammed control unit is its flexibility, many additions and any changes can be

done by changing the microinstructions in the memory.

III. PARALLEL ARCHITECTURE OF MICROPROGRAMMED FIR FILTER

The parallel architecture utilizes multiple adders and multipliers, based on the size of the FIR filter, in contrast to single adder and multiplier used in the sequential architecture design. Fig. illustrates the parallel architecture of the

Microprogrammed FIR filters. For example, the data path micro architecture of 4-tap parallel FIR filter consists of the following sub-modules:

- Four 8-bit data registers
- One 2-to-4 decoder
- Four 8-bit coefficient registers
- Four multipliers (8×8)
- Three 16-bit adders
- One 16-bit register for latching the output

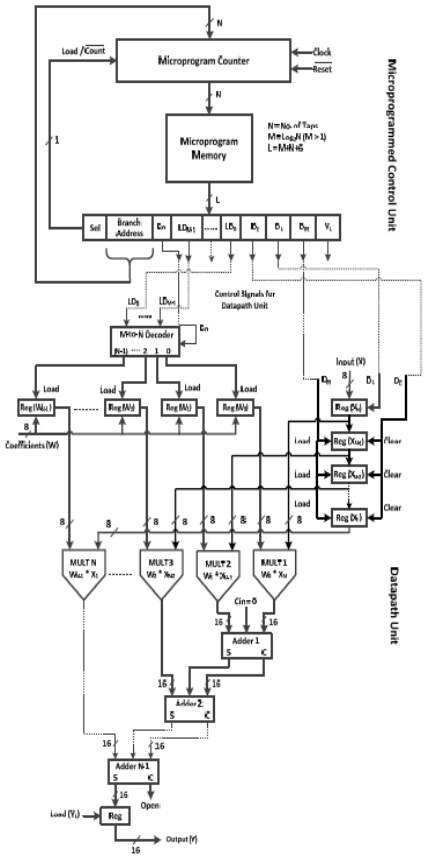


Figure 2 : Architecture of parallel microprogrammed FIR filter

A. WALLACE TREE MULTIPLIER DESIGN

Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integers. Multiplication of two integer numbers is carried out in three steps.

1. Multiply each bit of a multiplier with same bit of multiplicand. Depending on the position of multiplier bits generated partial products have different weights.
2. Reduce the number of partial products to two by using layers of full adders and half adders.
3. Group the wires into two and adder them using conventional adder.

The advantage of Wallace tree is that it has small delay. By using a Wallace tree the number of logic levels required to perform a summation can be reduced. The disadvantage is that layout is complex and it has irregular wires. In this paper, Wallace tree architecture uses carry skip adder .The carry skip reduces the delay in the carry chain of Ripple Carry Adder (RCA) and checks if a carry propagates through a next block. The advantage of using CSA is to improve the speed.

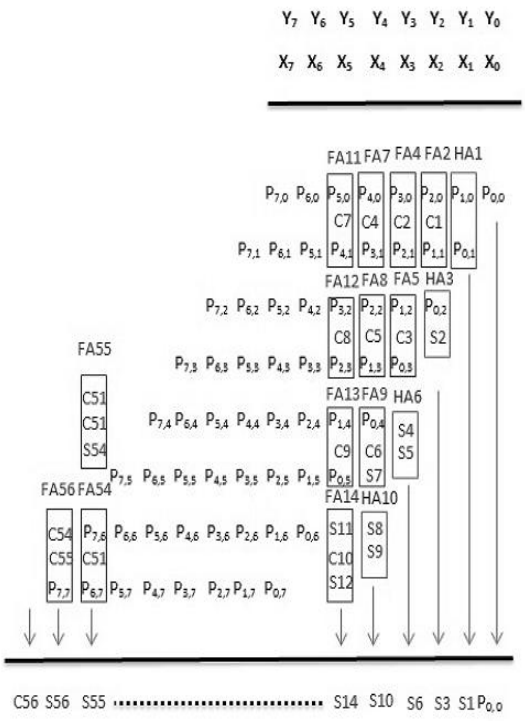


Figure 3 : Wallace tree multiplier using full adders and half adders

B. VEDIC MULTIPLIER DESIGN

Vedic mathematics is an ancient form of mathematics which was developed in India by Sri Bharati Krishna Tirthaji, a renowned Sanskrit scholar and mathematician of his times. It is based on sixteen Sutras or algorithms.

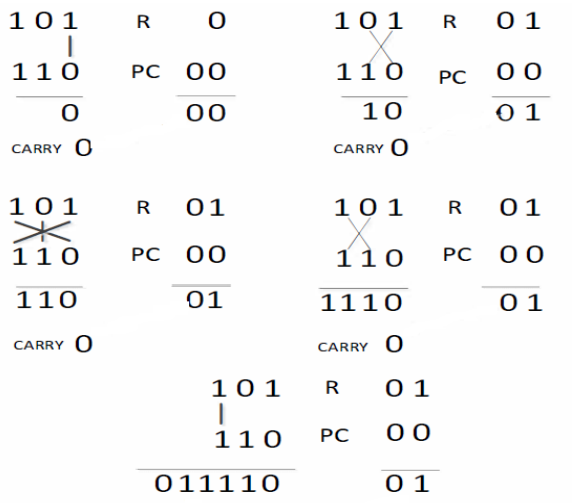


Figure 4 : Example of Urdhva Tiryakbhyam algorithm

UrdhvaTiryakbhyam Sutra (vertically and crosswise algorithm) is used

For efficient digital multiplication. Its calculation is defined by vertical and crosswise product that gives advantage over the normal conventional horizontal multiplication. For binary number, the multiplication operation is reduced to bitwise "AND" operation and the addition operation use full or half adders.

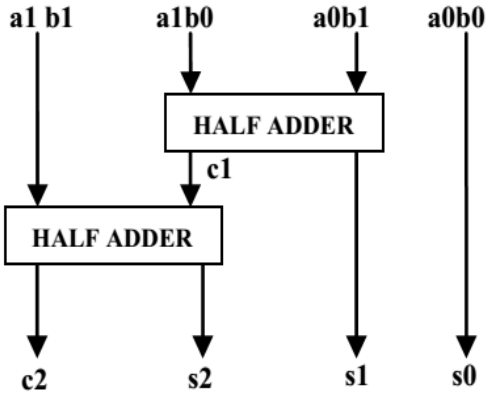


Figure 5 : 2x2 Vedic Multiplier

The Vedic mathematics concept is applied to develop modular RTL Verilog code for 2×2 multiplier which can be used as a building block to develop 4×4 multiplier. An 8×8 multiplier can be further designed using the 4×4 multiplier and so on. The 4-bit and 8-bit multipliers used conventional half and full adders for the proposed design. The same Vedic multiplier design is realized using Kogge-Stone adder (KSA). KSA is a parallel prefix form of carry look-ahead adder. It generates the carry signals in $O(log2N)$ time, and is thus widely considered as the fastest adder design possible.

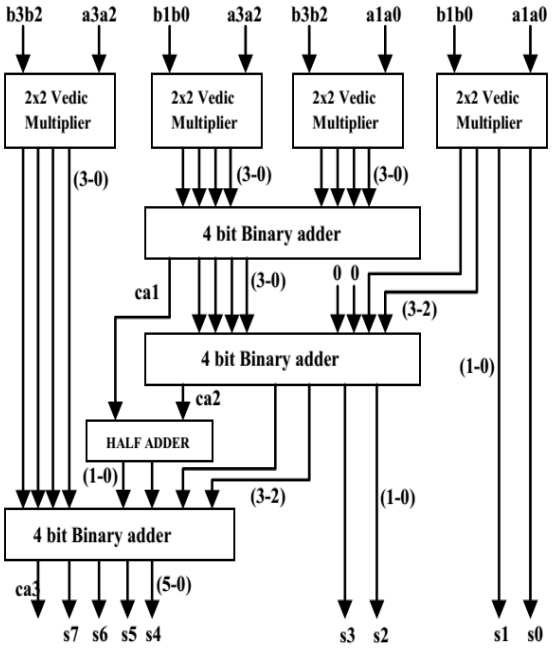
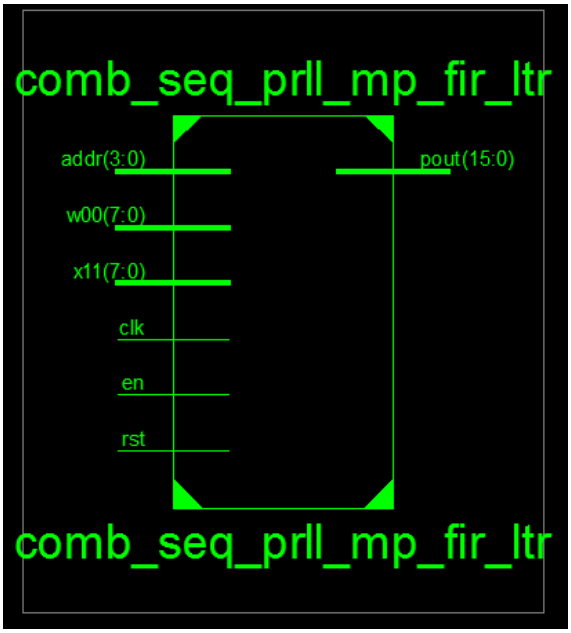


Figure 6 : 4x4 Vedic Multiplier

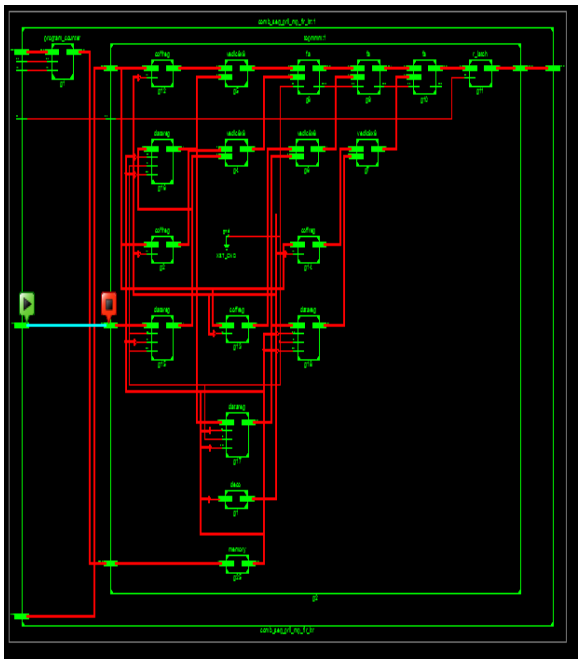
IV. SIMULATION RESULT

The FIR filter designs are coded in Verilog hardware description language (HDL) and implemented in FPGA using Xilinx Virtex-5 (xc5vlx50t-1ff1136) as the target device. The Wallace tree and Vedic multipliers are used in parallel architecture of micro programmed 8 tap FIR filter. The FPGA resource utilization table includes slice look-up tables (LUT's), minimum period and maximum clock frequency.

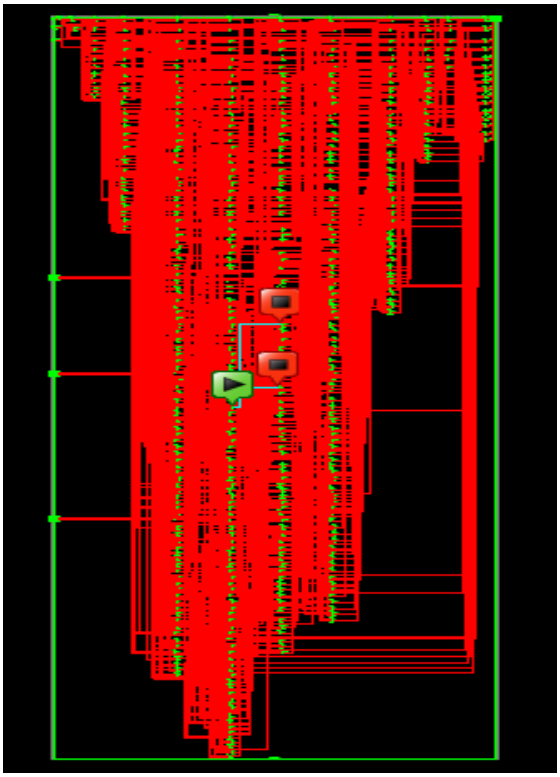
Block diagram



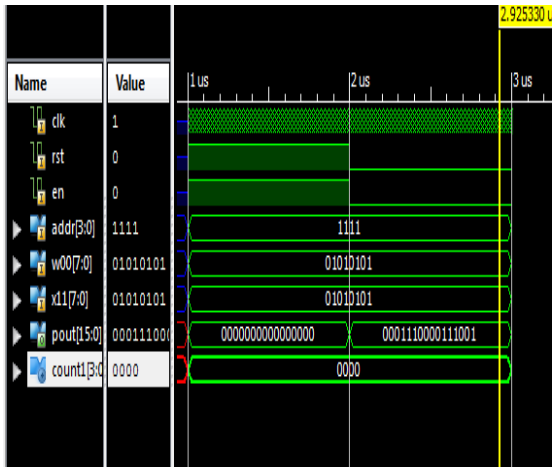
RTL Schematic Diagram



View Technology Schematic



Simulation output waveform



V. CONCLUSION

Digital filters are one of the main elements of DSP. The most commonly used digital FIR filter consists of multiply and accumulate structure. Since the performance of FIR filter depends on the multiplier used, an enhanced and improved multiplier will enhance the overall system performance. In this paper

we designed and implemented parallel microprogrammed 8 tap FIR filter architecture in Xilinx Virtex-5 FPGA using Wallace tree multiplier/conventional adder, Wallace tree/carry skip adder, Vedic multiplier/conventional adder and Vedic multiplier/Kogge-Stone adder combinations respectively. Based on the implementation results the proposed method proves that the FPGA resource utilization of Wallace tree and Vedic multiplier has improved as compared with the existing method.

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