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An Inverter with Coupled Inductor

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ABSTRACT

Energy request is expanding step by step. To meet this sustainable power sources must be joined. Sustainable power sources like PV cells, energy units deliver DC voltage. For house hold reason and modern reason this DC voltage must be changed over into AC voltage. For this power electronic inverters are utilized. Multilevel inverters has across the board acknowledgment as it would synthesis be able to relatively sinusoidal wave shape. This paper manages a solitary stage multilevel inverter which can deliver a five level AC yield voltage from a solitary DC source. The task instrument of this inverter is examined in detail. Reproduction and also the model demonstrates the plausibility of the paper.

Keywords: Coupled Inductor, Multilevel Inverter, Power Converter, Pulse Width Adjustment.

I. INTRODUCTION

Multilevel inverters have changed the substance of medium and high voltage drives. The most prominent single stage multilevel topologies are the diode-braced, capacitor cinched and fell composes [1]-[4]. There exist numerous different topologies. So multilevel inverter topologies can be grouped into two sorts: Type I and Type II. Sort I utilizes various DC voltage sources and Type II utilizes numerous (split or cinching) DC voltage capacitors [5]. As the level expands, the required number of DC sources likewise increments in Type I. This made the utilization of Type I a restricted one. Sort II is restricted basically by the adjusting of the capacitor voltages. So the most attractive topology might be, a multilevel inverter with single source and no split capacitor. Multilevel inverters with coupled inductors require just a single source other than split capacitors are not required. For the inverter with coupled inductor, a three appendage coupled inductor is the most attractive one; however coupled inductor with high inductance esteem isn't favored [6]. The examination of the coupled-inductor outlines in [7] proposes that lessening the objective inductance of the coupled inductor could enhance the general adjust of misfortunes in the coupled inductor, with just a minor increment in swell current. The quantity of voltage levels can be expanded by utilizing a part twisted coupled inductor inside every inverter-leg and utilizing interleaved pwm switching of the upper and lower switches [8]. The coupled inductor provides excellent protection against dc-rail shoot-through conditions.

II. FIVE LEVEL INVERTER TOPOLGY

The inverter used in this paper can synthesis an AC voltage with five levels from a single DC source. Besides in this inverter, no voltage split capacitors are used. Figure1 shows the circuit of the single-phase five level inverter. 2E is the dc-link voltage and L1 and L2 are the coupled inductors. The mutual inductance of the two inductors is M and the output terminals of this inverter are 1 and 2.

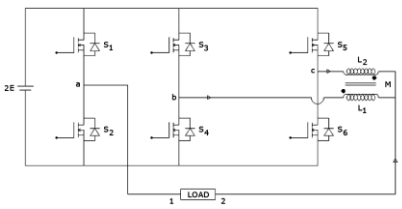

Figure 1. Single-phase five-level inverter

A. Switching States for Five Level Output Voltage

The power switches in one arm are assumed to switch complementarily. For an instant switch S1 is ON then the switch S2 must made OFF and vice versa. Similarly in case of S3, S4 and S5, S6. The details of the switching state is given in the below table.

Table 1. Switching states for five-level output voltage

S_1	S_3	S_5	u_{12}
1	0	0	+2E
1	0	1	+E
1	1	0	+E
1	1	1	0
0	0	0	0
0	0	1	-E
0	1	0	-E
0	1	1	-2E

The number "1" is used to denote the ON state of one switch and "0" will be used to denote the OFF state. There are mainly four switching states in this inverter circuit. In each case one of the upper switches or a combination of the upper switches is made ON and similarly on the bottom switches. The assumption taken for explaining the cases are the inductance L1, L2 of the coupled inductor are equal and the leakage inductance, Lk is zero. Case-1 (+2E): In this case, the required output voltage level is +2E. To achieve this upper switch S1 is turned ON along with the lower switches S4 and S6 are turned ON. The equivalent circuit becomes Figure 2

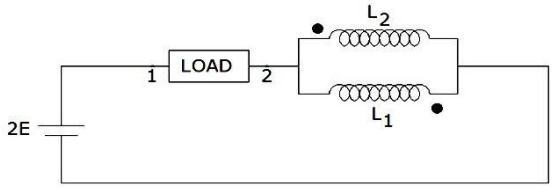

Figure 2. Equivalent circuit of case1

The inductors are parallel and opposing. So the net or equivalent inductance is

$$\frac{L_1 L_2 M^2}{L_1 + L_2 + 2M} \qquad (1)$$

The inductance of the coupled inductor can be expressed as the sum of mutual inductance and the leakage inductance. By considering the assumption it can be stated as L1 = L2 = (mutual inductance + leakage inductance) = M + Lk. By substituting this in the above equation, the net equivalent inductance become

$$\frac{L_k}{2} \qquad (2)$$

So the net equivalent circuit become Figure 3.

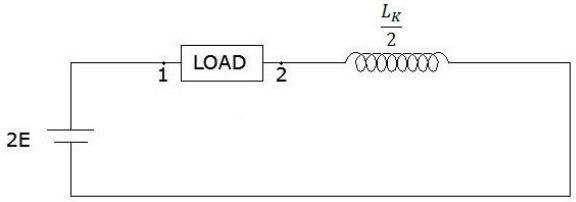

Figure 3. Net equivalent circuit of case1

The leakage inductance, Lk is assumed to be zero. So +2E voltage across the load. Case-2 (+E): In this case, the required output voltage level is +E. To achieve this there are two options. Option-1 with upper switches S1, S5 are turned ON along with lower switch S4 is turned ON. Option-2 with upper switch S1, S3 are turned ON along with lower switch S6 is turned ON. The equivalent circuit becomes Figure 4.

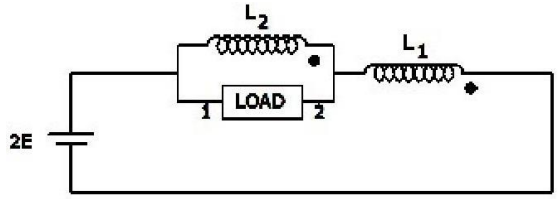

Figure 4. Equivalent circuit of case2

Now apply Thevenin theorem. Thevenin voltage is given by the Figure6. The inductors share the applied voltage equally. So voltage across L2 is +E. Thevenin impedance is given by the Figure7. Inductors are parallel and opposing. So the net inductance is given by

$$\frac{L_k}{2} \qquad (3)$$

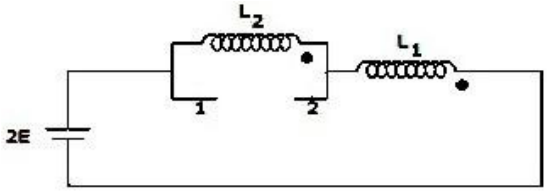

Figure 5. Load is removed from the equivalent circuit of case-2

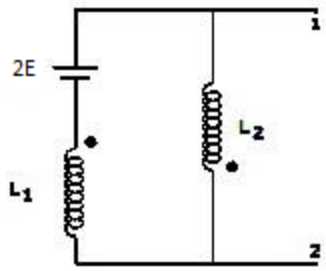

Figure 6. Thevenin voltage of case-2

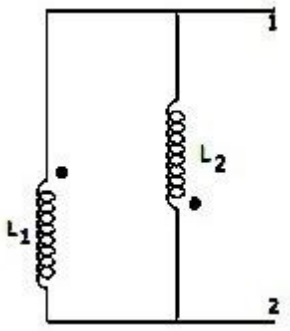

Figure 7. Thevenin impedance of case-2

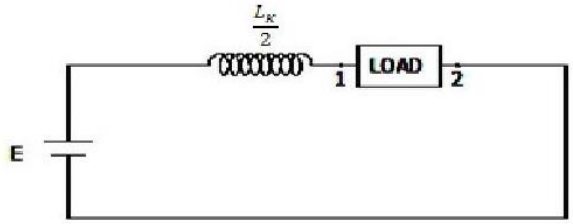

Figure 8. Thevenin equivalent circuit of case-2

The Thevenin circuit is given by the Figure8. The leakage inductance, Lk is assumed to be zero. So +E voltage across the load.

Case-3 (-E): In this case, the required output voltage level is -E. To achieve this there are two options. Option-1 with upper switch S5 turned ON along with lower switches S2, S4 are turned ON. Option-2 with upper switch S3 turned ON and lower switches S2, S6 are turned ON. The equivalent circuit becomes Figure9. By applying Thevenin theorem as in the previous case, the Thevenin equivalent circuit is given as Figure10. The leakage inductance, Lk is assumed to be zero. So -E voltage across the load as the load is connected from 2 to 1.

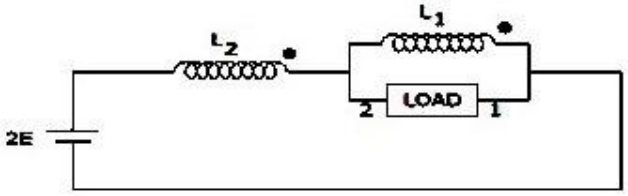

Figure 9. Equivalent circuit of case3

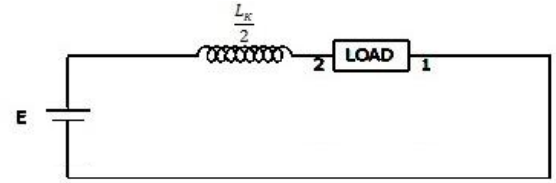

Figure 10. Thevenin equivalent circuit of case-3

Case-4 (-2E): In this case, the required output voltage level is 2E. To achieve this, upper switches S3, S5 are turned ON along with the lower switch S2 is turned ON. The equivalent circuit becomes Figure 11.

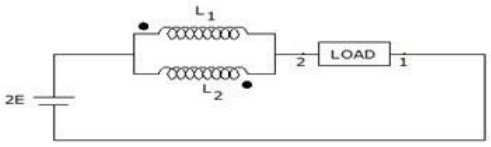

Figure 11. Equivalent circuit of case4

The inductors are parallel and opposing. So the net or equivalent inductance is

$$\frac{L_1 L_2 M^2}{L_1 + L_2 + 2M} \qquad (4)$$

As in case-1, by considering the assumption it can be stated as L1 = L2 = (mutual inductance + leakage inductance) = M + Lk. By substituting this in the above equation, the net equivalent inductance become

$$\frac{L_k}{2} \qquad (5)$$

So the net equivalent circuit become Figure12 The leakage inductance, Lk is assumed to be zero. So -2E voltage across the load as the load is connected from 2 to 1.

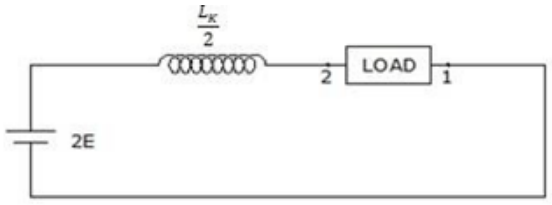

Figure 12. Net equivalent circuit of case4

B. Pluse Width Modulation

By proper modulation the existence of the DC component in the output voltage can be reduced. The DC components in the output voltage result in large current, which may result in the failure of the inverter. By modulation the size and weight of the coupled inductor can be reduced.

III. SIMULATION RESULTS

To verify the validity of the paper, the circuit in this paper is simulated using MATLAB/Simulink tool. The inverter is tested with series connected RL load. A 70V DC source is given as the input. Gate signals to the switches are given according to the data given in the Table I. MATLAB simulation is given in the Figure 13.

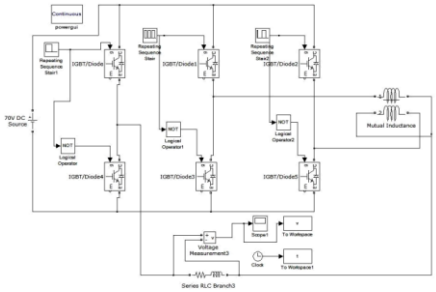

Figure 13. Simulation of five level inverter with coupled inductor for R-L load

A five level AC voltage is obtained as the output with the input DC voltage as the maximum value. The frequency of the output wave form is 50Hz. Simulation result is given in the Figure 14.

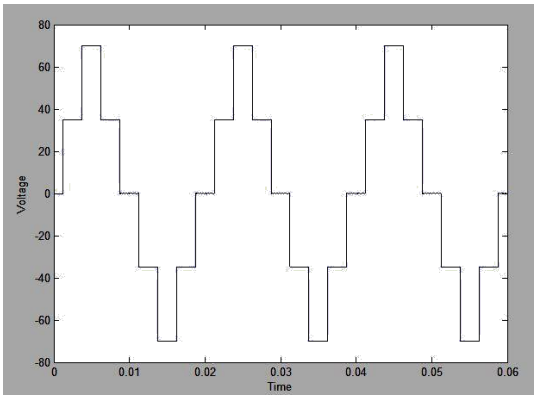

Figure 14. Simulation result of five level inverter with coupled inductor for R-L load

IV. EXPERIMENTAL RESULTS

Equipment area comprises of three sections; control circuit, drive circuit and power circuit. In the control circuit entryway signals for the switches are created by the rationale given in Table I. To deliver beat width tweaked door flag PIC18F4550 is utilized. Driver circuits are utilized to support the door flag to the required driving voltage of the switches. FAN7392 is utilized to drive the MOSFET. It is a solid high and low side entryway drive IC that can drive the rapid MOSFETs. A solitary FAN7392 can deal with two switches on a similar arm. The power circuit comprises of MOSFET IRF830 and the coupled inductor with shared inductance of 1mH. The exchanging recurrence is 7kHz. The yield is taken over the heap of 470ohm and 1.1mH. The information given to the equipment is 70V DC. A five level AC voltage with a pinnacle of 70V is gotten as the yield. The recurrence of the yield waveform is 50Hz. The Figure15 is the gotten yield wave shape. When all is said in done, from a solitary DC source, a five level AC voltage is acquired with the info DC voltage as the most extreme esteem. Research center model of the five level inverter is appeared in the Figure 16.

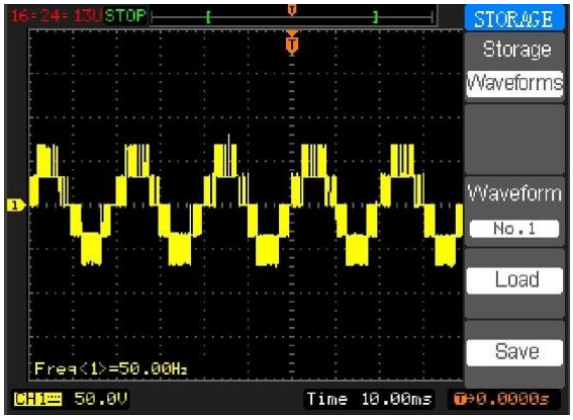

Figure 15. 70V Five level AC output voltage

V. CONCLUSION

The inverter in the paper would synthesis be able to a five level AC yield voltage. Activity system of this inverter was investigated and the recreation is finished utilizing MATLAB/Simulink device. It required just a solitary source to deliver the five level yield. Heartbeat width balanced door signals are utilized as a part of the model. Check of the outcome demonstrates the legitimacy of the inverter.

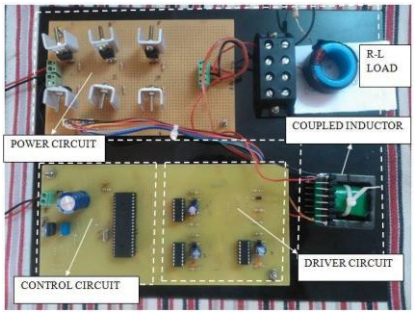

Figure 16. Laboratory prototype of the single phase five level inverter

VI. REFERENCES

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