



Design and Switching of Single Phase Five Level Cascaded H-Bridge Multilevel Inverter Using SPWM Technique

Shubham Gajbhiye¹, Esha Vyas², Trupti Kapse², Prof. Abhijit Dutta³

¹Student BE 8th Sem Dr. Babasaheb Ambedkar College of Engineering and Research, Nagpur, Maharashtra, India

²Student Dr. Babasaheb Ambedkar College of Engineering and Research, Nagpur, Maharashtra, India

³Assistant Professor Dr. Babasaheb Ambedkar College of Engineering and Research, Nagpur, Maharashtra, India

ABSTRACT

The utilization of multilevel inverter in medium and high power applications is increasing for improving the power quality. The multilevel inverter was introduced as a solution to increase the converter operating voltage above the voltage limits of classical semiconductors. The function of the multilevel inverter is to synthesize a desired high voltage from several levels of dc voltages. The multilevel inverters are becoming popular as they have low harmonic contents, better electromagnetic compatibility and lower switching losses. This paper deals with a single phase five level cascaded H-bridge multilevel inverter with R-load. Sinusoidal Pulse Width Modulation technique is used to develop the switching pattern for the five level H-bridge multilevel inverter to reduce the total harmonic distortion at the output. A Pi filter is used to further reduce the total harmonic distortion and improve the power quality. This paper also compares the percentage THD of multilevel inverter with and without filter. It has been shown that the total harmonic distortion in multilevel inverter with filter is less than that in multilevel inverter without filter.

Keywords: Multilevel inverter (MLI), cascaded H-bridge (CHB), total harmonic distortion, sinusoidal pulse width modulation, Common mode voltage (CM)

I. INTRODUCTION

Power electronics circuits play vital role in production of electricity using renewable energy sources. It is mainly used to convert and control the signal. It converts the sources, either from DC/AC to AC/DC. To avoid the entire harmonic content filters are used.

Multilevel inverters are applied in the area of medium voltage and high power applications. It

produces a desired MLI output voltage from the separate DC sources. The number of output voltage levels 'n' is determined by the number of separate dc sources 's' using the formula $n=2s+1$. When $s=2$, then the level of the inverter is $n=5$ [1].

Demand for high-voltage, high power converters capable of producing high-voltage quality waveforms while utilizing low voltage devices and reduced switching frequencies has led to the multilevel inverter development with regard to

semiconductor power switch voltage limits. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages [2].

The concept of multilevel converters was introduced in 1975. The term multilevel began with the three level converters. Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. The steps are supplied from different DC levels supported by series connected batteries or capacitors.

Advantages of multilevel inveter

Compared with the traditional two-level voltage converter the primary advantage of multilevel converters is their smaller output voltage step, which results in high power quality, lower harmonic components, better electromagnetic compatibility, and lower switching losses. Multilevel inverters make small Common mode voltage; consequently the stress in the bearings of a motor allied to a multilevel motor drive can be condensed. In addition CM voltages can be eliminated by using advanced modulation technique. Multilevel inverters can draw input current with low distortion [3].

Topologies of multilevel inverter

Topologies for multilevel inverter have been classified as shown in figure 1.

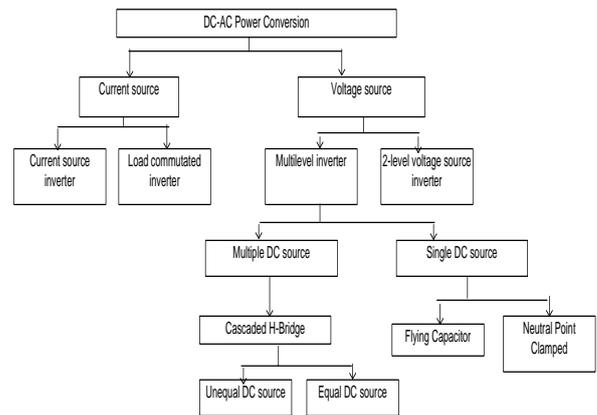


Figure 1. Classification of inverter topologies

Comparison of multilevel inverter topologies

Table 1 shows the comparison between the various topologies of multilevel inverter

Table 1. Comparative study between various classical topologies of multilevel inverter.

Characteristic s	Cascaded H-Bridge	Diode-Clamped	Flying capacitor
Main switching device	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	0	(m-1)(m-2)	0
DC Bus Capacitor	(m-1)/2	(m-1)	(m-1)
Balancing capacitor	0	0	(m-1)(m-2)/2
Redundancy	Redundant	Not redundant	Redundant
DC Bus sharing	Separate DC source	DC Bus sharing	DC Bus sharing
Structure	Modular	Not modular	Not modular
Flexibility	Flexible	Not flexible	Not flexible

Cascaded H-Bridge Multilevel Inverter

The number of output voltage levels ‘n’ is determined by the number of separate DC sources ‘s’ using the formula $n=2s+1$. When $s=2$, then the level of the inverter is $n=5$ [1].

The separate DC voltages are V_1 and V_2 given to the MLI, it operates with eight switches $Q_1, Q_2, Q_3, Q_4, Q_5, Q_6, Q_7$ and Q_8 as shown in figure 2.

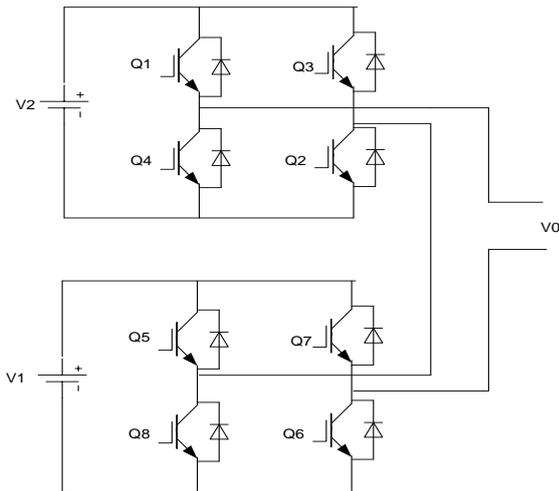


Figure 2. Five level cascaded H-bridge multilevel inverter

Modes Of Operation

The input voltages $V_1=40V$ and $V_2=40V$ are given. The switches Q_1, Q_2, Q_5 and Q_6 operate to produce the output voltage $V_o=80V$. The switches Q_1 and Q_5 operate to produce the output voltage $V_o=40V$. The switches Q_1, Q_2, Q_5 and Q_6 operate to produce output voltage $V_o=0V$. The switches Q_3 and Q_7 operate to produce the output voltage $V_o=-40V$. The switches Q_3, Q_4, Q_7 and Q_8 operate to produce the output voltage $V_o=-80V$. Thus staircase output voltage waveform is generated as shown in table 2.

Table 2. Eight Modes Operation

V_o	$2V_1$	V_1	0	$-V_1$	$-2V_1$
Q1	1	1	1	0	0

Q2	1	0	1	0	0
Q3	0	0	0	1	1
Q4	0	0	0	0	1
Q5	1	1	1	0	0
Q6	1	0	1	0	0
Q7	0	0	0	1	1
Q8	0	0	0	0	1

Why cascaded multilevel inverter

The cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity, a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high voltage applications. The cascaded H-bridge multilevel inverters have been applied where high power and power quality are essential, for example, static synchronous compensators, active filter and reactive power compensation applications, photo voltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging [2]. Cascaded H-bridge multilevel inverter requires the least number of components for the same voltage level as compared to all three types of inverter [4]. Cascaded multilevel inverter features a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation. With an appropriate control strategy, it is possible to bypass the faulty module without stopping the load, bringing an almost continuous overall availability. H-bridge inverters have voltage boosting capability. It is highly reliable with lowest voltage unbalance problem. The CHB multilevel inverters can be divided into two groups from the viewpoint of values of the dc voltage sources: the symmetric and asymmetric topology. In the symmetric topology, the values of all the dc sources are equal. In the asymmetric types, the values of the

dc voltage sources of all H-bridges are dissimilar. The major advantage of asymmetric topology is its ability to create a substantial number of output voltage levels by using a low number of dc voltage sources and power switches but the high diversity in the magnitude of dc voltage sources is their most outstanding disadvantage.

Sinusoidal Pulse Width Modulation

In this method of modulation, several pulses per half cycle are used. Instead of maintaining the width of all pulses, the width of each pulse is varied proportional to the amplitude of a sine-wave evaluated at the centre of the same pulse. By comparing a sinusoidal reference signal with a triangular carrier wave, the gating signals are generated [1].

Good quality output voltage in SPWM requires the modulation index (m) to be less than or equal to 1. For $m > 1$ (over-modulation), the fundamental voltage magnitude increases but at the cost of decreased quality of output waveform [3].

The switching moments and commutation are established by the intersection of the carrier signal v_c and the reference signal v_r . By varying the modulation index M, the rms output voltage can be varied. Each pulse corresponds approximately to the area under sine wave between adjacent midpoints on off periods on the gating signals [5].

Pi Filter

Pi filter consists of a shunt capacitor at the input side, and it is followed by an L-section filter as shown in Figure 3. The pulsating DC output voltage is filtered first by the capacitor connected at the input side and then by another choke coil and then by another shunt capacitor. This filter is also called capacitor input filter.

The ultimate aim of a filter is to achieve ripple free DC voltage. In pi-filters, the major filtering action is accomplished by the capacitor at input C1. The residual AC ripple is filtered by inductor coil L and capacitor C2.

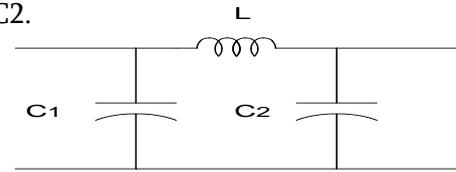


Figure 3. Pi filter

Advantages of pi-filter

Pi filter offers low voltage drop across choke coil and capacitor C2 in order to maintain high output voltage across its output terminals. Due to the involvement of two capacitors in addition with one inductor, pi filter provides improved filtering action. The peak inverse voltage in the case of pi filters is more in comparison to L-section filter.

Disadvantages of pi-filter

In an application where load current varies, pi-filters are not suitable.

II. SIMULATION RESULTS

Simulation of single phase five level cascaded H-bridge multilevel inverter without filter.

Figure 4. shows the pulse generation for MLI circuit by comparing the sinusoidal waveform with triangular waveform.

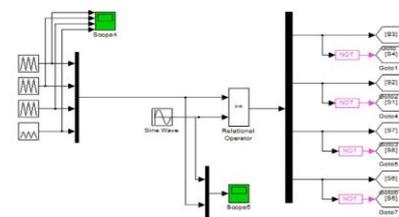


Figure 4. Pulse generation for MLI circuit

Figure 5 shows the pulse generation using carrier signal and reference signal.

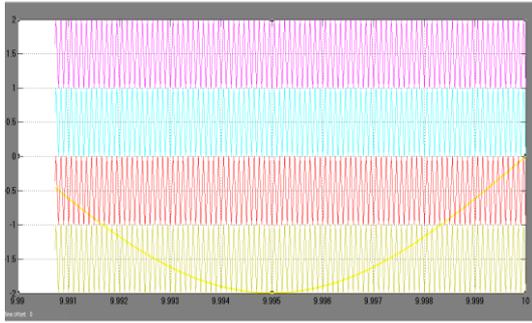


Figure 5. Pulse generated using carrier signal and reference signal.

Figure 6 shows the design of single phase five level cascaded H-bridge multilevel inverter without filter. Input supply, Vdc of 12 V is given and the R-load is of 100 ohms.

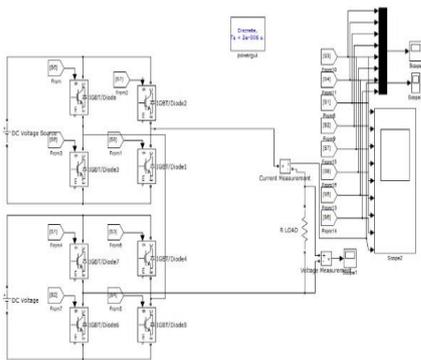


Figure 6. Design of single phase five level cascaded H-bridge multilevel inverter without filter.

Figure 7 shows the output voltage waveform of single phase five level cascaded H-bridge multilevel inverter without filter.

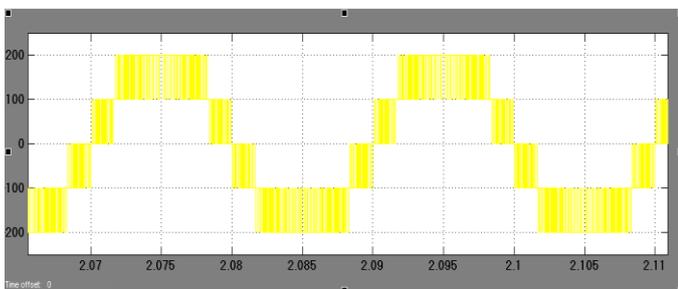


Figure 7. Output voltage without filter

Figure 8 shows the THD analysis of output voltage without filter.

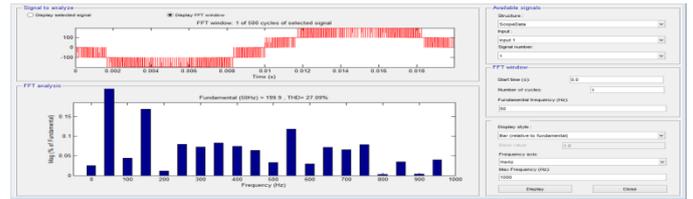


Figure 8. THD analysis of output voltage of single phase five level cascaded H-bridge multilevel inverter without filter. (THD=27.09%)

Simulation of single phase five level cascaded H-bridge multilevel inverter without filter.

Figure 9 shows the design of a single phase five level cascaded H-bridge multilevel inverter with pi filter. The output of the pi filter is connected to the resistive load.

Parameters for filter are taken as:-

$$L=0.24H$$

$$C1= C2=13.86 \mu F$$

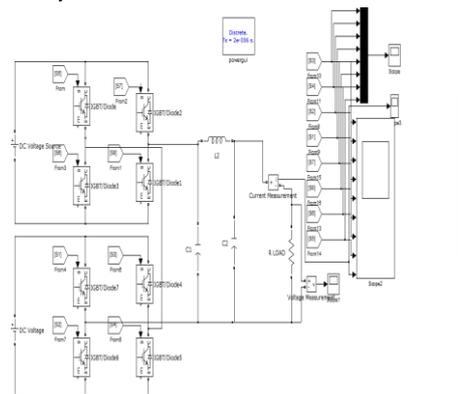


Figure 9. Design of single phase five level cascaded H-Bridge multilevel inverter with pi filter.

Figure 10 shows the output voltage waveform of single phase five level cascaded H-bridge multilevel inverter with filter.

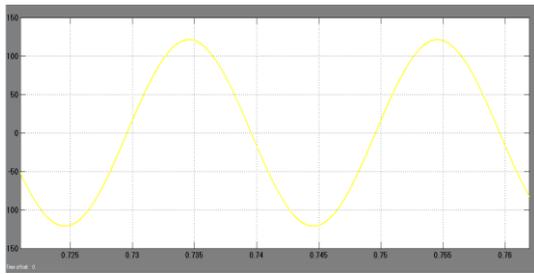


Figure 10. Output voltage with filter

Figure 11 shows the THD analysis of output voltage with filter.

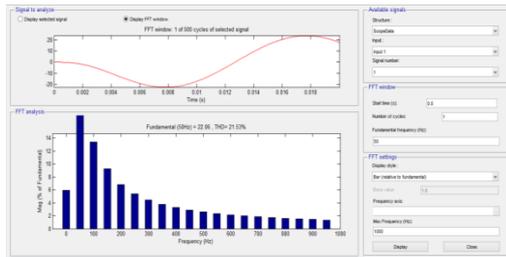


Figure 11. THD analysis of output voltage of single phase five level cascaded H-bridge multilevel inverter with filter. (THD=21.53%)

Comparison of THD values

Table 3 compares the THD values of the multilevel inverter with and without filter.

Table 3. THD Values

	Single phase five level cascaded H-bridge multilevel inverter with R-Load	
	Without filter	With filter
%THD	27.09	21.53

III. CONCLUSION

In this paper, the total harmonic distortion in multilevel inverter with and without filter is compared. The THD reduces when the filter is used and hence the power quality is improved. The %THD in multilevel inverter without filter is found to be 27.09 and that in multilevel inverter with filter is found to be 21.53.

IV. REFERENCES

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