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Implementation of High Speed Double Tail Comparator

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ABSTRACT

In recent years, with the advance of wireless communication systems, microelectronics and sensor technologies, wireless sensor networks (WSNs) are becoming a hot-spot for scientific research and industrial applications. High speed and low power comparators are very much essential in the design of a very good analog to digital converter. In this paper a novel high speed, low offset voltage and low power double tail comparator is designed and simulated. The proposed design does not use any preamplifier stages before the latch stage, which accounts for the direct reduction of power dissipation and silicon area. For power optimization, the MOSFETs of the input differential pair comparator are designed to operate in sub-threshold region rather than in saturation region. The designed double tail comparator consumes 366μW when operated from a 1.8V power supply. The operating speed of the design is 100MHz and exhibits a propagation delay of 600μs. The simulated propagation delay is found to be 600μs and the entire design of the proposed double tail comparator circuit is carried out in 180nm CMOS technology and verified using the cadence-spectre simulator.

Keywords: high speed, positive feedback, analog to digital converter (ADC), digital to analog converter (DAC), threshold, and offset voltage.

I. INTRODUCTION

Comparators play very crucial part in the design of several mixed signal systems. They are widely used in many applications such as high speed Analog to Digital Converter (ADC), Digital to Analog Converters (DAC) and higher order filters. ADCs have become a major component in driving the semiconductor industry over the past decade. Increased integration of various functional blocks within an integrated circuit single chip makes ADCs more conventional and they are able to offer very high speed along with low power consumption. The operating speed of a comparator circuit can be changed by changing the various parameters of a transistor. Though, it is not straightforward approach to scale down transistor dimensions, as it requires high channel doping, gate-induced drain leakage, and band to band tunneling across the junction. The difficulty of short channel effects in transistors also needs to be properly controlled. Furthermore, the design of analog circuits becomes more complex and reliability also concerns, when supply voltages (V_{DD}) need to be decreased according to the nano and micro dimensions of the transistors. Comparator's plays a key role on the overall performance of the ADC. Currently in most applications, there is a need for high speed and high resolution ADCs, in which an high speed and highly accurate comparator circuit is desirable. With only a few external components, it can perform a wide variety of analog signal processing tasks. Comparators are among the utmost widely used electronic circuits today, being used in a vast group of consumer, industrial, and scientific devices.

With the rapid improvements of computer aided design (CAD) tools, advancements of semiconductor

modeling, miniaturization in transistor scaling, and the developments in fabrication processes, the integrated circuit market is growing rapidly. Nowadays, Complementary Metal-Oxide Semiconductor (CMOS) technology has become dominant over Bipolar (BJT) technology for analog circuit design in a mixed-signal system due to the industry trend of applying standard process technologies to implement both analog circuits and digital circuits on the same chip. While many digital circuits can be implemented in smaller device lengths with a lower power supply voltage, most existing analog circuitry requires minimum voltage to operate or even a redesign to accomplish the same design. With transistor length being scaled down to a few tens of nanometers, analog circuits are becoming increasingly more difficult to design. Scaling down of CMOS feature sizes results in higher unity gain frequency (fT) which means the transistors operate faster than before. However, this is achieved at the cost of a reduction in transistor's open loop gain (AOL). Also due to scaling power supply voltage can be reduced. So because of this the weight and size of the battery reduces and enables longer battery life time. Hence for the same reason, low-powered circuits reduce thermal dissipation.

This paper is organized as follows. Section II presents the theoretical explanation of double tail comparator. Section III explains the working and design of the proposed comparator circuit. The simulated results and performance summary of the proposed double tail comparator circuit are presented in Section IV. Finally, conclusions are drawn in Section V.

II. COMPARATOR CIRCUIT

A comparator is a circuit that compares an analog signal with another analog signal or reference voltage and generates a binary signal. The output signal generated is based on the comparison of the two inputs. The schematic diagram of the proposed double tail comparator is shown in figure 1.The comparator is one of the most commonly used circuits for converting a given input analog signal to output digital signal. In the analog to digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the input analog signal. The important parameters considered in the design of a comparator circuit are speed, input capacitance, kickback noise, offset voltage, power dissipation and input common mode range.

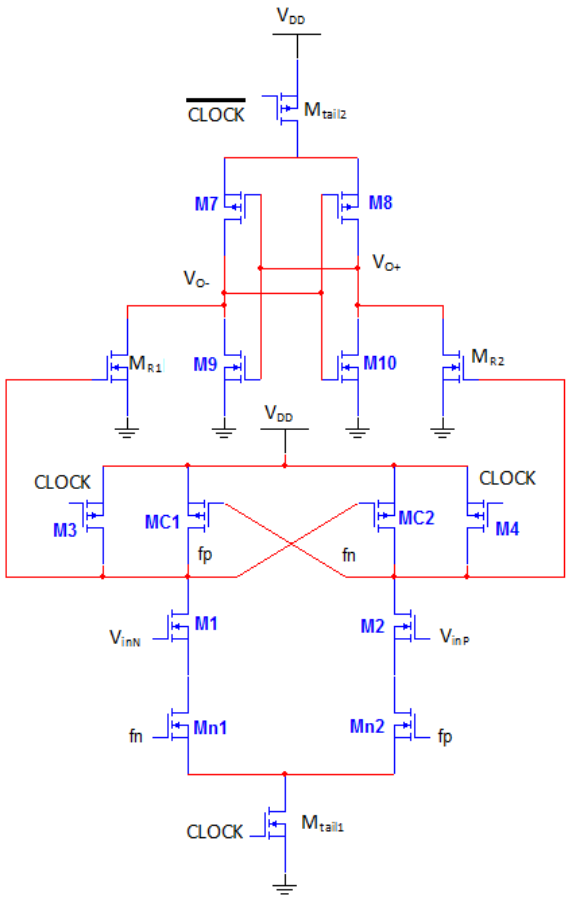

Figure 1. Schematic diagram of double tail comparator

In general, voltage comparator circuits are categorized into three types. They are open-loop comparators (operational amplifiers without compensation), Preamplifier based latch comparators (open loop comparator combined with dynamic regenerative latch) and fully dynamic latched comparator. The preamplifier based comparator consists of three stages

namely input amplifier stage, a latch stage and an output buffer stage. The preamplifier stage consists a differential amplifier with active loads. The preamp stage amplifies the input signal to improve the comparator sensitivity. It increases the minimum input signal with which the comparator can make a decision and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage. It also can reduce the input referred latch offset voltage

III. OPERATION

The double tail comparator design is based on the double tail architecture. The idea of this comparator is to increase $\Delta Vf_n/f_p$ in order to increase the latch regeneration speed. To achieve this constraint, the two control transistors M_{C1} and M_{C2} are added to the first stage in parallel to (M_3-M_4) transistors however in a cross-coupled manner.

The operation of the modified double tail comparator is as follows. During reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (i.e. when CLOCK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 are switched off. Likewise, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about power supply voltage V_{DD}). Thus, f_n and f_p start to drop with not the same rates according to the input voltages. Suppose $V_{inP} > V_{inN}$, thus f_n drops faster than f_p, (since M_2 provides more current than M_1). As long as f_n continues decreasing, the corresponding PMOS control transistor (M_{C1} in this case) starts to switch on, pulling f_p node back to the power supply voltage V_{DD}; so another control transistor (M_{C2}) switches off, allowing f_n to be discharged completely.

In other words, unlike conventional double-tail dynamic comparator, in which $\Delta Vf_n/f_p$ is just a function of input transistor transconductance and input voltage difference, in the existing double tail structure as soon as the comparator detects that for instance node f_n discharges faster, a PMOS transistor (M_{C1}) turns on, pulling the other node f_p back to the V_{DD}. Therefore by the time passing, the difference between f_n and f_p ($\Delta Vf_n/f_p$) increases in an exponential manner, leading to the reduction of latch regeneration time.

IV. SIMULATION RESULTS

The proposed double tail comparator circuit has been verified and simulated using the spectre simulator from cadence. The cadence virtuoso in an 180nm CMOS process parameter is utilized in this design. The transient analysis behavior of the double tail comparator is demonstrated in Figure 2.

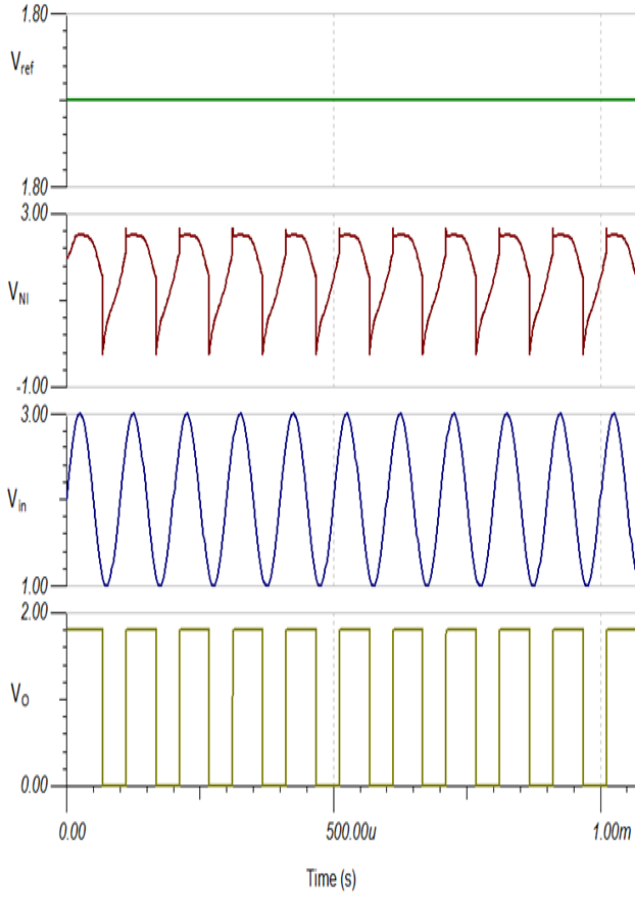

Figure 2. Transient analysis of the comparator

Table 1 shows the summary of the designed double tail comparator circuit.

Table 1. Summary of the double tail comparator circuit

Clock frequency	100MHz
Power supply	1.8V
Offset voltage	2.5mV
Technology	180nm CMOS
Propagation delay	600µs
Input Signal Frequency	upto 1GHz
Power dissipation	366µW

The total magnitude and phase response of the proposed double tail comparator circuit is shown in figure 3.

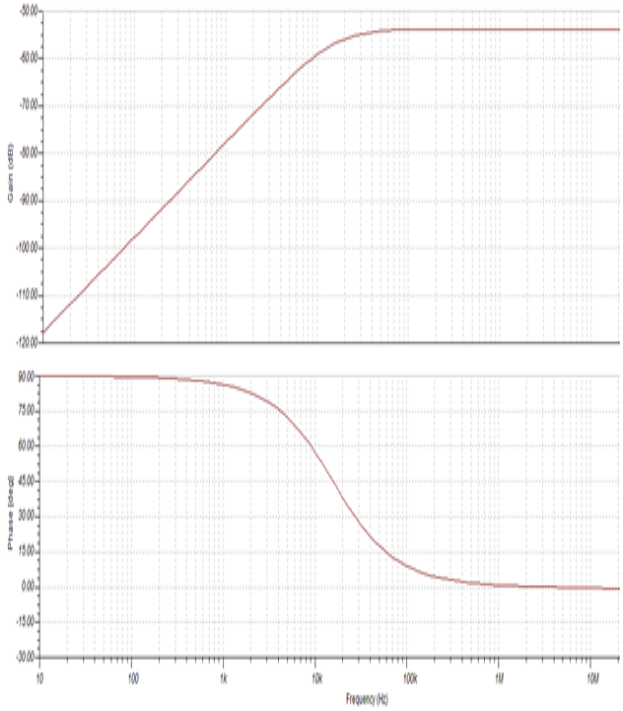

Figure 3. Magnitude and Phase response analysis of the comparator

The total output noise response of the proposed double tail comparator circuit is shown in figure 4.

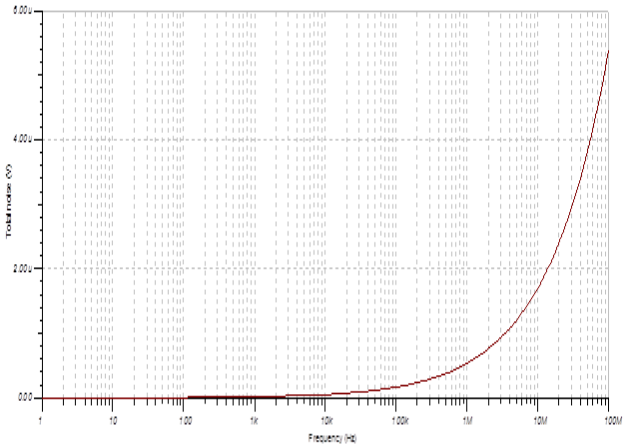

Figure 4. Total output noise response analysis of the comparator

V. CONCLUSION

In this work, a high speed CMOS double tail comparator circuit architecture for flash type ADC or pipelined ADC is designed and implemented. High speed and low power are very important parameters that need to be considered in the design of double tail comparator circuit. For reducing the power dissipation in the circuit, the transistors present in the input differential section of the comparator are operated in sub-threshold region rather than in the saturation region. The double tail comparator is designed and simulated using cadence-spectre in 180nm CMOS technology. Simulation results show that the designed double tail comparator circuit can work under as high clock frequency as 100MHz and its maximum offset voltage is about 2.5mV. The circuit exhibits a propagation delay of 600µs when operated at a power supply of 1.8V.

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