© 2016 IJSRST | Volume 2 | Issue 2 | Print ISSN: 2395-6011 | Online ISSN: 2395-602X
Themed Section: Science and Technology

Performance Analysis of CMOS Circuit by Using Sub Clock Power Gating Method

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ABSTRACT

Reducing the power consumed by the device is the emerging trend now-a-days. The aim is to reduce the leakage current of the circuit by using the Sub Clocking technology. It is the process of switching the circuit by means of partially ON to reduce the power consumption. There are two modes of operation are implemented. Half Mode Operation (HMO), Full Mode Operation (FMO). These modes of operation are implemented in the two designing methods One is Design-I,In that pMOS and nMOS are connected at header side of the standard CMOS circuit. In Design-II pMOS and nMOS are connected at the footer side of the standard CMOS circuit. pMOS and nMOS transistor at the header and footer side are refer to be as a Sub Clock control unit. Any one of the transistor is ON for a half mode operation and both the transistor are turn ON for full mode of operation. This will do by using the control signal to the sub clock unit which is placed in either header side or footer side of the CMOS gate. By this process the power consumed by the gate is reduced and also reduce the power leakage during the ideal mode of the gate.

Keywords: Corresponding MOS, Dual Mode Logic (DML), Static Power, Dynamic Power

I. INTRODUCTION

Sub clocking affects design architecture more than clock gating. It increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option.

An externally switched power supply is a very basic form of sub clocking to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal sub clocking is more suitable. CMOS switches that provide power to the circuitry are controlled by sub clocking controllers. Outputs of the power gated block discharge slowly.

Hence output voltage levels spend more time in threshold voltage level. Sub clocking uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

II. METHODS AND MATERIAL

1. Basic DML Architecture

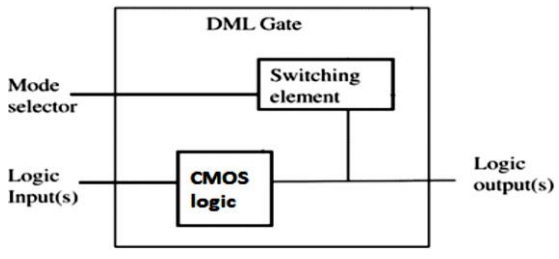

Figure 1: Basic DML Architecture

A novel low-power dual mode logic (DML) family, designed to operate in the sub threshold region. The proposed logic family can be switched between static and dynamic modes of operation with first approach using pMOS and nMOS as shown in the Figure 2. (a) and second approach as shown in Figure 2. (b) according to system requirements.

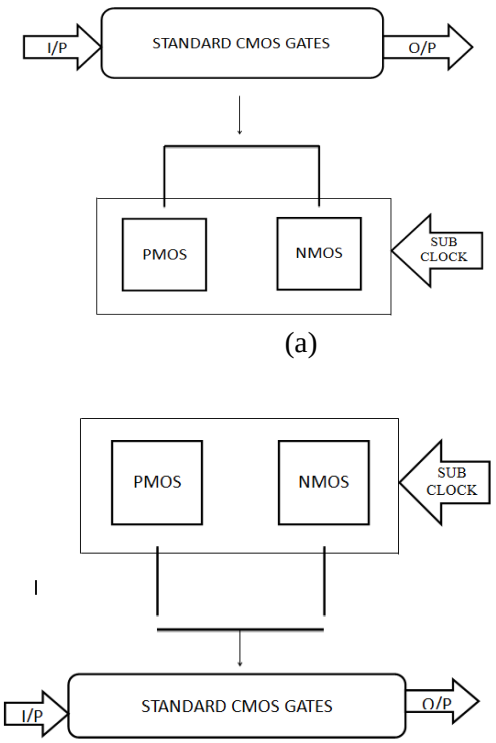

Figure 2: DML Gate Structure

In static mode, the DML gates feature very low-power dissipation with moderate performance, while in dynamic mode they achieve higher performance, albeit with increased power dissipation. Compare performance, power dissipation, and robustness of the proposed DML gates.

The basic DML gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal. At first glance, this architecture is very similar to the noise tolerant precharge (NTP) structure. However, in contrast to the NTP, which was developed as a high-speed, high-noise-tolerance dynamic logic, the DML aims to allow operation in two functional modes, static mode and dynamic mode. To operate the gate in the dynamic mode, the Clk is assigned an asymmetric clock, allowing two distinct phases precharge and evaluation.

2. Design of DML AND, OR & EXOR gates

The basic logic gates AND, OR & EXOR are implemented using Dual Mode Logic using CADENCE EDA tool. The schematic is simulated for Design I and II in static & dynamic modes and power is analyzed. In the DML Design I Static AND topology, the switching element is a PMOS and nMOS transistor as shown in the figure. 3 connected parallel to the Pull-up network. The input to the switching factor is a constant high voltage to make it OFF.

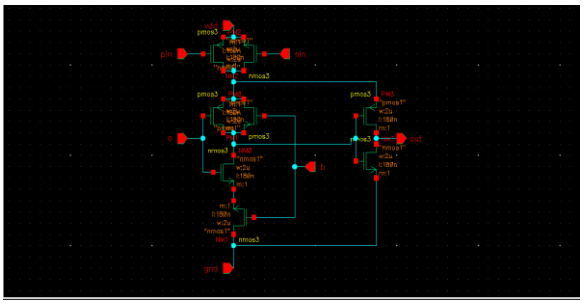

Figure 3: Schematic of Design-I Static AND

The only difference when designing DML Design-I Dynamic AND topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. Conventional OR logic gate design is done using CADENCE EDA tool and its power and performance are found. Also Dual Mode Logic AND gate Design-I and Design-II topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. In the DML Design-I Static OR topology, the switching element is a PMOS transistor connected parallel to the Pull-up network which is a series connection of 2 PMOS transistors. The input to the switching factor is a constant high voltage to make it OFF.

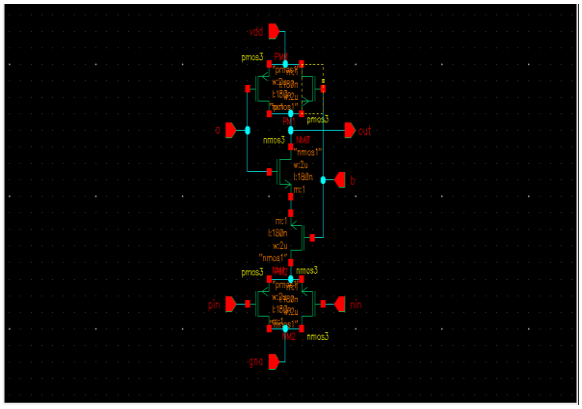

Figure 4: Schematic of Design-II Dynamic AND

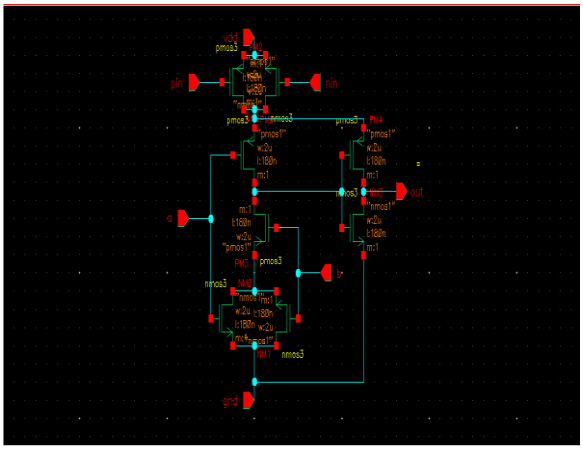

Figure5: Schematic of design I static OR

The input to the switching element is a stable low voltage to make it OFF. The only difference when designing DML Design-II Dynamic OR topology is that the input to the switching element is a clock signal having pre-charge and estimate phase for dynamic mode. Conventional inverter gate design is done using CADENCE EDA tool and its power and performance are found. Also Dual Mode Logic EXOR gate Design-I and Design-II topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. In the DML Design-I Static EXOR topology, the switching factor is a PMOS and NMOS transistor as shown in the figure. 4 connected parallel to the Pull-up network. The input to the switching element is a constant high voltage to make it OFF.

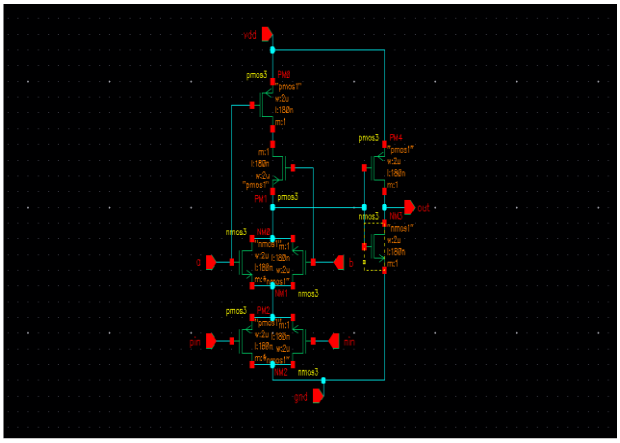

Figure 6: Schematic of Design-II dynamic OR

The only difference when designing DML Design-I Dynamic EXOR topology is that the input to the switching factor is a clock signal having pre-charge and estimate phase for dynamic mode.

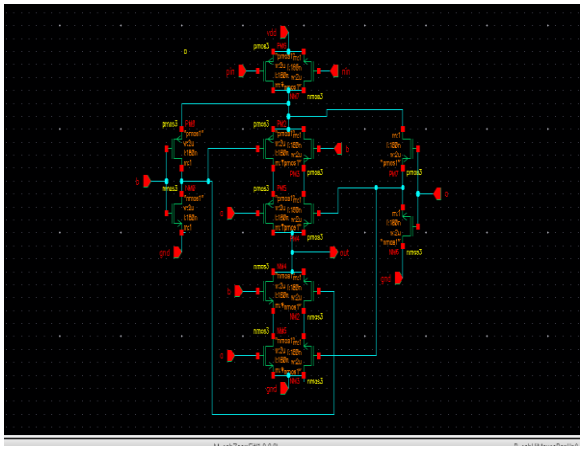

Figure 7: Schematic of Design-I Static EXOR

In the DML Design-II Static EXOR topology, the switching factor is an NMOS transistor connected parallel to the Pull-down network. The input to the switching factor is a constant low voltage to make it OFF. The only variation when designing DML Design-II Dynamic EXOR topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode. The total power consumption in micro watts and mile watts for AND, OR & EXOR logic gates Design-I and II is tabulated below.

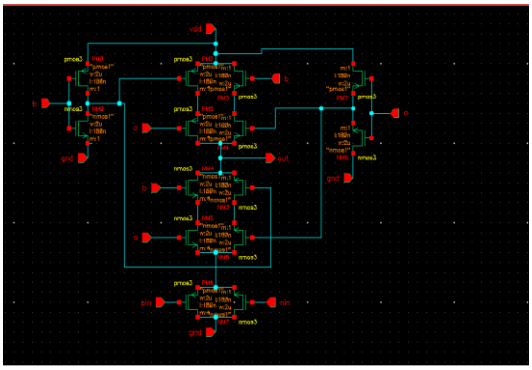

Figure 8: Schematic of Design-II Dynamic EXOR

Table 1: Comparison of AND, OR & EXOR gates

Gates	Design-I				Design-II			
	Both transistor OFF	pMOS ON	nMOS ON	Both transistor ON	Both transistor OFF	pMOS ON	nMOS ON	Both transistor ON
AND	0.299 µw	111.2 µw	20.04 µw	111.32 µw	0.379 µw	14.18 µw	143.7 µw	145.7 µw
OR	0.0203 µw	76.72 µw	18.65 µw	76.72 µw	0.388 µw	13.76 µw	97.12 µw	96.99 µw
EXOR	0.97 5mv	1.33 mv	0.953m v	1.332 mv	0.176 µw	12.29 µw	130.8 µw	130.8 µw

III. CONCLUSION

Power consumed by the gate by using the DML logic will be in the range of a milli watts and higher range of micro watts. Since the logic uses a pMOS and nMOS transistor at the output of the CMOS gate. The switching of the pMOS and nMOS gate is done using the High frequency pulse or directly connected to the operating voltage VDD. The Sub Clocking technique that reduces a power, consumed by the device during the Active mode and also in Ideal mode using the Design-I and Design-II technique. It uses a pair of pMOS and nMOS transistor in header side or in a footer side of the gate. Design-I approach use to reduce the power consumption by means of voltage dividing process and design-II approach used to reduce the leakage current during the high speed switching. Power consumed by the device is reduced upto 10% for a single gate(4 transistors) when implementing the design-I technique and also reduce the power up to 10^-1(1 watts) by implementing the design-II technique. Thus it can be implemented in any kind of logical circuit that can work in full power mode and also in half power mode. Compare to the DML logic the sub clocking method of design reduce the power consumed by a gates up to 10%.

IV. REFERENCES

[1] Asaf Kaizerman, Sagi Fisher and alexander Fish (2013), 'Subthreshold Dual Mode Logic' IEEE Transactions on Very large scale integration system vol..21 NO.5,pp. 979-983.

[2] Alioto. M (2012), 'Ultralow power VLSI circuit design demystified and explained: A tutorial' IEEE Trans. Circuits Syst. I, vol. 59, No. 1, pp. 3–29.

[3] Bol. D, Ambroise. R, Flandre. D, and Legat. J.D (2008) 'Analysis and minimization of practical energy in 45 nm subthreshold logic circuits' in Proc. IEEE Int. Conf. Comput. Design, pp.294–300.

[4] Calhoun. B. H, Wang. A, and Chandrakasan. A (2005), 'Modeling and sizing for minimum energy operation in subthreshold circuits' IEEE J. Solid-State Circuits, vol. 40, No. 9, pp. 1778–1786.

[5] Chang. M.H, Hsieh. C.Y, Chen. M.W, and Hwang (2015) W, 'Logical effort models with voltage and temperature extensions in super-/near-/sub-threshold regions' in Proc. VLSI Design, Autom. Test (VLSI-DAT), Int.Symp. pp. 1–4.

[6] Kwong. J and Chandrakasan. A.P (2006) 'Variation-driven device sizing for minimum energy sub-threshold circuits'Int. Symp. Low PowerElectron. Design, pp. 8–13.

[7] Levi, Kaizerman. A, and Fish. A (2012), 'Low voltage dual mode logic: Model analysis and parameter extraction'Excepted Elsevier, Micro electron J.,vol. 12, No. 9, pp. 1778–1786.

[8] Liu. X, Zheng. Y, Phyu. M.W, Endru F.W, Navaneethan. V, and Zhao. B (2012), 'An ultra-low power ECG acquisition and monitoring ASIC system for WBAN applications' IEEE J. Emerging Sel. Topics Circuits Syst., vol. 2, No. 1, pp. 60–70.

[9] Markovic.D, Wang. C.C, Alarcon. L.P, and RabaeyJ.M (2010) 'Ultralow power design in near-threshold region' Proc. IEEE, vol. 98, No. 2, pp. 237–252.

[10] Morgenshtein. E.G, Friedman, Ginosar. R, and Kolodny. A (2010), 'Unified logical effort-a method for delay evaluation and minimization in logic paths with interconnect' IEEE Trans. Very Large Scale Integr. (VLSI)Syst., vol. 18, No. 5, pp. 689–696.

[11] Pu. Y, de Gyvez. J.P, Corporaal. H (2009) 'An ultralowenergy/ frame multi-standard JPEG co-processor in 65 nm CMOS with sub/near-threshold power supply,' in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 146–147.

[12] Razak. H (2008)High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow. Cambridge, U.K.: Cambridge Univ.