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Design and Benchmarking of Gigabit Transceiver Protocol for 45nm based FPGA

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ABSTRACT

This paper gives the design of link where the parallel digital data are transmitted serially at the rate of 2.5Gbps on the Spartan 6 evaluation board. The implemented design is to test Gigabit Transceiver Protocol in order to transfer 16-bit parallel data serially over the SMA cable in full duplex mode. The 16-bit Parallel data are transmitted and received by the Serialized/De-serialized (SERDES) using Multi-Giga bit transceiver (MGT) at the clock rate of 125MHz.Gigabit Transceiver Protocol converts the parallel data to serial and serial to parallel. The proposed design is simulated in Xilinx 14.7 and implemented on Spartan 6 FPGA. The serial data are transmitted at the rate of 2.5Gbps over the SMA Cable link.

Keywords: Gigabit Transceiver Protocol, Multi-Giga bit transceiver (MGT), Phase-locked Loop (PLL), ChipScope Pro Analyzer.

I. INTRODUCTION

The field signal from any test facility gives the 16-bit parallel digital signals. The digital data are transmitted serially through SMA Cable and converted serial to parallel at the end of the receiver side. So, Number of the SMA Cable link can be reduced to transfer each field signals by using wave division multiplexing and reconstructed 16-bit parallel digital signals at the receiver side.

The paper gives the solution to encode the parallel data into the serial form and also gives the solution for the PLL based clock and data recovery at the end of receiver side with the use of 8b/10b encoder.

A Multi-Giga bit transceiver (MGT) is an SERDES capable of operating at serial bit rates above 1 Gigabit/second. MGTs are used increasingly for data communications because they can run over longer distances, use fewer wires, and thus have lower costs than parallel interfaces with equivalent data throughput.

Chapter I. Introduction about the Paper, Chapter II. GTP Architecture, Chapter III. Simulation and Testing using ChipScope Pro, Chapter IV. Conclusion, and Chapter V. References.

II. GTP ARCHITECTURE

The GTP transceiver is a power-efficient transceiver for Spartan®-6 FPGAs. The GTP transceiver is tightly integrated and highly configurable with the programmable logic resources of the FPGA. It provides the following features to support a wide variety of applications:

- Current Mode Logic (CML) serial drivers/buffers with configurable termination and voltage swing.

- Programmable TX pre-emphasis, linear continuous-time RX equalization
- Optional built-in PCS features, such as 8B/10B encoding, comma alignment, channel bonding, and clock correction
- Support for multiple industry standards with the following line rates:
  i. 0.614 Gb/s to 0.810 Gb/s
  ii. 1.22 Gb/s to 1.62 Gb/s
  iii. 2.45 Gb/ to 3.125 Gb/s

Their shown in Figure 1 is Simplified Spartan-6 FPGA GTP Transceiver Block Diagram. Here inside the block diagram PCS (physical coding sublayer) and PMA (physical medium attachment). Their PMA main Work Serial Data Transmit (Tx) and Parallel Data Receive (Rx), inside the PMA SIPO, Clock Divider, PISO and etc. As well PCS inside FIFO, PCIe, PRBS Generator, Frame Checker, 8B/10B, FPGA and etc.

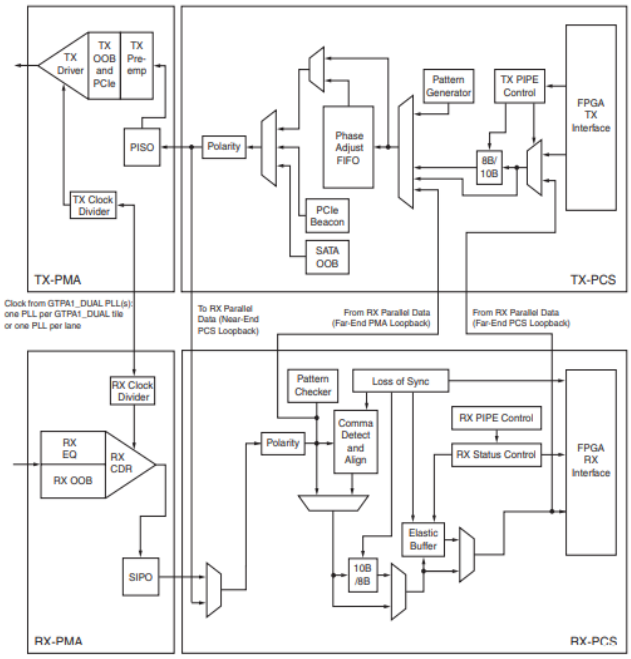

Figure 1. Simplified Spartan-6 FPGA GTP Transceiver Block Diagram[1]

GIGABIT TRANSCEIVER PROTOCOL

This LogiCORE IP GTP is lightweight, scalable, link layer protocol for high-speed serial communication. This protocol is very useful for low-cost, high-rate data channels applications. This IP core is open and can be implemented through the Xilinx environment. The user application interface of the protocol can be seen in figure

As per the specification, the protocol contains one more lanes. Each lane is full duplex serial data connection. That can transmit the serial data at the rate from 0.6 Gb/s to 2.5 Gb/s. With the help of channel partner, the user device can communicate together. Those channels are automatically initiated a channel when they are connected to a channel partner. After the initialization, the user application can transfer the data across the channel as a stream of the framing data structure.The GTP provides two type of transmission mode:

1. Full Duplex mode,
2. Simplex Mode (Tx- only simplex and Rx- only simplex)

The transmission mode for this design is full duplex mode. The protocol can be customized as per the design.

Lane width decides the number of bytes transmitted during the period of one clock cycle. This GTP supports PCI Express and 4 lane width.

If the selected lane width is 4 then the user clock (USRCLK) should be half of reference clock (REFCLK). The multi-Giga bit transceiver is configured using GTP that converts each byte of data i.e. 2 byte of data into 20 bits (each byte i.e. 8 bits into 10 bits). Here GT REFCLk is 125 MHz, which is generated through PLL. So the Line rate will be 125 MHz * 20 (bits) equal to 2.5 Gb/s. At this data rate, the serial data are transmitted over the SMA channel.

MULTI-GIGA BIT TRANCEIVER

Multi-Gigabit-transceiver/Multi-Gigabit-serialize/De-serializer receives parallel data and allows transportation of high-speed data over the serial link design, Spartan 6 have provided 4 MGTs to access. From that four MGTs one MGT is used, the one for MGT SMA Connectors, which are used in this designs.

In serializer, the encoder will modify the parallel data & adds some overhead bit. It helps in synchronization and channel transmission in serial. Also, it used to achieving DC balancing, error detection, and clock recovery. In 8B/10B encoding scheme, 8-bit input data is serialized at 10x serial clock. PLL is used to generate serial clock (10x) from the parallel clock. And that serial data transmitted over the differential channel, where at receiver side Deserializer word synchronizer finds word packet boundaries from serial data. The main function of Deserializer is clock and data recovery (CDR). It receives serial data and extracts the synchronized clock either from data itself or generates the synchronized serial clock from reference parallel rate clock. For that phase lock loop is required for both options.

In PLL based clock and data recovery, a phase-frequency detector generates two output signals which are UP and DOWN signals and depends on the phase difference between the input data and the generated clock. A phase difference will be detected as a phase difference and the PDF will generate steady UP-DOWN signal. Now this signals cause the charge pump (CP) to output or source a current, which is converted into the voltage and filtered by the loop filter. This voltage controls the output frequency of VCO. This voltage controlled oscillator output is recovered clock; it will feed back to the phase frequency detector. This PLL's negative feedback faces phase & frequency of the recovered clock to be same as the phase, bit rate, and clock condition. This PLL is Shown in Figure 2.

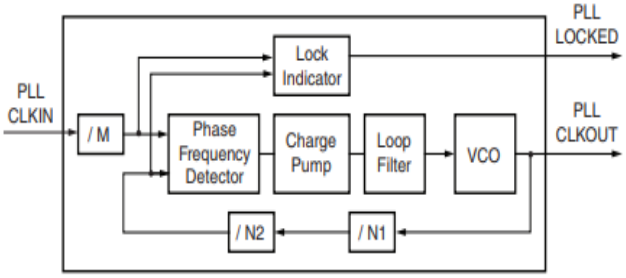

Figure 2. PLL Detail (Phase-lock Loop)[1]

GTP transceiver is a power efficient transmitter-receiver for Spartan 6 FPGA. In the physical implementation of MGTs; it takes the form of differential based electrical interface. There are three differential methods such as:

1. Current Mode logic (CML),
2. Low voltage differential signaling (LVDS) &
3. Low voltage Pseudo emitter coupled logic (LVPECL).

CML is most common and preferable for the Giga-bit link for AC or DC termination and selectable output drive. GTP provides programmable Tx_pre emphasis, linear continuous time Rx equalization. The GTP transceiver has the line rate of 3.125 Gb/s, which is implemented tested for the SMA link of 2.5 Gb/s line rate.

GTP MODULE INTERFACE

The Gigabit Transceiver Protocol (GTP) is compact and hot-pluggable transceiver used for both telecommunication also for data communication.

A. Software and Hardware Resources:

1. Xilinx ISE 14.7 tool.
2. Xilinx Core Generator.
3. Xilinx LogiCORE IP GTP Tranceiver wizard core.
4. Xilinx Spartan 6 (SP605) hardware development board.
5. SMA cable.
6. GTP transceivers in ChipScope Pro Analyzer.

III. SIMULATION AND TESTING USING CHIPSCOPE PRO

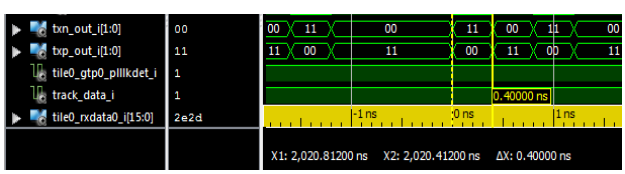

Figure 3. GTP Transceiver Line Rate 2.5Gbps

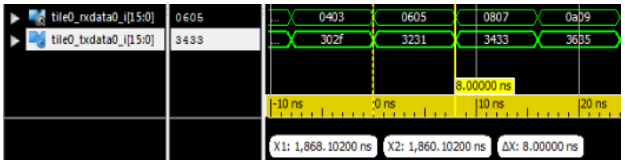

Figure 4: GTP Transmit Data at 1860.10200 ns

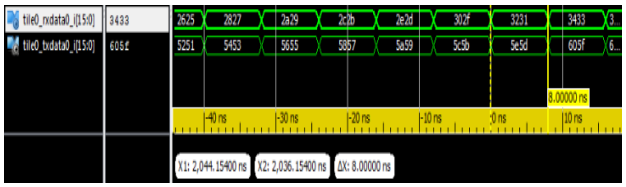

Figure 5. GTP Receive Data at 2036.15400 ns

Here, Difference between receive and transmit data through find a latency. In GTP Transmit Data and Receive Data difference latency equal to 176.052ns.

Listing - DEV:1 MyDevice1 (XC6SLX45T) UNIT:0 MyILA0 (ILA)

<->	Sample	GTP_TX_DATA	GTP_RX_DATA
	815	7877	4847
	816	7A79	4A49
O	817	7C7B	4C4B
	818	7E7D	4E4D
	819	0100	504F
	820	02BC	5251
	821	0403	5453
	822	0605	5655
	823	0807	5857
	824	0A09	5A59
	825	0C0B	5C5B
	826	0E0D	5E5D
	827	100F	605F
	828	1211	6261
	829	1413	6463
	830	1615	6665
	831	1817	6867
	832	1A19	6A69
	833	1C1B	6C6B
	834	1E1D	6E6D
	835	201F	706F
	836	2221	7271
	837	2423	7473
	838	2625	7675
	839	2827	7877
	840	2A29	7A79
X	841	2C2B	7C7B
	842	2E2D	7E7D
	843	302F	0100
	844	3231	02BC

Figure 6. Listing table of GTP Transmit and Receive Data

The testing results give the transmitted and received bit pattern on the input data. The transmitted input sequence can be seen at the end of the listing table in chipscope pro analyzer tool [6] (Figure 6). Figure 7 shows waveform of the GTP_TX_DATA sequence and GTP_RX_DATA the received signal.

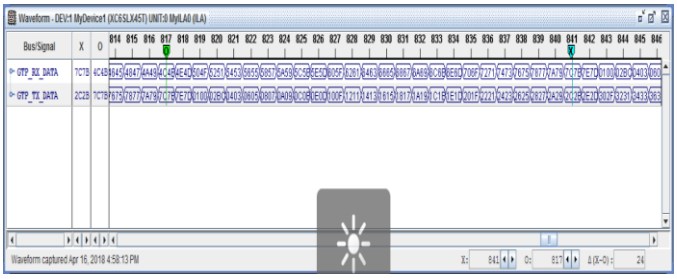

Figure 7. Waveform of GTP Transmit and Receive Data

Figure 8 shows the Hardware implementation as shown them. To Spartan-6 FPGA Board (sp605) is 45nm technology using High-speed Data transfer.

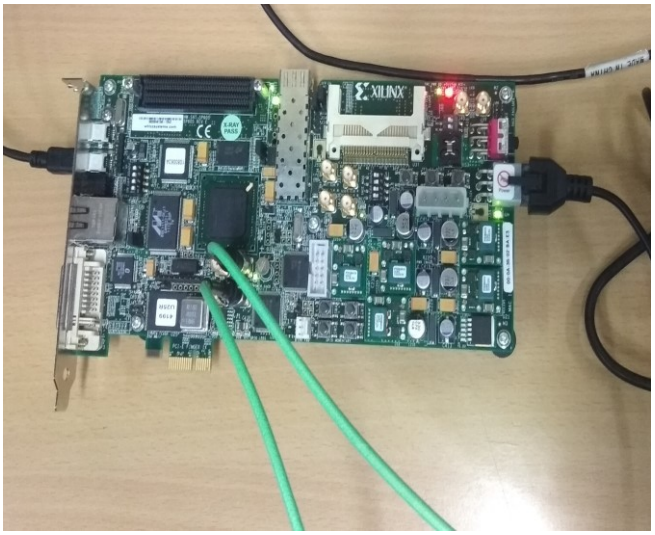

Figure 8. Implementation GTP Transceiver on Board

IV. CONCLUSION

The implemented design gives the perfect and proper description to transfer the high-speed serial data over the higher bandwidth serial cable. The design is giving the results for Gigabit Transceiver protocol in full duplex mode. The design proposed to make a simplex transmitter and receiver link on the individual Spartan 6 board. The transmitted signal marked as X cursor at sample 24 and the input sequence can be seen at sample 0 marked by O cursor from their onwards input sequence can receive at the receiver side.

V. ACKNOWLEDGMENT

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VI. REFERENCES

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