

# Full-Bridge Power DC-DC transformation by MOSFET Switching Techniques

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## ABSTRACT

This paper presents a collection of novel soft-switching techniques to extend the ability conversion potency in PV cell (PVC) systems employing a full-bridge topology. For this causes, a special right-arranged modulation sequence is developed to attenuate conductivity losses whereas maintaining soft-switching characteristics within the MOSFETs. Ancient auxiliary parts within the primary, like series inductors that square measure impractical for realizing because of the intense input current, square measure avoided and mirrored to the output response of the converter to attenuate current and generate soft transitions within the output diodes are replaced by MOSFET. By that result, the projected techniques with success scale back conductivity losses, minimize reverse-recovery losses within the output rectifiers, minimize transformer ringing, and guarantee low stress altogether the switches. The high potency is maintained within the entire vary of loading conditions, whereas taking into thought exceptional challenges related to PVC power conversion: input current, low voltage and poor regulation, and big selection of loading conditions. A close techniques for potency gains square measure bestowed and A phase-shift zero-voltage shift topology is used as a reference topology to focus on the mechanisms for performance improvement and therefore the blessings within the use of the special modulation. Experimental results of a power convertor square measure bestowed to validate the potency gains, illustrate the advantages of the special modulation, and demonstrate the soft-switching transitions.

**Keywords :** Photo-Voltaic Cell (PVC), Soft Switching, More Efficient, System Modulation, Losses.

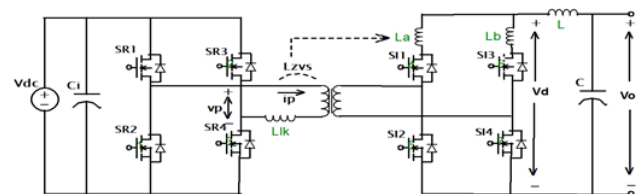
## I. INTRODUCTION

Photo-voltaic cell (PVC) are power sources that convert solar power into voltage with high potency. Several approaches to understand dc-dc isolated power conversion for PV-cell power sources are planned supported full-bridge, push-pull, and current-fed topologies. A number of the key contributions within the space embody the study made public within the following. A PV-cell power convertor supported a controlled voltage device was introduced, that uses phase-shift modulation to manages the facility flow through the electrical device leak inductance. This fascinating topology established to be less economical than alternative ancient topologies, however presents the advantage of low part count. A PV-cell {inverter\electrical convertor} supported a conventional push-pull dc-

dc converter was given that includes low value, low part count. Based upon push-pull topology, a standard design was given to boost measurability and dependability. Associate degree category of the push-pull circuit has been reported as a part of a grid-connected electrical converter system. The same current fed push-pull topology was utilized in a very step up resonant convertor, presenting a high voltage-conversion magnitude relation. A bridge forward dc-dc convertor with bridge rectifier was given. this can be a really strong topology once operated with zero-voltage shift (ZVS) technique associate degree represents an trade customary in several applications, like telecommunication power provides (highin-place voltage). A three-phase version of the full-bridge forward convertor was recently planned, supported  $\Delta$ -Y electrical device association and a clamp circuit to cut back the leak

inductance and current currents. a brand new family of phase-shift ZVS with reconciling energy storage was conjointly planned to extend soft- shift in operation vary victimisation auxiliary circuits . As well, topologies supported current fed to bridge topology were planned that includes low input ripple current and reduced stress within the input aspect switches, whereas conjointly together with active clamping circuits, and interleaved electrical device windings to attenuate losses and leak inductance so as to extend power conversion capability and supply increased characteristics, current-fed was also used in resonant ,two- inductors boost ,and three-phase converters . Alternative topologies, like input-current electronic device associate degreed an output-voltage electronic device were combined to supply high voltage-conversion magnitude relation. As well, novel half-bridge topologies were planned to supply soft-switching characteristics. Finally, a three- port triple-half-bridge two-way dc-dc convertor topology was planned, that employs a high-frequency three-winding electrical device , and therefore the full-bridge counterpart with 2 series resonant tanks was enquired. Successful power acquisition for PV systems needs deal- ing with poor voltage regulation, high input current, and a good vary of output loading conditions whereas maintaining high potency and low change stress. once exposed to those stringent necessities, full-bridge zvs, push-pull, and current fed topologies are confronted with many technical challenges. for instance, maintaining zvs (full-bridge) is easy because of the voltage regulation of the pv-cell and therefore the big selection of loading conditions, that creates excessive conductivity losses because of current within the primary. the push-pull topology reduces electrical device utilization (primary center tap), compromises magnetizing balance because the power rating will increase (winding spatiality and excitation imbalance), also the probabilities for soft-switching operation. Current fed based topologies

want large input inductors (high current), oscillations created by the interaction between parasitics (leakage inductance, intrawinding capacitance, and therefore the input inductor), and will gift excessive degrading high-frequency ripple current within the output capacitors because of filter electrical device. whereas the trend for high-input-voltage converters (e.g., connected to the line) has been to reduce change losses and manage comparatively tiny line regulation, in contrast to applications with high input voltage achieving zvs with low voltage doesn't result insubstantial potency gains, given the little energy hold on within the MOSFETs output capacitance the facility dissipated during a MOSFET because of the output capacitance throughout activate may be a perform of the sq. of the PV voltage pv a pair of . Since pv-cell are power sources,the relative importance of change losses will be outweighed by conductivity losses within the MOSFETs that are a perform of unagency a pair by taking into thought the same technical challenges, it becomes crucial to handle the subsequent relevant points in pv cell power conversion: 1) want for reduction in conduction losses, and thus, unneeded current within the primary; 2) minimize substantial reverse-recovery losses within the output rectifiers (due to the high output voltage); 3) minimize the associated electrical device oscillations (ringing); and 4) make sure that the high potency, by combining points maintained wide input voltage vary and 0%–100% loading conditions.



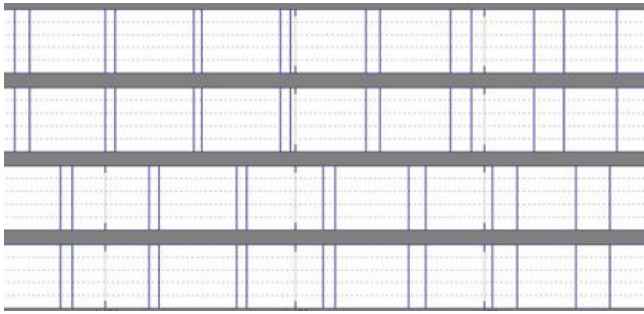


Fig. 1. Schematic circuit waveforms with Lzvs reflection to the output of the device right-aligned gate signals within the upper switches and duty cycle within the lower switches

In paper, this addresses the challenges by proposing a group of soft-switching techniques during a full-bridge forward topology. For this purpose, a special modulation sequence is developed to attenuate conductivity losses where as maintaining soft-switching characteristics within the MOSFETs and soft transitions within the out-place rectifiers. Auxiliary components within the primary, like series inductances & capacitors that square measure impractical to understand due the acute input current square measure avoided by reflective them to the secondary of the circuit to attenuate current and generate soft transitions within the switches. These variations square measure conceptually pictured in Fig. 1 indicating 3 major modifications suited to pv cell power conversion. Elaborate analysis of the techniques for potency gains is given and the phase-shift ZVS topology is used as a reference topology to spotlight the mechanisms for performance sweetening and therefore the benefits within the use of the special modulation. Experimental results of an influence convertor given to validate the potency gains, illustrate the advantages of the special modulation, and demonstrate the soft-switching transitions.

## II. OPERATIONAL TIME INTERVALS

Operational time intervals responses and loss-reduction responses the mix of the projected techniques, Lzvs inductance reflects to the output, aligned signals by gate for the higher switches ( a pair of ), and +51% duty cycle within the lower switches square measure investigated well during this section. shows the switch sequence for MOSFETs  $M1 =SR1$ ,  $M2 =SR2$ ,  $M3 =SR3$ , and  $M4 =SR4$  at the side of the most waveforms for the techniques below study. Transition intervals are exaggerated for clarity. The structures non inheritable by the facility device throughout the switch intervals square measure represented in Fig.2. The switch with in the sequence leads to twelve completely different intervals  $T1 -T12$ , that square measure wont to justify the behavior of the device. so as to look at varied efficiency-gain mechanisms, an in depth analysis of this and voltage wave shape is bestowed for the higher and lower MOSFETs, followed by the higher and further down output rectifiers.

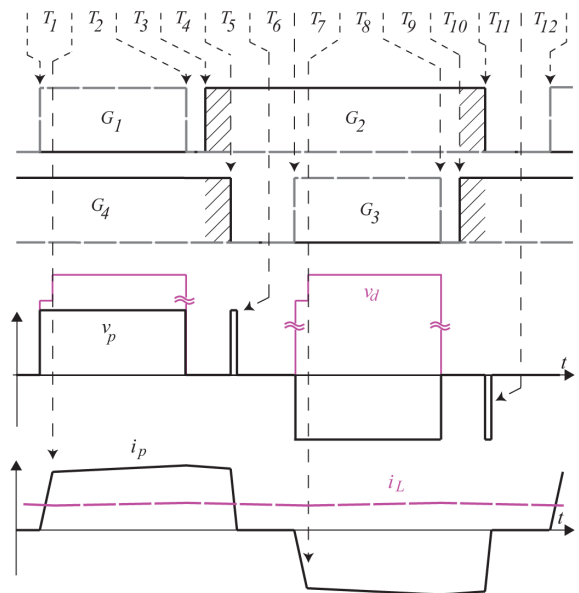


Fig. 2. MOSFETs  $M1$ , to  $M4$  switching intervals and voltages and current waveforms for.

### MOSFETs Waveforms

The waves for MOSFETs  $M_1$ ,  $M_4$  and their several body MOSFET  $M_5 = S_{11}$ ,  $M_2 = S_{12}$ ,  $M_3 = S_{13}$ , and  $M_4 = S_{14}$  throughout a full-cycle amount, as well as the gate signals  $tt_1$  and  $tt_4$ , drain-source voltages  $V_{M1}$  and  $V_{M4}$ , currents for the MOSFETs n-channel  $i_{M1}$  and  $i_{M4}$ , and therefore the body diodes  $i_{D1}$  and  $i_{D4}$ . The waveforms for  $M_2$ ,  $M_3$ ,  $D_2$ , and  $D_3$ , follow constant pattern for ensuing shift cycle.

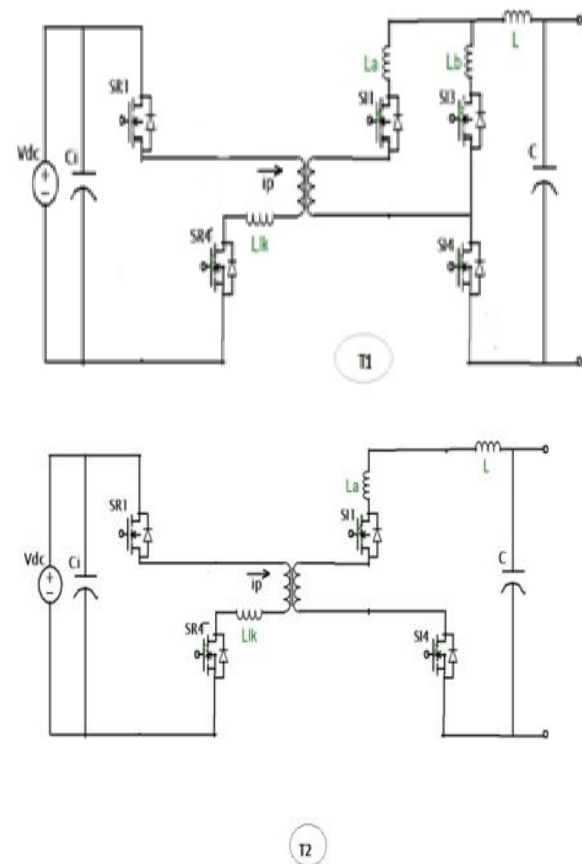
Interval at  $T_1$ : The right-aligned modulation, that ensures no current within the primary, starts with interval  $T_1$ . The higher MOSFET  $M_1$  supply activates with zero-current shift (ZCS), and therefore the current path is thru  $M_4$  that's already within the ON-state. a motivating impact within the primary current rate of  $di/dt$  will be known throughout the  $T_1$  interval, that is inherently restricted by the action of the inductors  $L_a$  and  $L_{lk}$  to the first, manufacturing a  $L_{zvs}$  like impact. Once the first current reaches this level of the filter inductance mirrored to the first  $i_L$ , interval  $T_1$  ends.

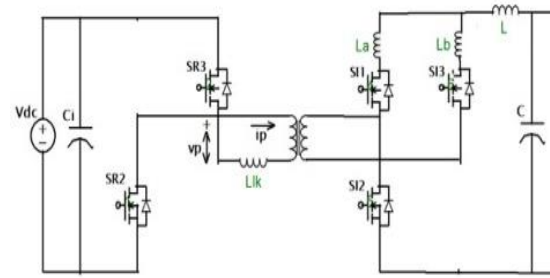
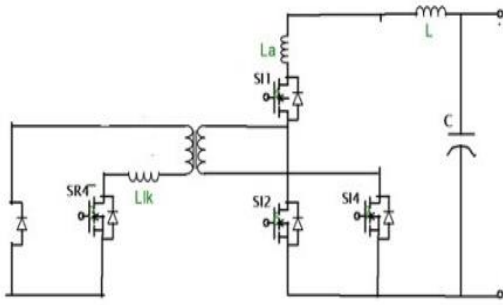
Interval at  $T_2$ : MOSFETs money supply and  $M_4$  area unit within the ON-state and their current still build with continue to ramp slope slope  $(V_i - V_o)/(L_{lk} + L_a + L)$ .

Interval at  $T_2$ : The  $T_2$  begins  $M_5$  reaches the present level of the filter electrical device inductor. MOSFET  $M_7$  recovers with a soft transitions because of the moderate  $di/dt$  and additionally experiences a reduced interference voltage within the low electrical device ringing, each serving to to cut back reverse-recovery losses. this may be explained because of the actual fact that the zero voltage condition within the secondary of the electrical device is eliminated with the inter-deed action of  $L_a$ ,  $L_b$ , so preventing associate abrupt voltage step within the electrical device secondary

that excites the parasitics that cause self-resonance (leakage inductance, capacitances, etc.). whereas ancient full-bridge ZVS needs a snubber to limit the ringing, the planned technique removes the snubber whereas reducing the losses within the higher diodes and MOSFETS.

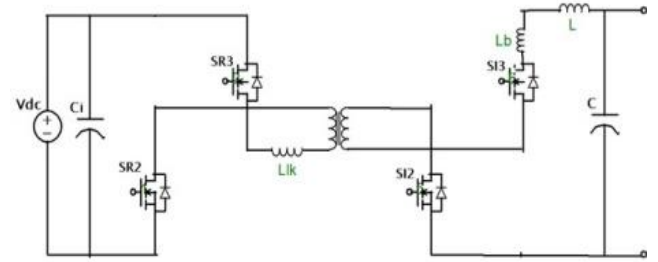
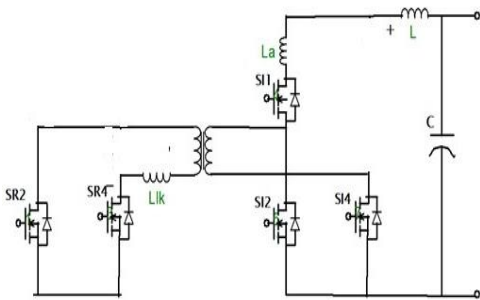
### III. INTERVALS $T_1 - T_2$





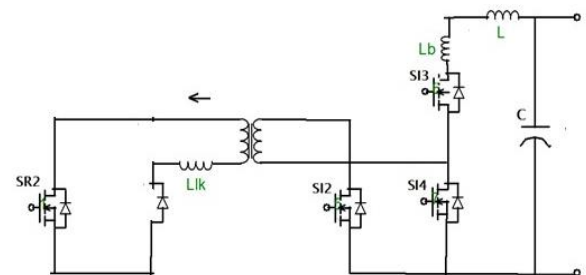
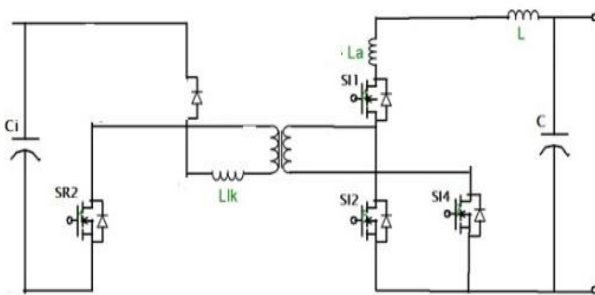
T3

T7



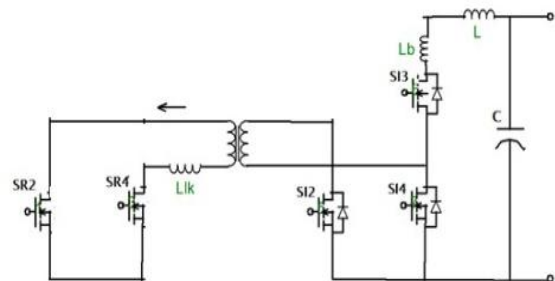
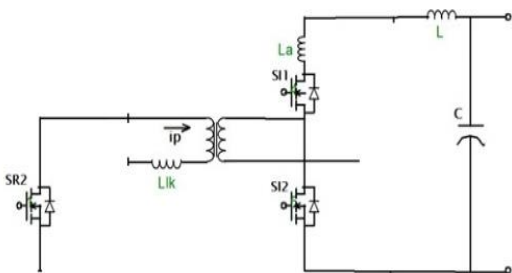
T4

T8



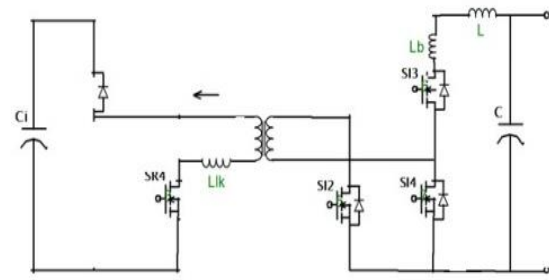
T5

T9

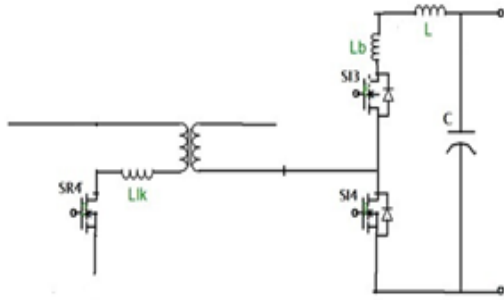


T6

T10



$T_{11}$



$T_{12}$

Fig.3. Intervals  $T_1 - T_{12}$

Here,  $V_o$ ,  $L_a$ , and  $L$  denote, respectively, the output voltage, auxiliary inductor, and output filter inductor reflected to the primary.

*Interval at  $T_3$*  : Begins once gate signal  $tt_1$  drops inflicting  $M_1$  to show off and  $D_2$  to start out conductivity. This interval may be a short time between  $M_1$  and  $M_2$ , and finishes once the gate signal  $tt_2$  increases. The behavior of  $M_2$  and  $D_2$  is that the same as  $M_4$  and  $D_4$  within the next cycle.

*Interval at  $T_4$* :  $M_2$  activates with ZVS, providing  $D_2$  was forward-biased throughout  $T_3$ . This interval is additionally temporary and ends once  $tt_4$  gate signal drops. The target of extending  $tt_4$  slightly on the far 51% to confirm ZVS on each lower switch.

*Interval at  $T_5$*  : The energy hold on within the run inductance  $L_{lk}$  is came back to dc bus capacitors by  $D_3$  body diode. Since the standard  $L_{zvs}$  has been mirrored to the secondary, the inductance within the primary  $L_{lk}$  is dramatically decreased by employing a flattened electrical device planar transformer. The transformer electrical device primary current  $i_p$  is, therefore, reset to zero throughout this short interval.

*Interval  $T_6$* : The current within the primary is deleted, translating into tangible potency gains gives the input current that's characteristic in pv cell power conversion. Here the remaining Time intervals  $T_7 - T_{12}$  repeats constant behavior for  $M_2$  and  $M_3$  and corresponding  $D_2$  and  $D_3$ .

*Interval at  $T_7$*  : Explains the conductivity of interval of  $M_7$ .

*Intervals at  $T_4 - T_5$*  : Explains the Initiatives and the recovery in  $M_8$ .

*Interval at  $T_6$*  : The recovery of  $M_8$  doesn't expertise reverse voltage because of the interleaving result of  $L_a$  and  $L_b$ . Therefore, The transition has less losses. This result results

in substantial potency gains within the lower diodes  $M_6$  and  $M_8$ . In summary, the waveforms. for the proposed soft-switching techniques reveals the subsequent improving change.

1) The inductors  $L_b$  and  $L_a$  form the present waveforms of  $M_5$  and  $M_7$  throughout reverse recovery. Therefore, the auxiliary inductance values will be elect to attain an impression the entire reverse- recovery power losses. 2) MOSFETs  $M_6$  and  $M_8$  expertise negligible reverse-recovery losses, not like the phase-shift ZVS topology, which is near-zero forward current once the decreased reverse voltage given. The presence of  $L_a$  and  $L_b$  decreases oscillations and therefore the peak reverse voltage applied to  $M_6$  and  $M_8$  those results from electrical device transformer. Transformer Oscillation ends up in undesirable impact, like high most back voltage grading for the diodes, over voltage between power losses and windings in snubber circuits. The conception of avoiding a zero-voltage condition on the electrical device transformer secondary is addressed by preventing synchronal conductivity of  $M_5$ ,  $M_6$ ,  $M_7$ , and  $M_8$ . As a result, the stimulant pulse is part mirrored to the secondary of the electrical device as if the device were operational in discontinuous conductivity mode. Hence, the oscillations were reduced below any loading condition. These combined enhancements increase the potency of the rectifier stage additionally to the potency gains of the MOSFETs. The behavior of the device highlights the benefits of the projected techniques in full-bridge topology for PV cell power conversion (low input voltage, terribly higher input current, combined with less current, higher output-voltage rectifier).

**TABLE I - PARAMETERS**

PARAMETER	VALUE/RANGE
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$V_{PV}$	10-30V
$V_O$	230V
$M_1 - M_8$	2*IRFB4110
L	1.33mH
$L_a, L_b$	10uH
C	680uF
$C_i$	4400uF
$F_{sw}$	40-100KHz
TRANSFORMER PRIMARY TURNS $N_p$	2(FOIL)
TRANSFORMER SECONDARY TURNS $N_s$	26(STRANDED)

A power-converter example was utilized to validate the waveforms of the planned soft-switching techniques and to approve efficiency potency gains. A briefing of resistive masses was utilized to perform the measurements. The convertor was designed the parameters and elements in Table I, and a phase-shift ZVS topology was utilized as a reference topology. By ZVS operation, the inductance  $L_{zvt}$  was enclosed and  $L_a$  and  $L_b$  were eliminated. On the opposite hand, the planned modifications were tested victimisation  $L_a$  and  $L_b$  and eliminating  $L_{zvt}$ . The sensible implementation of the convertor follows current trends by victimisation DSP management and modulation (TMS320F2808), specifically to modify the task of generating the modulation. As well, as a part of the necessities to comprehend the planned techniques, the drivers of the higher MOSFETs was organized to supply actual pulsewidth modulation, instead of the fixed 51% duty cycle utilized within the phase shift ZVS counterpart.

#### IV. Validation of the Result Waveforms

A complete cycle in  $M_1$ ,  $M_4$ ,  $M_7$ , and  $M_8$  was measured beneath medium loading condition to

validate the waveforms so as to facilitate the visualisation, the shift frequency, the waveforms of MOSFET money supply, together with gate and drain-to-source voltages, and also the secondary transformer electrical current. It is seen that the MOSFET current starts near zero (ZCS) at the start of T1 and slowly ramps up till it reaches this level of the output-filter inductance at the start of T2. The MOSFET turns off throughout T3, limiting the physical phenomenon interval to T1 -T2. The body diode D1 physical phenomenon interval is seen in T11 that returns the energy of the run inductance to the input dc bus and avoids current circulating within the primary. The tiny energy within the run leakages are absorbed and clamping by the input capacitors of the convertor. The lower MOSFET M4 waveforms shown at figure 2. wherever the zero-voltage transition throughout stimulation turning on is seen at the start of T11. Thereafter, at the start of T4, M4 turned off. As well, D4 includes a soft-switching transition throughout T5. The physical phenomenon interval in M4 similar to M1, showing reduced physical phenomenon losses. In order to gauge the convertor operation beneath phase-shift ZVS, the inductance  $L_{zvt}$  was enclosed and  $L_a$ ,  $L_b$  were removed. MOSFET M1 signals the secondary current is. It is seen that the stimulation transition happens throughout (T1) interval and also the physical phenomenon is extended till the top of (T6). As represented by the analysis of physical phenomenon losses, the physical phenomenon interval presents unnecessary current. MOSFET M4 (lower aspect switch) presents an analogous behavior with current.

#### V. SIMULATION DIAGRAM



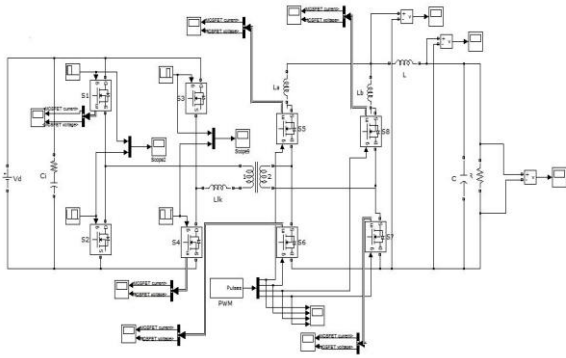


Fig.4 Simulation diagram

### 5.1 SIMULATION RESULTS

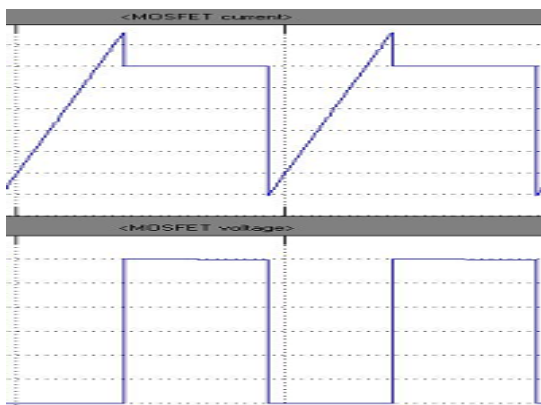


Fig.5. Lower aspect MOSFET M4 waveforms within

the projected changed topology below medium loading condition: drain source voltage (Ch1), signal (Ch2), and with transformer secondary current (Ch4).

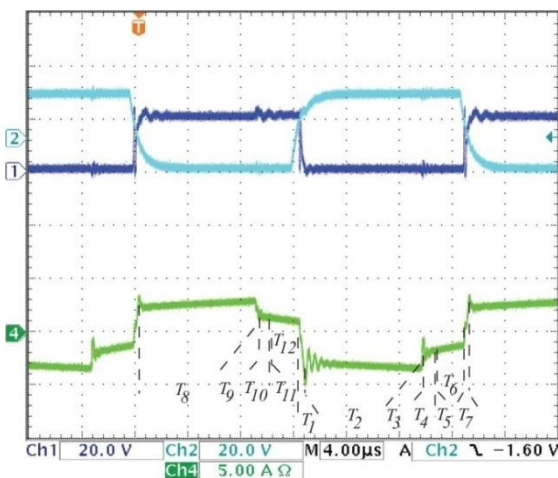


Fig 6.Upper side MOSFET M1 waveforms within the planned changed topology underneath medium loading condition: drain source voltage (Ch1), gate- to- supply signal (Ch2), and with transformer secondary side current (Ch4).

### 5.2 RESULT WITH OUT FILTER

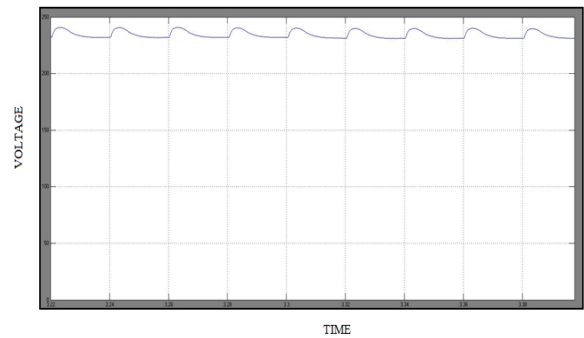


Fig.7. RESULT WITH OUT FILTER

### 5.3 RESULT WITH FILTER

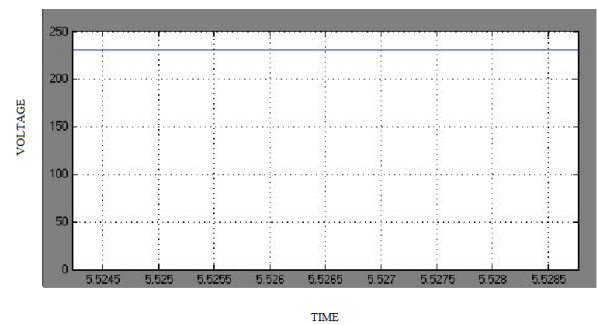


Fig 8. RESULT WITH OUT FILTER

## VI. Comparison Measurements of Efficiency

The combined switch and physical phenomenon losses for the projected soft-switching techniques

area unit bestowed during this section. By phase-shift ZVS is used as a referred topology for comparative analysis. Identical power devices, drivers, power transformer, dead time insertion, heat sink and fan, and output filter were used in each cases to make sure a good comparison (see Table I).. Note that the target of the experimental potency mensurations is Associate in the potency gains with the projected modifications instead of performing arts an absolute measurement of the convertor potency. The potency mensuration accounts for the power ability switches, computer circuit board, connections, and magnetic elements and doesn't embrace losses within the drivers & controllers. For ZVS operation, the auxiliary Lzvt inductance and snubber were enclosed, whereas removing La, Lb tests were performed for numerous input voltages VPV = 12, 25, and 30 beneath variable loading conditions (500w&ndash;1KW range) for each power converters. The results area unit shown in Fig. 9, The potency profile achieved with the projected soft-switching techniques, named as changed within the figure 9 is pictured with circle markers, whereas the phase-shift ZVS is explained with star markers. It is seen that the projected modifications gift a significantly gain under any in operation condition. For instance, Associate in potency gain of 3%&ndash;6% power convertor with associate in overall efficiency of 96% provides an improvement near 30% &ndash; 40% within the thermal management of the ability stage and permits the utilization of lower value heat sinks/ power semiconductors/ . This could be thought- about considered. As a superb improvement toward power density and price of the ability Conversion stage, whereas maintaining the simplicity of a full-bridge circuit. As well, the potency gains lead to additive savings beneath any operational condition (light, medium, and heavy) by using the planned soft-switching techniques.

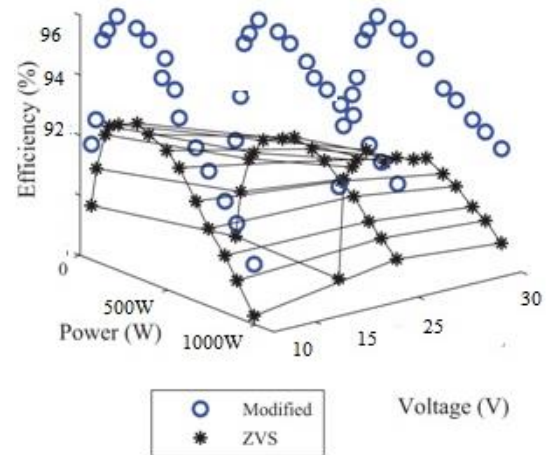


Fig 9. Comparison Measurements of Efficiency phase-shift ZVS (ZVS).

## VII. CONCLUSION

A set of soft-switching techniques for the full-bridge topology were explored during this study as well as the reflection of the normal Lzvs inductor electrical device to the output response of the rectifier, right-aligned modulation for the higher switches, and +51% duty cycle within the lower switches. The study bestowed during this paper known the most power-loss mechanism in full-bridge pv cell power conversion within the presence of a low voltage regulation of pv cell and also the big selection of loading conditions. The combined techniques with success self-addressed the foremost vital power loss effects and issues in pv cell power conversion:

- reduction in unnecessary high current within the primary, and thus, conductivity losses;
- elimination of sensible impractical high-current inductors within the primary;
- reduction of reverse-recovery losses within the output rectifiers;
- minimisation of electrical device oscillations (ringing); and
- improved potency underneath the pv cell wide

input voltage vary and 0%–100% loading conditions.

As anticipated by the analysis, taking put in a favourable the opportunities for performance enhancements, consider- in a position potency gains were through an experiment ascertained within the entire vary of operation of the system whereas Maintaining the simple and rugged of the full-bridge topology. As can be seen, unlike resonant converters, the techniques prevent unnecessary circulating current in the and through the MOSFETs, and this allows power transfer during the conduction interval. As may be seen, not like phase-shift or resonant converter, the proposed planned techniques stops unnecessary current within the electrical transformer and thru the MOSFETs, and permits power transfer throughout the conductivity interval. This is often a key demand in low-tension, high-current applications, wherever the conductivity losses are unit substantial and prevail over switching losses at moderate frequencies. As well, the +51% duty-cycle modulating sequence ensures zero-voltage transitions in MOSFETs M2 and M4. The gains delineate during this section are further increased within the output rectifier as delineate within the following section. The study given during this paper known the most power-loss mechanism in full-bridge pv cell power conversion within the poor voltage regulation of pv cell and also the big selection of loading conditions. The combined techniques with success addressed the foremost vital power loss effects and problems in pv cell conversion.

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joined in JNTU in 1985 and worked in various Capacities. Became Professor in the year 2005. He was head of the Department from 2006-2008. As Head of the department he has established Power Electronic controlled drives lab, which is unique in the state of Telangana.