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A Voltage Boost NPC Multilevel Inverter using LC Impedance Network

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ABSTRACT

For many industrial applications, a voltage boost neutral point clamped (NPC) multilevel inverter is a preferred choice due to its advantages such as low cost, light weight and small in size as compared to a conventional inverter. As this inverter has the boosting property which makes it more suitable for low and medium power renewable energy system. The voltage boost multilevel Z-source inverter and quasi-Z-source inverter have been proposed for dc to ac power conversion with improved power quality. Multilevel ZSI and quasi-ZSI (QZSI) uses more number of passive components in the intermediate impedance network, which increases the system size and weight. So here in this proposed voltage boost neutral-point clamped multilevel (three-level) inverter with LC impedance network uses comparatively less number of passive components and only single dc source required, at the same time it provides all the advantages of multilevel ZSI/QZSI. This proposed inverter has the ability to boost the input dc voltage and provide required three level ac output voltage in a single stage using a shoot through state. Modulation technique adopted for the proposed inverter is unipolar pulse width modulation (PWM) technique to investigate its performance. The prototype has been made and tested using Simulink and DS1104 R&D controller board dSPACE. The results analysis has been done using MATLAB/Simulink software package.

Keywords : Neutral point clamped inverter, Boost inverter, LC impedance network, PWM scheme, shoot through state.

I. INTRODUCTION

Recently the modern power electronics equipment has attracted the attention in many industrial applications. Most of the industrial applications need high power equipment, such as motor drives, hybrid electric vehicles, renewable energy system, etc.[1]. Some industries require medium voltage and high power, so for these purposes, the multilevel inverter has been introduced. The multilevel inverter provides high power rating and enables the use of renewable energy sources [2]. The multilevel inverter available with different topologies. Each of three main topologies provides some advantages over conventional two-level inverters such as the use of high switching frequency, improve efficiency and power quality of outputs with some limitations. The neutral point clamped (NPC) inverter topology can be applied to three level or higher-level inverters. Because of industrial developments over the past several years, now the three-level NPC inverter has been used extensively in industrial applications [3-5].

In conventional system, DC-DC boost converter was used before inverter or step up transformer after the inverter to get required AC output voltage from low input voltage. Due to this the power conversion stages increases, system efficiency decrease and the system becomes complex [6]. The Z-source converter identifies all the above limitation of conventional converter and to overcome these limitations provides

a new power conversion method. Z-source converter which uses LC impedance network has been utilised for AC-DC, DC-AC, DC-DC power conversion. This Z source network is uses in between supply source and converter main circuit [7-9]. Conventional voltage source inverter (VSI) operated in active state and zero state while the Z-source Neutral point clamped (NPC) multilevel inverter can operates with one additional state i.e. active state, zero state and shoot through state. Shoot through state means turning on all the switches of one or all legs of inverter. Using this shoot through state the input DC voltage gets boosted and provides expected AC output voltage.

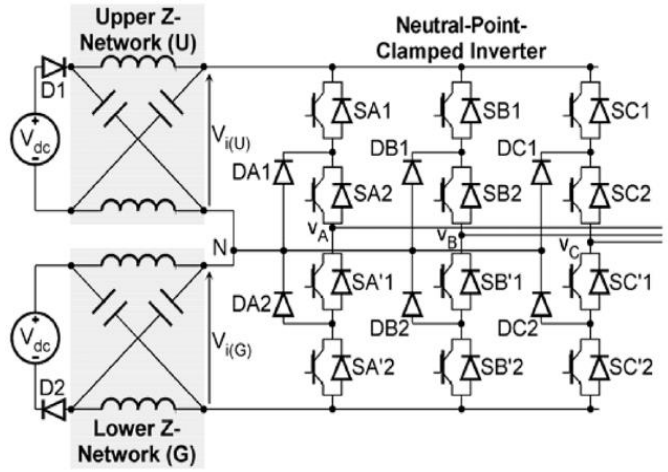


Fig -1: Conventional three level NPC Z-source inverter

Conventional NPC Z-source inverter utilizes four inductors, four capacitors, two diodes in its LC impedance network as shown in figure-1. This conventional inverter needs two isolated DC voltage sources to get expected output [10]. Similarly, the three-level dual Z-source inverter uses one diode, two inductors, two capacitors and open end winding line frequency transformer to get desired output. But the use of open-end winding line frequency transformer and more number of passive elements makes system complex and bulky. The input current of this Z-source inverter is discontinuous and making it continuous requires equal inductor and capacitor pair in its LC impedance network. It has been difficult to get the equal value of inductor and capacitor pair while making this system in practice [11]. Quasi Z-source multilevel inverter provides continuous input current, but it also required more number of passive elements and isolated DC source supply [12]. Similarly, a cascaded three-level NPC Quasi Z-source multilevel inverter utilizes more number of passive elements and two or more isolated dc sources supply for better quality. But the use of more number of passive elements and multiple isolated dc power supply increases the system size, weight so the overall cost [13-14].

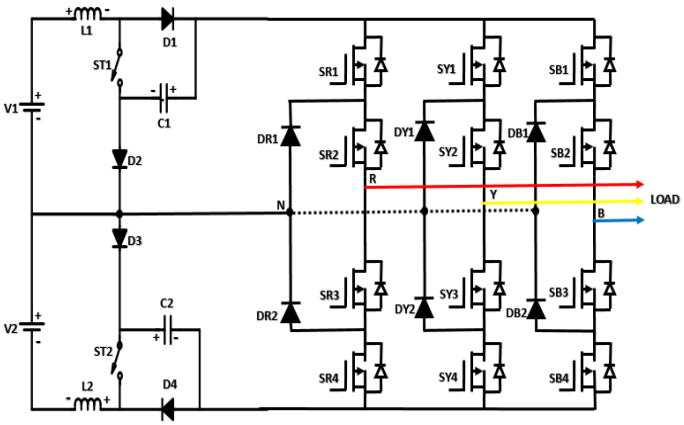


Fig -2: Proposed voltage boost NPC multilevel inverter using LC impedance network

This paper presents proposed work on a voltage boost NPC multilevel inverter using LC impedance network. This inverter uses impedance network comprises of two inductors, two capacitors, four diodes, and two intermediate switches (shoot through switches) between NPC inverter legs and DC source supply. It requires comparatively less number of passive elements while providing all the advantages of conventional available inverter. These features of this proposed inverter making it reliable and system weight and size are reduced. This inverter can be used in medium or low power application where weight and size are main constraints.

Rest of the paper is arranged as follows. The operational principle of the proposed inverter with its different operating state is presented in Section II. Design consideration and mathematical formulation of L and C are presented in Section III. Modulation

scheme use for this proposed inverter is discussed in Section IV. Simulation and prototype results are discussed in Section V and conclusion of this proposed work in presented in Section VI.

II. PROPOSED VOLTAGE BOOST NPC INVERTER AND OPERATIONAL PRINCIPLE

The proposed voltage boost NPC inverter is able to boost the input DC source supply (V) and provide required multilevel AC voltage. The schematic circuit diagram of proposed voltage boost NPC inverter using minimal count of L and C in impedance network is as shown in figure-2. Here input to this inverter is a simple dc input voltage source. This DC source supply can be fed from the dual power supply as two DC source. Another way is DC source can be split into two by proving required DC voltage in parallel to two series connected capacitor, where the center point between two capacitors considered as a neutral point. This input is then provided to upper and lower part of this proposed inverter. The inverter is consists of three legs, one per phase, each containing two series connected high-side switches and two series connected low-side switches. The center of each device pair is clamped to the neutral through clamping diodes.

In this inverter, the impedance network comprises of one inductor (L1), two capacitors (C1 and C2), four diodes (D1, D2, D3, and D4) and two active intermediate switches (ST1 and ST2). This impedance network is placed between input DC source supply and NPC inverter legs. As compared to the conventional three-level Z-source inverter this proposed inverter utilizes almost half of the number of passive elements. Hence the size and the weight is reduced, so overall cost also reduces. Conventional VSI operated in only in two states while the proposed inverter can operate in three states i.e. active state, zero state, and the shoot through state. Using this third additional state the input voltage has boosted. The detail working of all possible mode of this inverter is discussed as follows.

A. Active state (Non-shoot through state)

In this mode of operation, the power is transferred from DC supply side to AC load side. It is same as the active state of traditional NPC VSI. In this state, the AC load gets either "+Vdc" or "-Vdc" voltage level with respect to a neutral point "N". Here for simple understanding, only one leg from three legs of three-phase NPC inverter is considered as the normal constant current flowing through it.

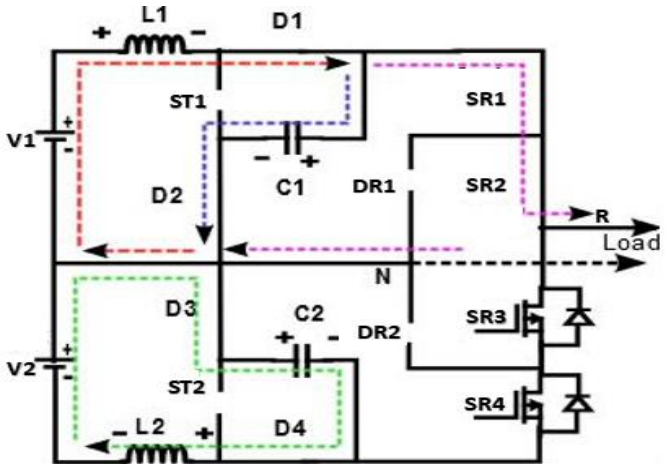


Fig-3: Operating circuit of proposed inverter to get "+Vdc"

For attaining the "+Vdc" (positive half cycle) across the load the switches Sx1 and Sx2 are turned 'ON' while switches Sx3, Sx4, ST1, and ST2 are turned 'OFF'. As a result diodes D1, D2, D3 and D4 are getting forward biased while Dx1 and Dx2 (where x = R, Y, and B) are get reversed biased, as shown in figure-3. In this mode of operation both upper DC voltage source 'V1' and energy stored in inductor 'L1' supplies the power to the AC load as well as energizing the capacitor 'C1'. Similarly lower DC voltage source 'V2' and energy stored in inductor 'L2' energizing the capacitor 'C2' to '+VC1' as shown in the figure above. So, the voltage appears across the AC load in this period is '+VC1'.

Similarly, for attaining the "-Vdc" (negative half cycle) across the load the switches Sx3 and Sx4 are turned

'ON' while switches Sx1, Sx2, ST1, and ST2 are turned 'OFF'. As a result diodes D1, D2, D3, and D4 are getting forward biased whereas diodes Dx1 and Dx2 (where x = R, Y, and B) are get reversed biased, as shown in figure-4. In this mode of operation both lower DC voltage source 'V1' and energy stored in inductor 'L2' supplies the power to the AC load and energizing the capacitor 'C1'. Similarly lower DC voltage source 'V1' and energy stored in inductor 'L1' energizing the capacitor 'C1' to '+VC2'. So, the voltage appears across the AC load in this period is '+VC2'.

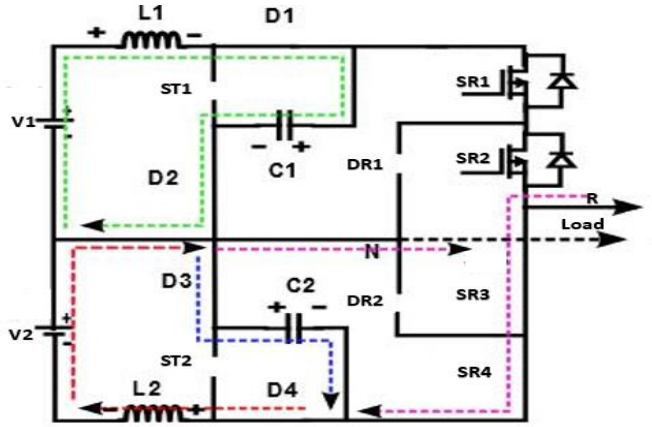


Fig -4: Operating circuit of proposed inverter to get "-Vdc"

B. Zero state

Figure-5 shows the zero state of the proposed inverter. In this mode of operation, switches Sx2, Sx3 are turned 'ON', whereas switches ST1, ST2, Sx1 and Sx2 (where x = R, Y, and B) are turned 'OFF', and diodes D1, D2, D3, and D4 are forward biased. So voltage appears across the load is zero. It simply means that no power is transferred to load from DC source to load side. Here upper DC voltage source 'V1' and energy stored in inductor 'L1' energizing the capacitor 'C1', whereas lower DC voltage source 'V2' and energy stored in inductor 'L2' energizing the capacitor 'C2', same as in case of the active state operation.

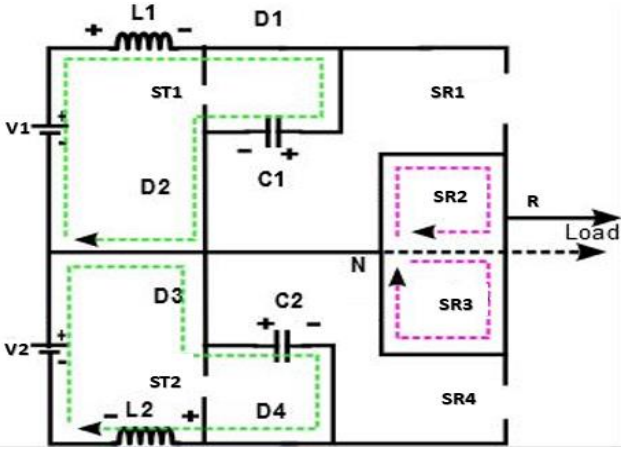


Fig -5: Operating circuit of proposed inverter during zero state "0 V"

C. Shoot through state

In the multilevel inverter, the shoot-through means switching on all the switches in the inverter leg results in the dead short circuit of the source in the conventional inverter, which can be avoided by using the proper dead band. Here the shoot-through state is utilized to get an additional level along with passive reactive element to boost the input dc voltage.

In this state of operation, all the switches of one or more inverter leg i.e. Sx1, Sx2, Sx3, and Sx4 as well as switches ST1 and ST2 are turned 'ON'. Due to this, diodes D1, D2, D3, and D4 are reverse biased as shown in figure-6. During this state stored energy in the capacitor 'C1' along with upper DC voltage source 'V1' energizes the inductor 'L1'. Similarly, stored energy in the capacitor 'C2' along with lower DC voltage source 'V2' energizes the inductor 'L2'.

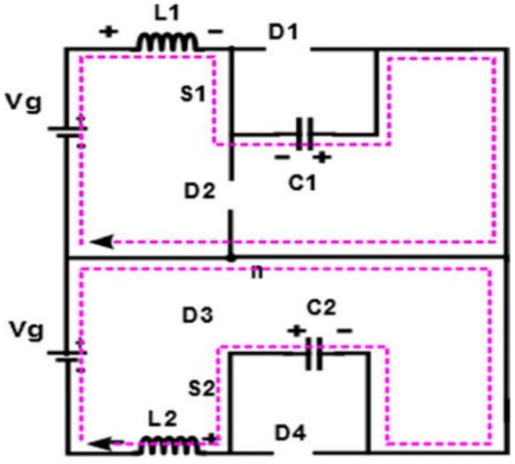


FIg-6: Operating circuit of proposed inverter during shoot through state

During both zero state and non-shoot through state in (1-Dst)*Tst:

VL1 = V1 – VC1 (1)

VL2 = V2 – VC2 (2)

While during shoot through state in (Dst*Tst)

VL1 = V1 + VC1 (3)

VL2 = V2 + VC2 (4)

Where,

V1 and V2 = Input DC voltage sources

VL1 and VL2 = Voltage across inductor L1 and L2

VC1 and VC2 = Voltage across capacitor C1 and C2

Dst = Duty ratio during shoot through state

Tst = Switching period of switches in the inverter

Now, using equation (1) and (3) under volt-sec balance condition,

(V1 – VC1)(1-Dst)*Tst + (V1 + VC1) Dst*Tst = 0 (5)

From equations (5), voltage across C1 is

$$VC1 = \frac{V1}{1-2Dst} \quad (6)$$

Similarly, using equation (2) and (4) under volt-sec balance condition,

(V2 – VC2)(1-Dst)*Tst + (V2 + VC2) Dst*Tst = 0 (7)

From equations (7), voltage across C2 is

$$VC2 = \frac{V2}{1-2Dst} \quad (8)$$

From equation (6) and (8), it can be seen that both the values of V1= V2= V,

Therefore, VC1 = VC2 = VC

$$VC1=VC2=VC = \frac{V}{1-2Dst} \quad (9)$$

From equation (9), it can be observed that the voltage across capacitors C1 and C2 are balanced. Let consider M is modulation index on which the inverter is operated. So, the relation between M and output phase voltage (AC peak value) will be,

$$\hat{V}_M = M*VC = \frac{MV}{1-2Dst} \quad (10)$$

The boost factor (B) of this inverter given by

$$B = \frac{1}{1-2Dst} \quad (11)$$

Comparing equation (10) and (11) we get,

$$\hat{V}_M = M*B*V \quad (12)$$

Voltage gain factor (G) is a factor by which the input voltage V becomes VC and is given by,

$$G = \frac{M}{1-2Dst} \quad (13)$$

$$G = M*B \quad (14)$$

So, by choosing proper values of M and Dst, this inverter can be used as boost inverter to get required output voltage. To get proper switching with this additional shoot through state the Dst and M should be, M+Dst ≤1.

III. DESIGNING CONSIDERATION OF THE L AND C AND MATHEMATICAL FORMULATION

For boosting purpose the value of inductor L and capacitor C should be properly selected. The designing of an inductor not easy and its selection is based on some typical criteria. It is typically larger and more expensive than the other circuit components and the most difficult of them to specify. Minimization of its inductance, size, and cost has become a very important factor while designing. The value of inductor for the boost converter has been selected on the basis of the inductor current ripple. With the help of some Texas Instrument datasheet [15-16], the calculation for inductor L has been done.

$$L = \frac{V \times (Vo - V)}{\Delta IL \times fs \times Vo} \quad (15)$$

Where,

V = typical input voltage
Vo = desired output voltage
fs = minimum switching frequency of the converter
ΔIL = estimated inductor ripple current
For estimating the inductor ripple current, following equation is used

$$\Delta IL = (0.2\ to\ 0.4) \times Io(max) \times \frac{Vo}{V} \quad (16)$$

ΔIL = estimated inductor ripple current
$Io(max)$ = maximum output current
Inductor ripple current (ΔIl) is normally 20%-40% of inductor current (IL).

The following equations can be used to calculate the capacitor values for a desired output voltage ripple

$$C = Co(min) = \frac{Io(max) \times D}{fs \times \Delta Vout} \quad (17)$$

$C = Co(min)$ = minimum output capacitance
$Io(max)$ = maximum output current
Dst = duty cycle
fs = minimum switching frequency of the converter
ΔVo = desired output voltage ripple

$$\Delta Vo = ESR \times \left(\frac{Io(max)}{1-Dst} + \frac{\Delta IL}{2}\right) \quad (18)$$

ESR = equivalent series resistance of capacitor

IV. MODULATION SCHEME FOR A VOLTAGE BOOST NPC MULTILEVEL INVERTER

As there are total twelve switches, four switches per phase leg for this three-phase NPC inverter are available. For simple understanding here only four switches (Sx1 to Sx4) of one leg and two intermediate shoot through switches (ST1 and ST2) are considered. Here for generating gate control signal for each of inverter leg switch, the conventional sine-triangle comparison based pulse width modulation (PWM) with unipolar voltage switching scheme is used. Here, for each phase, two modulating sine waves Vm(t) and –Vm(t) of 180° phase displacement are compared with triangular carrier signal Vtri(t) having a high frequency as shown in figure-7. When the modulating signal is greater than carrier signal the gate pulse is generated. For three phases, these modulating signals Vm(t) and –Vm(t) are phase displaced by 120° and compared with a triangular carrier signal to generate gate control signal for the inverter leg switches. The shoot through gate control signals are generated by comparing the high-frequency carrier signal *V*tri(*t*) with two constant signals *V*st and -*V*st of amplitude (1-Dst). When the upper carrier signal is greater than the Vst and the lower carrier signal is less than –Vst the shoot through signal is generated.

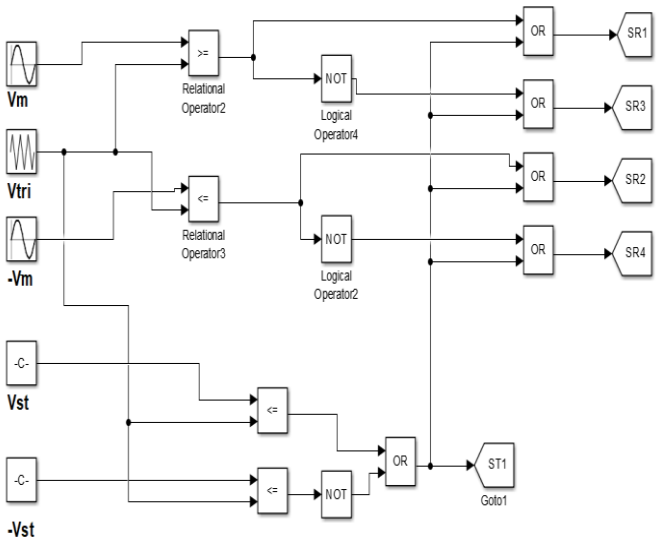


Fig -7: Unipolar PWM gate signal generation

The gate control signals generated by using this unipolar PWM scheme are logically compared with the shoot through control signal and the combination of these signals fed to the switches of the inverter legs. These control signals are provided using dSpace controller board and gate driver circuit as shown in figure-8.

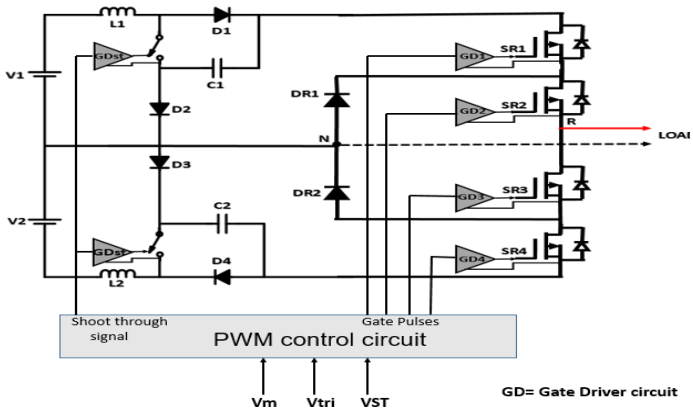


Fig -8: Actual PWM gate signal provide using gate driver circuit

V. SIMULATION AND PROTOTYPE RESULTS

The analysis of this proposed inverter has been done using MATLAB/Simulink. For simulation purpose, the parameters have been chosen using above calculations. The parameters are as, input DC voltage source V1=V2=30 V, inductor L1=L2=3.33 mH, capacitor C1=C2≥470 μC, fundamental frequency f =50 Hz, while switching frequency fs=2000 Hz, load/phase=350 Ω, and AC output voltage VM=64 V rms. The MATLAB simulation circuit of the proposed inverter as shown in figure-9.

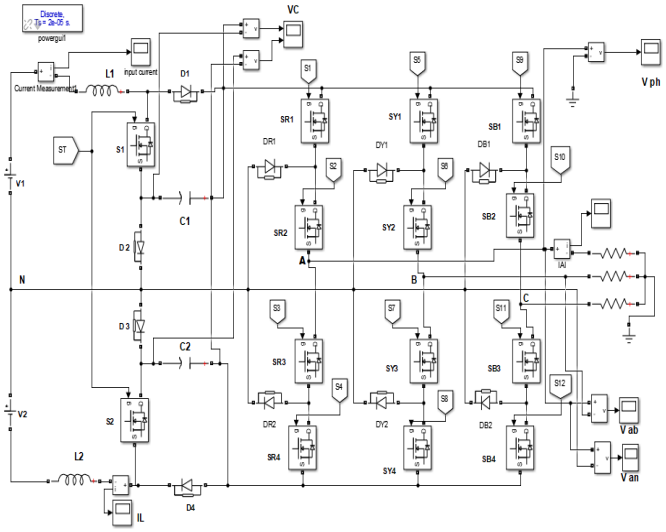


Fig -9: MATLAB simulation of proposed inverter

After simulating the proposed inverter in MATLAB Simulink with shoot through duty ratio (Dst) = 40% and modulation index have found to be (M) = 0.6, the following results have come. When the input voltage to the inverter is 30 V DC, the voltage across both the capacitors has found to be same, it means the capacitor voltages are balanced (VC1=VC2≈200 V) as shown in figure-10. Current flowing through the inductor during the working of the inverter is comes as nearly equals to 4 A, with 40 % current ripple. This current is as shown in figure-11.

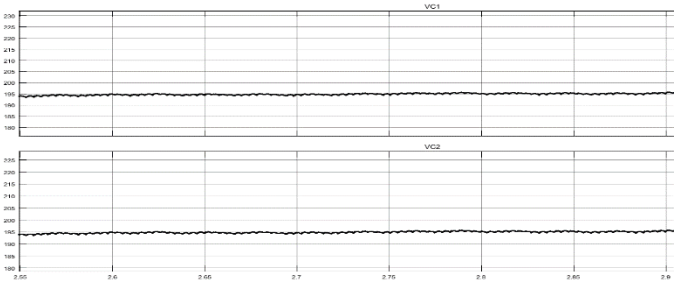


Fig -10: Voltage across the capacitor C1 and C2

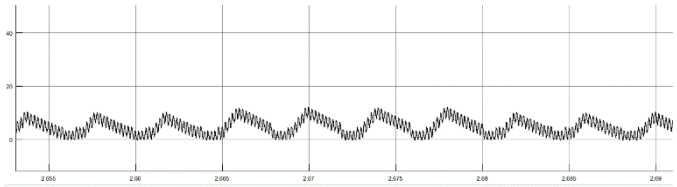


Fig -11: Inductor current

The three-level pole voltage (the voltage of one phase leg with respect to neutral point) VxN has been seen in in the figure-12. It is seen that this pole voltage has three levels +200 V, 0 V and -200V.

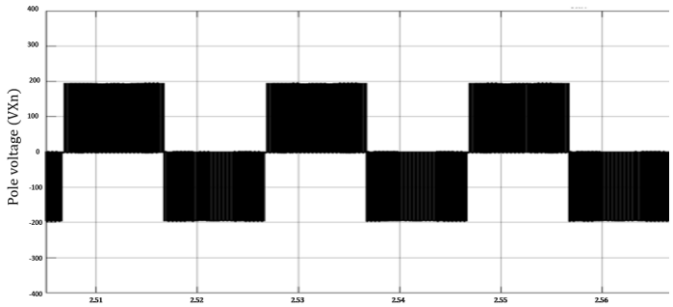
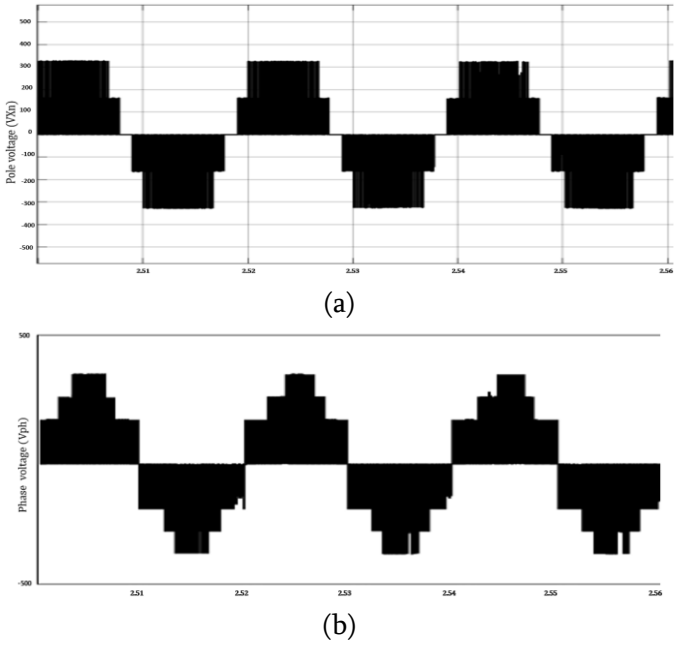


Fig -12: Pole voltage VxN

Similarly, the line to line voltage and phase voltage output waveform also as shown in following figure-13. It can be observed that the line to line voltage is approximately 1.73 times the pole voltage.



(a)

(b)

Fig -13: (a) Line to line voltage, (b) Phase voltage

After doing the FFT analysis the total harmonic distortion (THD) of the output phase voltage has found to be nearly 19%, as shown in figure 14.

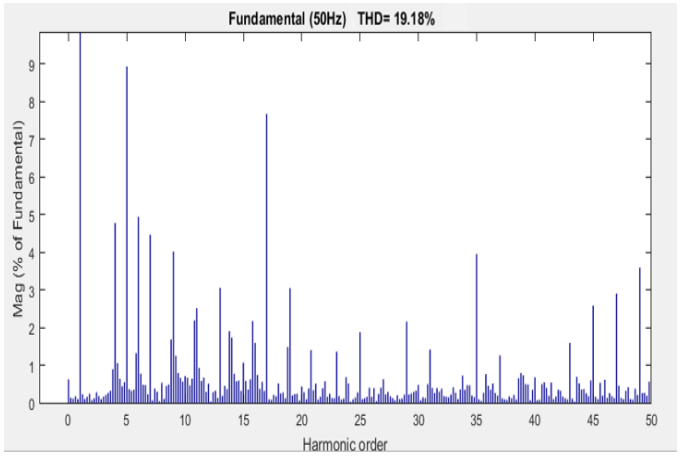


Fig -14: THD spectrum of proposed inverter

The prototype of this proposed inverter has been developed. Figure 15 shows the prototype of proposed inverter. The parameters for this voltage boost NPC multilevel inverter using LC impedance network are same as in case of simulation. Inductor and capacitor are selected on the basis of calculation. Modulating gate control signals have been generated using dSPACE R&D control Board 1104. Gate driver IC TLP 250 has been used here, which required +Vcc=15V for its operation. This gate driver circuit provides a gate signal to G terminal for the switch as shown in figure-16.

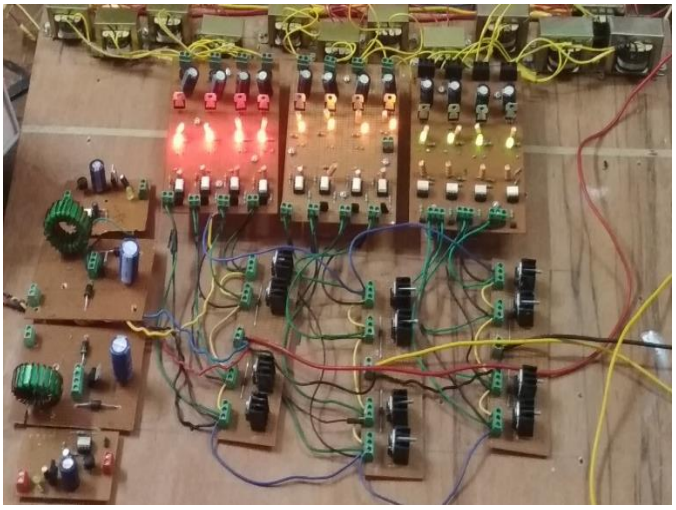


Fig -15: Hardware prototype of proposed inverter

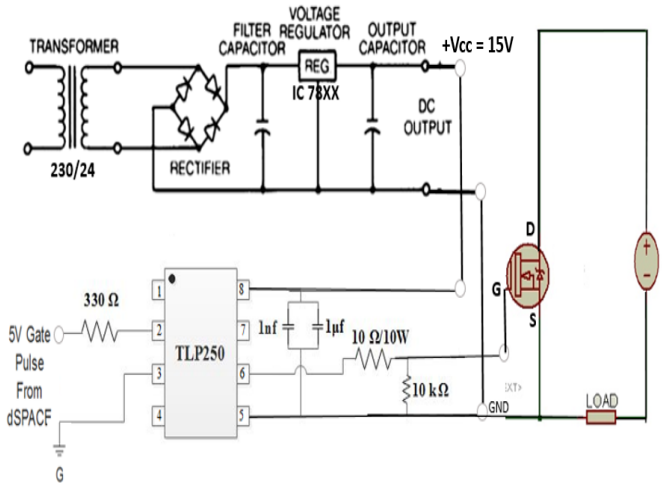
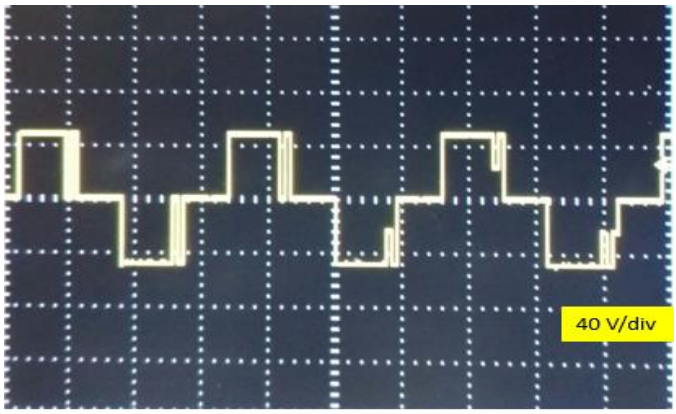


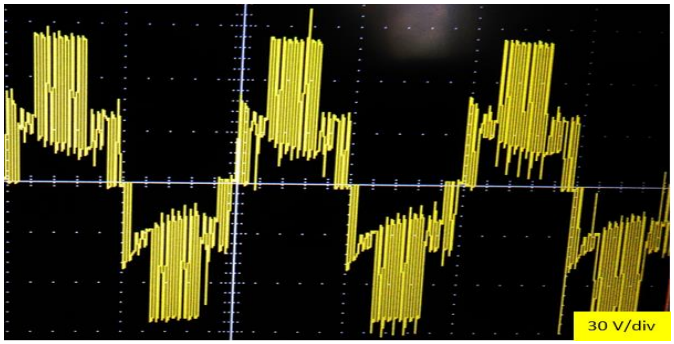
Fig -16: Complete control circuit for gate pulse generation

The prototype is initially run with low voltage and gradually its input voltage has been increased. When the input voltage set to 15 V the three-level pole voltage has been observed. The input 15 V to the proposed inverter has first being boosted to 46 V and same voltage have been fed to inverter legs.

The output waveforms of pole voltage and line to line voltage are as shown in figure 17.



(a)



(b)

Fig -17: Pole voltage and line to line voltage of prototype

VI. CONCLUSION

The proposed voltage boost multilevel NPC inverter using LC impedance network is able to boost the input dc voltage and provide required three-level ac output in a single stage. It uses the shoot through state for boosting up the voltage. It retains all the advantages of the multilevel Z-Source inverter and multilevel quasi Z-Source inverter using comparatively less number of passive reactive elements, so the weight, size, and cost are reduced. The most important part while designing this inverter is to design LC impedance network properly. If the values of L and C selected properly then the performance of this proposed inverter will be better and more efficient. Otherwise, the inductor may get saturated and performance will degrade. Unipolar PWM technique adapted for the proposed single inverter had been discussed which is simple and easy to implement. The inverter operation is analyzed by simulation using MATLAB/Simulink.

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