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# Design and Hardware Implementation of a Nine level Inverter with Less Switches Operating in Stand-Alone Mode

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## ABTRACT

This paper presentss a single-phase nine-level (9L) inverter configuration which can be suitable for grid-connected renewable energy systems. The proposed inverter is realized using a T-type neutral point-clamped inverter connected in series to a flying capacitor (FC) H-bridge. A self-voltage balancing based on superfluous switching state is developed and integrated with PWM controller, which is responsible for constrain the FC voltage at one-fourth of the input dc source voltage. The advance PWM technique employs the generation of 9L waveform without using any voltage sensor, thereby reducing the complicacy of the overall control scheme. In comparison to conventional and recent configurations, generation of the 9L waveform using a lower number of components is the notable contribution. Furthermore, a compendious comparison study is included which confirms the merits of the proposed inverter against those of other state-of-the art topologies. Finally, simulation results are included for validating the feasibility of the proposed system.

**Keywords:** Flying Capacitor, Nine-Level Inverter, Power Quality, Sensorless Voltage Control.

## I. INTRODUCTION

In recent days price of petroleum oil is increased and the environmental conditions are also becoming worst so that demand of electrical energy is increased. To supply this demand for electrical energy has elevated the need for generating energy from alternate sources. A simple three-level (3L) inverter presented by Nabae et al. [1] is one of the standard topology that has gained more attention. However, there are also some disadvantages like high switching frequency, high acoustic noise and for voltage levels greater than three level more number of dc sources are used due to that more power loss occurs [2].The concept of multilevel inverters (MLI) has been introduced since mid-1970. The term multilevel originated with the three-level inverter. Subsequently, several multilevel inverter topologies continue to emerge, especially in the last two decades. Multi-Level inverters are power conversion systems designed by power semiconductors and DC voltage sources that, when appropriately connected and controlled. They can generate a multiple-level-step voltage waveform with variable and controllable frequency, phase and amplitude [3].

Currently, some of the popular topologies that are considered as suitable for multilevel inverters. These are the cascaded H-bridge (CHB), neutral-point-clamped (NPC), modular multilevel converter (MMC), a flying capacitor and their variants [4], [5]. When the number of levels are increased, harmonic distortion increases. So that to achieve superior waveform quality more components are required. Which is profoundly impacts the inverter size and cost. Such inverters generate low harmonic waveforms; therefore they are most suitable for energy conversion applications to deliver efficient power to the loads

from renewable energy sources like photovoltaic systems [6-9]. Several innovative inverter topologies with a claim of a reduced part count (RPC) are reported in literature [10], [11].

The topology proposed in [12] can generate a Seven Level output voltage waveform with RPC. However it has disadvantage of unbalancing in capacitor voltage and control technique become more complex. An analyzed survey of applicable nine level inverters for distributed generation (DG) system is presented in [13]. Also, a new topology with a cascade connection of 5L active neutral-point-clamped (ANPC) and 3L floating capacitor (FC) H-bridge is proposed. A combination of CHB with FC H-bridge presented in [14] consists of one dc source and eight switches only. However, regulation of FC voltage at $1/3V_{dc}$ requires additional circuit. A configuration which includes 5L double flying capacitor multicell (DFCM) converters cascaded with FC Hbridge is recommended in [15] to overcome the increased diversity factor in a DFCM converter. A nine level cross-connected intermediate level unit integrated with ANPC is introduced in [16]. Most of these topologies are hybrid combinations of one or more converter families (NPC, FC, and CHB). Many such hybridizations resulting in nine level RPC inverter these are reported in literature [17]–[19]. Although for same voltage levels, the topologies mentioned require a lesser number of components, higher complexity in control mechanism.

This paper presents the Nine-level inverter for single phase system using self-voltage balancing technique integrated PWM technique. The paper is organized as follows. Section II explains nine level inverter. Section III explains the comparative study of the inverter. Section IV explains experimental results with harmonic analysis and Section V summarizes the result.

## II. PROPOSED NINE-LEVEL INVERTER CIRCUIT DESCRIPTION

### A. Circuit Description

Fig. 1 shows the power circuit topology of the proposed nine level inverter. It consists mainly three units; a 3L TNPC cascaded with 3L FC H-bridge unit and two low-frequency switches (LFS) across the dc-link. With $V_{dc}$ is the total input voltage, the voltages across the dc-link capacitors and FC are equal to $V_{dc}/2$ and $V_{dc}/4$ respectively. The idea of seriesing of TNPC with FC yields in the following advantage of less number of power switches, power diodes, and capacitors. Ideally, the inverter is capable of generating nine levels of output voltage: $\pm V_{dc}$, $\pm 3V_{dc}/4$, $\pm V_{dc}/2$, $\pm V_{dc}/4$, 0. At a first sight, the series configuration of TNPC and FC with two LFS might seem unnoticeable. In the absence of a LFS unit, with the dc-link midpoint being the return path for the output current, the cascade combination of TNPC and FC can only generate five levels: $\pm V_{dc}/2$, $\pm V_{dc}/4$, 0. As a result, it can combines output voltage with additional levels: $\pm V_{dc}$ and $\pm 3V_{dc}/4$. For this, power switches are to be gated appropriately in a sequence. Table I summarizes all the possible switching combinations and their effect on the FC voltage. Assuming the devices to be ideal, FC is large enough and load as pure resistive, the active current path over a positive half cycle of the output voltage for each level is obtained as follows:

1) Maximum positive output ($V_{dc}$): This voltage is designated as $S_{4}+$. Switches $S_1$, $S_3$, and $S_4$ are ON, connecting the terminal a to $V_{dc}$, and $S_5^-$ is ON, connecting the terminal b to ground.
2) Three-fourth positive output ($3V_{dc}/4$): Two switching configurations are available. For $S_{31}+$, switches $S_1^-$, $S_2^-$, $S_3^-$, and $S_4$ are ON, connecting the terminal a to $V_{dc}/4$, and $S_5^-$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{dc}/2 + V_{dc}/4 = 3V_{dc}/4$. For $S_{32}+$, switches $S_1$, $S^-_2$, $S_3$, and $S^-_4$ are ON, connecting the

terminal a to $-V_{dc}/4$, and $S_5^-$ is ON, connecting the terminal b to ground.

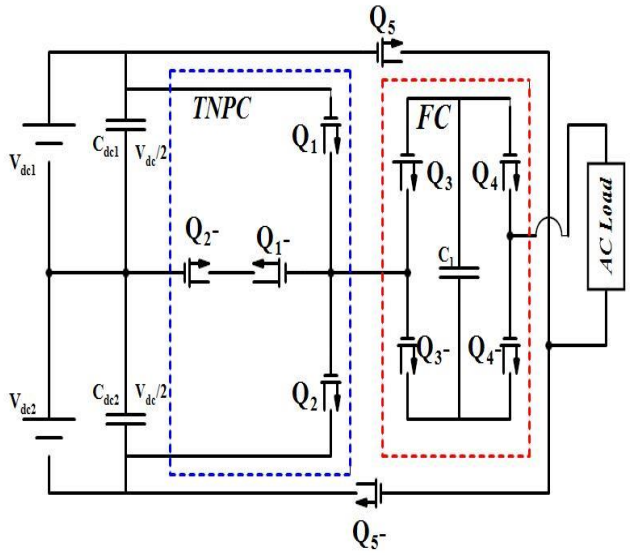



Fig. 1. Circuit topology of the inverter.

3) Half-level positive output ($V_{dc}/2$): This voltage is designated as $S_2+$. Switches $S_1^-$, $S_2^-$, $S_3$ and $S_4$ are ON, connecting the terminal a to $V_{dc}/2$, and $S_5^-$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{dc}/2 + 0 = V_{dc}/2$.
4) One-fourth positive output ($V_{dc}/4$): Two switching combinations are available. For $S_{11}+$, switches $S_2$, $S_3^-$ and $S_4$ are ON, connecting the terminal a to $V_{dc}/4$, and $S_5^-$ is ON, connecting the terminal b to ground. For $S_{12}+$, switches $S_1$, $S_2^-$, $S_3$, and $S_4^-$ are ON, connecting the terminal a to $+V_{dc}/4$, and $S_5^-$ is ON, connecting the terminal b to ground. Thus the voltage across the load is $V_0 = V_{dc}/2 - V_{dc}/4 = V_{dc}/4$.
5) Zero output: Two switching combinations are available. For $S_0+$, switches $S_2$, $S_3$ and $S_4$ are ON, connecting the terminal a to ground, and $S_5^-$ is ON, connecting the terminal b to ground. For $S_0^-$, switches $S_1$, $S_3$ and $S_4$ are ON, connecting the terminal a to $V_{dc}$, and $S_5$ is ON, connecting the terminal b to $V_{dc}$. In both cases, the terminal ab is short circuited, and the voltage across the load is zero.

Consequently, the number of active power switches in the circuit current path is lower in comparison to and hence, this topology has a better efficiency.

B. Sensorless voltage balancing controlling integrated into PWM Technique

Nine-level PWM scheme including four carriers' waves and the sinusoidal reference waveform is depicted in Fig. 2. The four carriers' waveforms ($Cr_1$, $Cr_2$, $Cr_3$, and $Cr_4$) are shifted vertically to modulate the reference waveform ($V_{ref}$) completely [20, 21]. The firing pulses associated with switching states 1, 2, 3, 4 and 5 (as listed in table I) are generated based on comparing $V_{ref}$ with those carrier waves. Moreover, surplus switching states of 4 and 5 are used to minimize the switching frequency. If $V_{ref}$ is positive, then state 4 will be used to produce the zero level at the output. On the other hand, if $V_{ref}$ is negative, the output zero level voltage will be generated by state 5. The described algorithm is shown in Fig. 2 which can produce the nine-level voltage waveform at the output without any feedback sensor.

TABLE I
SWITCHING STATES AND THEIR IMPACT ON FC VOLTAGE OF THE PROPOSED INVERTER

| States | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | Output voltage | FC voltage |
|---|---|---|---|---|---|---|---|
| S4+ | 1 | 0 | 1 | 1 | 0 | Vdc | No effect |
| $S31^+$ | 0 | 0 | 0 | 1 | 0 | $3V_{dc}/4$ | Dischargin g |
| $S32^+$ | 1 | 0 | 1 | 0 | 0 | $3V_{dc}/4$ | Charging |
| S2+ | 0 | 0 | 1 | 1 | 0 | $V_{dc}/2$ | No effect |
| $S11^+$ | 0 | 1 | 0 | 1 | 0 | $V_{dc}/4$ | Disharging |
| $S12^+$ | 0 | 0 | 1 | 0 | 0 | $V_{dc}/4$ | Charging |
| S0+ | 0 | 1 | 1 | 1 | 0 | 0 | No effect |
| S0– | 1 | 0 | 1 | 1 | 1 | 0 | No effect |
| $S11^-$ | 1 | 0 | 1 | 0 | 1 | $-V_{dc}/4$ | Dischargin g |
| $S12^-$ | 0 | 0 | 0 | 1 | 1 | $-V_{dc}/4$ | Charging |
| S2– | 0 | 0 | 1 | 1 | 1 | $-V_{dc}/2$ | No effect |
| $S31^-$ | 0 | 0 | 1 | 0 | 1 | $-3V_{dc}/4$ | Dischargin g |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| S32- | 0 | 1 | 0 | 1 | 1 | $-3V_{dc}/4$ | Charging |
| S4– | 0 | 1 | 1 | 1 | 1 | $-V_{dc}$ | No effect |

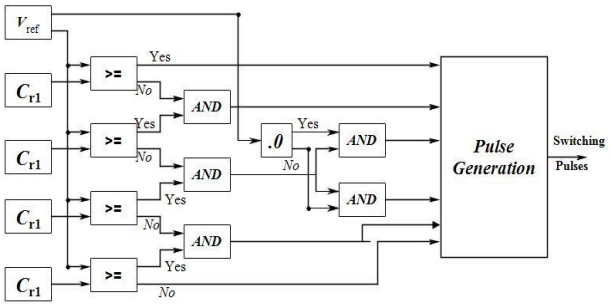



Fig.2 open-loop switching algorithm for self-voltage balancing of inverter

As mentioned before, applying the proposed algorithm on above inverter generates Nine-level voltage waveform at the output without using any voltage sensors and complex calculations in controller. The capacitor voltage would be constant even at start-up and also in load change conditions.

## III. COMPARATIVE STUDY OF MULTILEVEL INVERTER

Table II shows the components count in popular multilevel inverters as well as the presented inverter in case of producing single-phase 9-level output voltage waveform. It is prominent that the presented inverter with the sensor-less voltage balancing technique has the less components as well as its control scheme complexity is very low.

TABLE II
COMPONENTS COUNT FOR SINGLE-PHASE NINE-LEVEL INVERTERS

| Inverter type | DC Source | Capacitor | Clamped Diode | Active Switch | Total Part Count | Control Complexity |
|---|---|---|---|---|---|---|
| CHB | 4 | 0 | 0 | 16 | 20 | Low |
| NPC | 8 | 0 | 14 | 16 | 38 | Very high |
| FC | 1 | 7 | 0 | 16 | 24 | High |
| Presented Inverter | 2 | 3 | 0 | 10 | 15 | Very Low |

As a comparison between conventional inverter and the proposed nine level inverter, it should be noted that the other inverters needs a very complicated controller to produce desired voltage levels at the output which requires adjusting a lot of controller gains in practical works[24-26]. Moreover, the controller design needs a lot of effort in modelling the system accurately and using many state variable feedbacks that increase the number of state variables and consequently voltage and current sensors. Mainly, It is highly dependent on the system parameters including load, connection line resistance and inductance, switching frequency, sampling time, DC source voltage amplitude, DC capacitor value, modulation index and output voltage frequency. Less complex controller and lower switching frequency are some advantages of the proposed nine level inverter with less number of components.

## IV. EXPERIMENTAL RESULTS

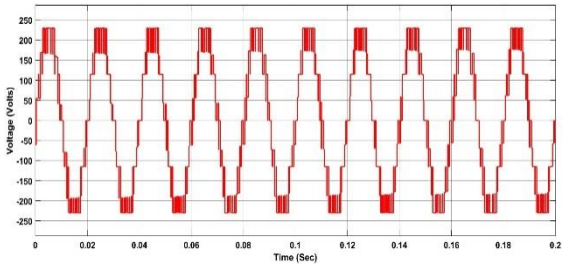
MATLAB simulation of nine level inverter is simulated to check the results. The voltage balancing of capacitor is validated in both stand-alone mode and grid connected modes. The parameters are Grid voltage-240V,50 Hz, Grid link inductor-1.5mH, DC Source Voltage-240V,Switching Frequency-2.5kHz, Stand Alone RL load-10 Ohm,30mH, Dc floating Capacitor-2.5uF

A. Stand Alone Mode

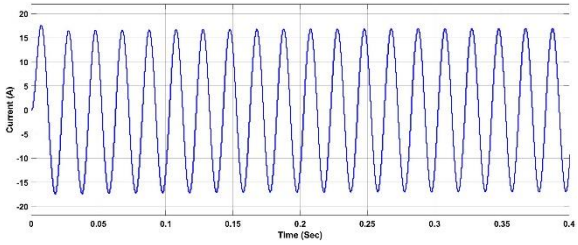
The Nine level inverter is tested under stand-alone mode as Uninterruptible Power Supply (UPS) application. In this application we can change load

and DC supply. Here, the inverter supplies an RL type of Load.

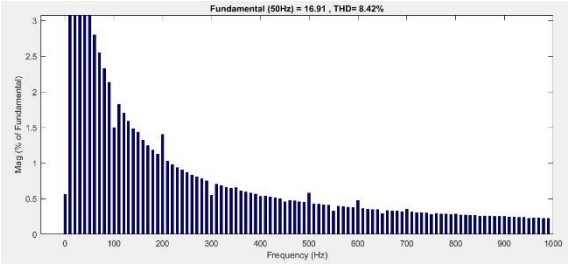
Fig. 4(a) shows the starting of inverter. The capacitor is charged up to the one-fourth of the DC source. This happen because of self-voltage balancing technique and Sinusoidal PWM technique, so that nine level symmetric output voltage is generated. From result we can that Capacitor is need not to be charged previously, because of this switching technique. The Fast Fourier Transform (FFT) analysis of inverter output current is carried out and it is shown in fig.5 (c). It should be mentioned here that the THD of the output current is less than 10% and it is achieved without using any kind of harmonic filters



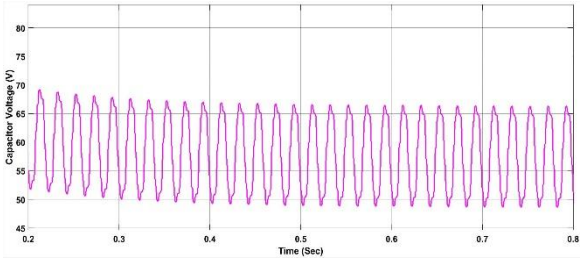

(a)




(b)




(c)




(d)

Fig. 4. Simulation results: (a) Inverter's Nine level output voltage. (b)Output current of RL load (c) THD of the load current from FFT analysis. (d) Voltage across dc-link capacitors for a step change in dc source amplitude

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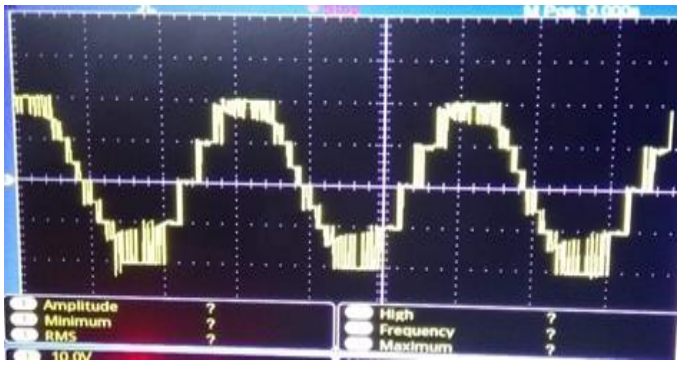
Fig 4 (d) shows that, when the dc source voltage is changed and capacitor voltage is tracking the reference value exactly. This shows that the sensorless voltage regulator technique is integrated into the proposed PWM technique.

B. Hardware Implementation

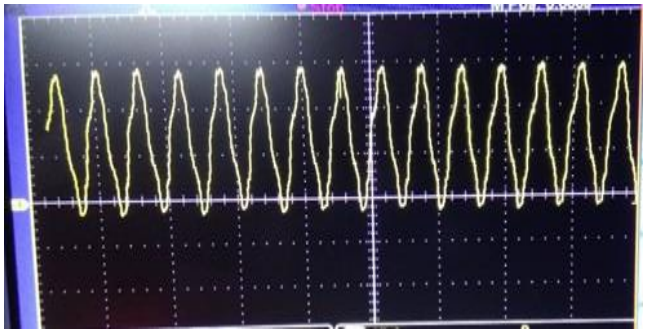
The following fig. 5 shows the hardware setup of the proposed inverter. 10 separate power supply given to the 10 gate driver circuits. Dual power supply is used to give two battery supply for the inverter. In this experiment gate pulses for the inverter are given by Arduino MEGA 2560 microcontroller. Digital Oscilloscope is used to check the output waveform of the inverter.

Fig. 5 Hardware setup of multilevel inverter

Fig.6 (a) shows the Output of the inverter. In this the simple R-L load is used. The Rheostat is set on the 50 Ohm value. Thus we got the nine level of the output voltage. The distortion of the capacitor voltage is also shown. The waveform is not smooth. Due to the improper capacitance values and also the loose connections. This whole setup is run by using ARDUINO (Mega2560) micro controller on the low switching frequency (1 KHz), so that the proper nine level output voltage waveform is not getting.




(a)



(b)

Fig. 6. Hardware results: (a) Inverter's Nine level output voltage of RL load (b) Voltage across dc-link capacitors for a step change in dc source amplitude

Thus we got the nine level of the output voltage. The distortion of the capacitor voltage is also shown. The waveform is not smooth. Due to the improper capacitance values and also the loose connections. This whole setup is run by using ARDUINO (Mega2560) micro controller on the low switching frequency, so that the proper nine level output voltage waveform is not getting. There is also the voltage imbalance between the voltage levels of the capacitor which are connected at the input side. To avoid this imbalance, capacitors of proper value will be used in next setup. There is also the power losses in the wiring of the inverter.

## V. CONCLUSION

Multilevel inverters are being developed and extensively exploited for generating high quality output voltages for numerous medium-voltage application fields. Applications urging a higher number of voltage levels escalate the number of components required. But use of high number of part counts in conventional multilevel inverters increases both the circuit intricacies as well as the control scheme involved, thereby resulting in higher cost implications and reduced reliability. Therefore, to subdue these disadvantages, this proposes a novel hybrid 9L inverter topology formed by cascading a TNPC and FC with two LFS connected across the dclink. This is achieved using only ten power switches (among which two are operated at line frequency). Only one FC is incorporated in the circuit for generating the 9L output voltage. Further, it is confirmed that the proposed inverter structure has improved reliability and by cascading additional FCs, it can be effortlessly extended to obtain even higher number of voltage levels. In addition, a sensorless PWM technique based on the principle of energy balance for regulating the voltage of FC is suggested. An exhaustive review of recently proposed multilevel inverter topologies with RPC applicable for grid integration of renewable sources is carried out and the ensuing comparison certifies the merits of the proposed topology over conventional inverters.

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