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Closed Loop Fuzzy Logic Control of an Open Ended Induction Machine using a Dual Inverter System with a Floating Capacitor Bridge

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ABSTRACT

This paper shows a dual three stage open end winding induction motor drive. The drive comprises of a three stage induction machine with open stator stage windings and dual extension inverter provided from a single DC voltage source. To accomplish multi-level output voltage waveforms a floating capacitor bank is utilized for the second of the dual extensions. The capacitor voltage is controlled utilizing excess switching states at half of the principle dc interface voltage. The primary controller (master controller) is designed as a Fuzzy logic controller. This specific voltage proportion (2:1) is utilized to make a multi-level output voltage waveform with three levels. An altered modulation conspire is utilized to enhance the waveform nature of this dual inverter. This paper likewise thinks about the losses in dual inverter system conversely with single sided three-level NPC converter. At last, point by point simulation and experimental comes about are exhibited for the motor drive working as an open loop v/f controlled motor drive and as a shut loop field oriented motor controller.

Keywords : Field oriented control, floating bridge, Open End Winding Induction Machine (OEWIM), space vector.

I. INTRODUCTION

VARIOUS multi-level converter topologies have been proposed during the most recent two decades [1-4]. A few converter topologies have been researched to accomplish multi-level output voltage waveforms, among them the diode braced [3], flying capacitor [5, 6] and cell [4] converters are normally utilized. Multi-level converters have bring down dv/dt and reduced harmonics distortion alongside bring down semiconductor switchingdevice blocking voltage prerequisites, in this manner multi-level converters are beneficial in medium voltage, high power or low voltage, high frequency applications [7-9].

Among the cascaded converters, dual two-level inverter topology has received consideration because of the effortlessness of the control organize and the scheme's fault tolerant limit [10, 11]. Conventional dual two-level inverter topologies utilize two standard three-stage inverters to accomplish a multi-level voltage output. This topology does not have the neutral point vacillations found in NPC converters, utilizes less capacitors than the flying capacitor topology and requires less isolated supplies than H-bridge converters [5, 12, 13].

Besides dual inverters are more dependable, in light of the fact that in instance of a disappointment in one converter the outputs of the converter can be shortcircuited and the system would then be able to work as a standard single sided three stage inverter[14]. To accomplish multi-level voltage waveforms and to cut the way of basic mode current flow two isolated dc sources are utilized for traditionaldual inverter topology, expanding the size and weight of the system. In this paper a dual two-level inverter is displayed which lessens the size and

weight of the system for an open end winding inductionmotor drive application. Dual inverter topologies have been considered in various papers for various applications. The traditionaldual inverter topologies (utilizing two confined dc sources) has been analyzed [15-20], with various space vector modulationschemes used to create the multi-level output voltage waveforms. A blockdiagram of a conventional open stage load and converters is appeared in Fig. 1. It is conceivable to utilize a single supply for the dual inverters with a typical mode end strategy [15, 21, and 22]. These topologies utilize particular switchingcombinations that create level with normal mode voltages which cross out at load terminals. A decrease in the quantity of voltage levels and lower dc transport voltage usage are the principle detriments of this variety of the topology.

A modulationtechnique to adjust the power flow between the two inverters in a dual inverter system has too been proposed [23-27]. This topology still uses aisolation transformer; the extent of this transformer can be decreased at the cost of decreased modulationindex. The floating capacitor bridge topology alongside a reasonable control scheme to permit the supply of receptive power was presented in [28]. Different creators [29, 30] have displayed strategies to make up for supply voltage droop so as to keep the drive operational in steady power mode. This topology utilizes a floating capacitor extension to balance the voltage droop in fast machines.

In this paper, a circuit topology is investigated which is utilized as a three-level open end winding inductionmotor drive. This topology utilizes dual inverters with just a single DC voltage source at the essential side of the converter. The secondbridge converter is associated with a floating capacitor bank.

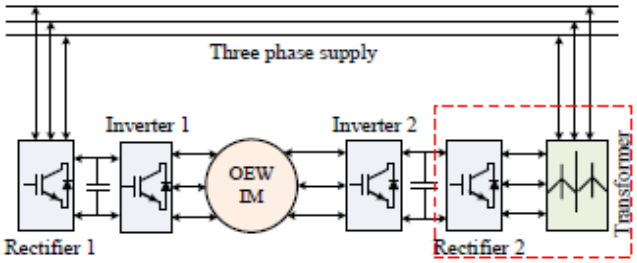

Fig. 1. Conventional open end winding IM drive topology.

The point of this topology is to dispense with the necessity for a massive isolation transformer while accomplishing multi-level output voltage waveforms. The voltage over the floating capacitor bank is controlled utilizing the excess switching vectors alongside an altered SVM conspire which stays away from undesirable voltage levels in the stage voltage waveforms during the dead-time interims, in this manner enhancing the by and large waveform quality.

II. PROPOSED SYSTEM

A. Floating capacitor bridge inverter

The floating extension capacitor dual inverter based topology has been analyzed for various applications [28, 31]. The topology can be utilized to supply reactive energy to a machine and to make up for any supply voltage droop [28, 32], however the likelihood of multi-level output voltage waveforms were not considered. A control scheme to charge the floating capacitor bridge alongside multi-level output voltage waveforms has been exhibited [33-35]. In this technique the fundamental converter works in six stage mode and the floating converter is called molding inverter as it is enhancing the waveform quality.

The work depicted in this paper is to control the voltage over the floating inverter bridge capacitor utilizing the repetitive switching states, consequently expelling the requirement for any separation

transformer and enabling the converter to accomplish multi-level output voltage waveforms. Fig. 2 appears a blockdiagram of the dual inverter with a floating bridge what's more, related capacitor. The utilization of a dc interface voltage proportion of 2:1 enables the dualbridge inverter to deliver up to a three levels in the output voltage waveform [36, 37]. The power phase of the proposed topology is appeared in Fig.3.

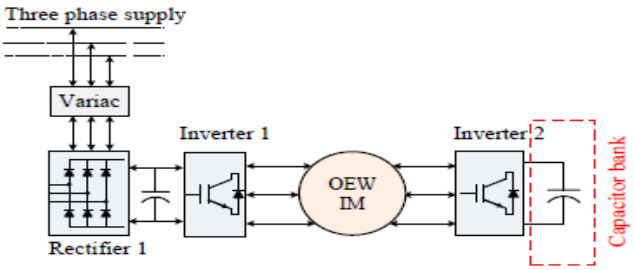

Fig. 2. Block diagram of proposed floating bridge topology.

B. Principles of operation

Keeping in mind the end goal to indicate how the floating capacitor can be charged and released the conceivable switching states are examined. The space vector outline for the topology is appeared in Fig.4, which is determined by accepting that both converters as being provided from separated DC sources with a voltage proportion of 2:1. In Fig.4 the red numbered switchingcombinations release the floating capacitor, while the green numbered switchingcombinations charge the floating capacitor. The blue numbered switchingcombinations hold the last condition of capacitor and are subsequently unbiased in wording of the condition of charge of the floating capacitor. As an illustration state (74) appeared in Fig.5 gives the switching successions for both converter's best switches 7 (1) represents to the best three switches for primary inverter and 4 (0 1 1) represents to the switching states for top three switches of the floating converter.

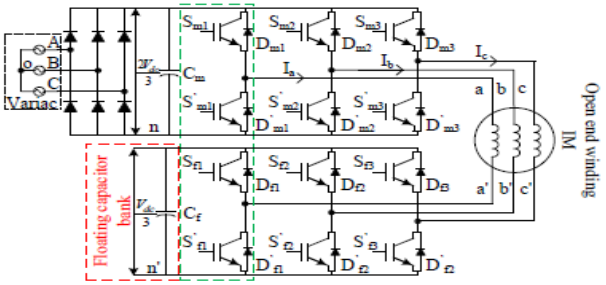

Fig. 3. Power stage of the floating bridge topology (the floating capacitor is charged to half of the main DC link voltage).

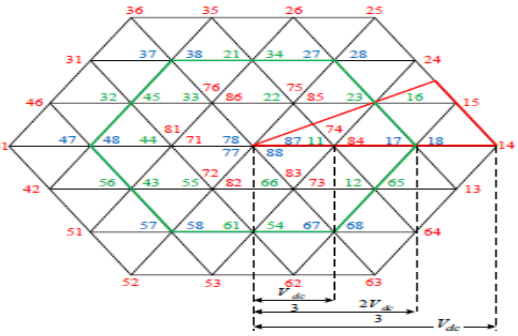

Fig. 4. Space vector of dual two-level inverter (source ratio 2:1).

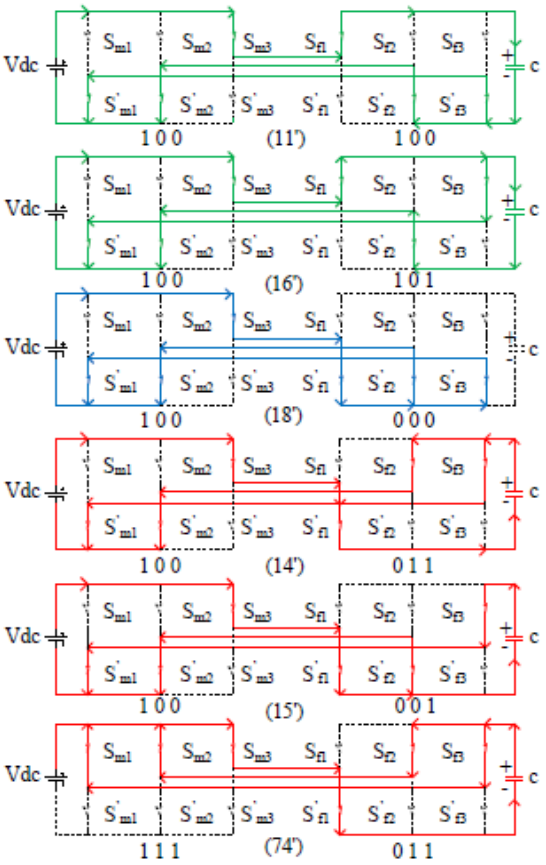

Fig. 5. Current flow for different switching state.

It can be seen from the Fig. 5 that combinations (11) and (16) will guide the current through the positive to negative terminal of the floating capacitor along these lines will act to charge the capacitor. Mixes (14), (15) and (74) will bring about a current the other way and will consequently act to release the capacitor. Mixes finishing with 7 (111) or, on the other hand 8 (000) are zero states and will in this manner have no effect of floating capacitor's voltage. It is apparent from Fig. 4 that if the reference voltage is in external hexagon at that point there are as it were two switching mixes in every area to charge the floating capacitor. Duringinductive load operation capacitor release rate will be slower and will cause cheating if the reference voltage lies in external hexagon. Additionally, because of need of charging states, the floating capacitor will release if the machine is drawing dynamic power. To maintain a strategic distance from these two marvel a limitation must be forced on modulation record. Subsequently the most extreme useable number voltage levels over the load will be diminished to nine (thirteen for detached sources) alongside a somewhat lower than perfect DC transport voltage use. In this manner the floating capacitor can charge to half of the primary DC bridge capacitor voltage just if the balance record (m) is constrained as appeared in condition (1).

$$m=0.66 \qquad (1)$$

This is 33% diminishment of DC transport use conversely with a dual inverter provided by two disengaged sources. The dual inverter with a zero arrangement disposal method moreover utilizes single supply with 15% diminishment in DC transport use what's more, can accomplish five-level voltage over the load [21].

C. Modulation system

A decoupled space vector modulation system has been utilized for this dual inverter floating bridge topology. Switchingcombinations are chosen such that the normal produced voltage for each of the converters is 180 degree stage moved from the other [Fig.6 (a)]. These voltages will then include at load terminal to coordinate in general voltage reference [Fig.6 (b)]. Recognizable proof of the subsectors, abide time estimation and the switching succession outline can be found in [38, 39].To accomplish better outcomes, the outputswitching successions are adjusted. The change of the pulses is important to limit the undesirable voltage levels because of dead-time interims in each stage leg [40, 41]. In general, the output voltage of a converter is administered by load current during dead-time interims and the voltage is equivalent to one of the voltage levels earlier or after the dead-time interims. The dual inverter with unequal voltage sources will demonstrate an alternate trademark, rather than bracing the output voltage to one of the voltage levels earlier or after the dead-time interim voltage levels, it braces the output voltage to some other voltage levels. This is valid for synchronous switching for each stage legs of the converters.

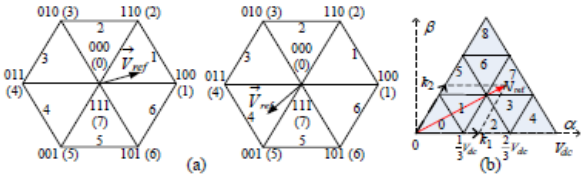

Fig. 6. (a) Space vector diagram of individual converter (not in scale). (b) Space vector diagram of the dual inverter system with source ratio of 2:1.

For an illustration, consider stage legs inside green specked line in Fig. 3 for positive load (current flowing frommain to floating converter). In the event that the best switches of the legs (S_{m1} and S_{f1}) are on then the load current will experience switch Sm1 and diode Df1. Presently, if the two legs go to its dead-time in the meantime the load current will alter cascaded what's more, will experience diode D' m1 and diode D_{f1}. At long last when both the converter legs base switches (S'_{m1} and S'_{f1}) turned on current will

experience diode D' m1and switch S'fi. It is clear that during dead-time interim, voltage level is unique to the voltage levels previously, then after the fact the dead-time interim.

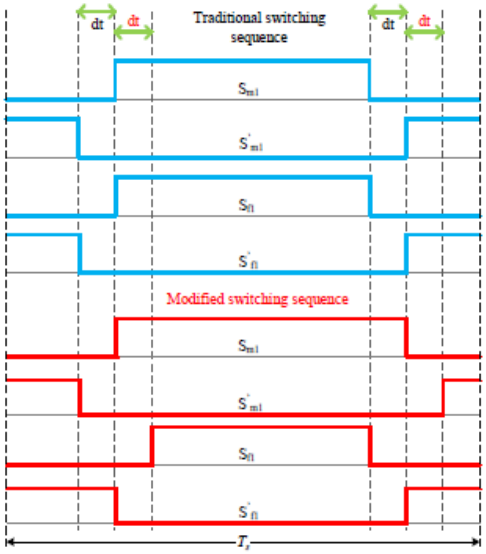

Fig. 7. Delayed dead-time intervals in both converters when current direction is positive.

To keep away from this undesirable voltage level, in this situation, the primary converter leg will go into its dead-time first and after that second converter will go to its dead-time interim when the fundamental converter relaxes interim. A summed up arrangement is appeared in Fig. 7 for positive load current. It can be seen from the Fig. 7 that the pulses are postponed relying upon the switching states advances. Table I demonstrates the summed up answer for positive and negative loadflows to stay away from the undesirable voltage levels.

Because of the modified switching groupings, the current bearing does not changeduring the dead-time. The condition of the floating capacitor will rely upon the current just some time recently the event of dead-time interim. For instance, if the capacitor was charging then it will continue charging when the converter is in dead-day and age. The estimation of dead-time is too little for the any cheat or release to change the capacitor voltage definitely.

TABLE I

DELAY TIME DEPENDING ON CURRENT DIRECTION

	Inv-1 Top	Inv-1 Bot	Inv-2 Top	Inv-2 Bot
I > 0	Turn off	Turn on	Turn on	Turn off
I < 0	Turn on	Turn off	Turn off	Turn on

III. FUZZY LOGIC

Fuzzy logic is a complex scientific strategy that permits taking care of troublesome reproduced issues with many sources of info and yield factors. Fuzzy logic can give brings about the type of suggestion for a particular interim of yield state, so it is basic that this scientific technique is entirely recognized from the more natural logics, for example, Boolean polynomial math. This paper contains a fundamental outline of the standards of Fuzzy logic. The Fuzzy logic investigation and control techniques appeared in Figure 3 can be depicted as:

1. Receiving one or vast number of estimations or other appraisal of conditions existing in some framework that will be broke down or controlled.
2. Processing every got contribution as per human based, Fuzzy "assuming at that point" rules, which can be communicated in straightforward dialect words, and joined with conventional non-Fuzzy handling.

Averaging and weighting the outcomes from all the individual tenets into one single yield choice or flag which chooses or instructs a controlled framework what to do. The outcome yield flag is an exact defuzzified esteem.

In FLC, fundamental control activity is dictated by an arrangement of semantic principles. These tenets are dictated by the framework. Since the numerical factors are changed over into etymological factors, scientific demonstrating of the framework is not required in FC..

The FLC involves three sections: fuzzification, obstruction motor and defuzzification. The FC is portrayed as I. seven fuzzy sets for each info and yield. ii. Triangular enrollment capacities for effortlessness. iii. Fuzzification utilizing nonstop universe of talk. iv. Suggestion utilizing Mamdani's, "min" administrator. v. Defuzzification utilizing the tallness technique.

III. SIMULATION RESULTS

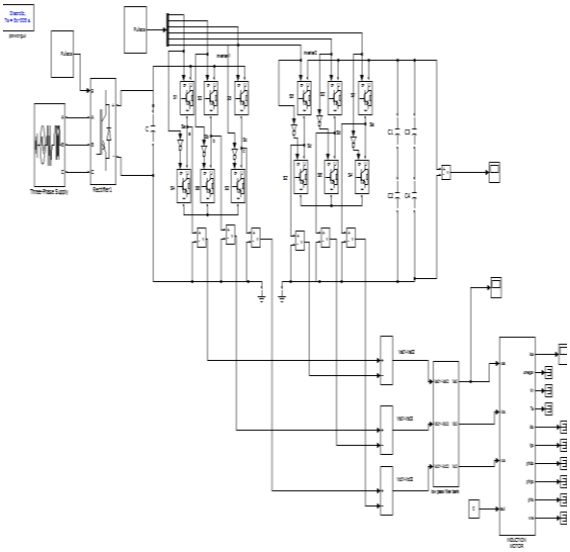

Fig. 8. Open loop v/f control IM drive Top to bottom: Simulink Model

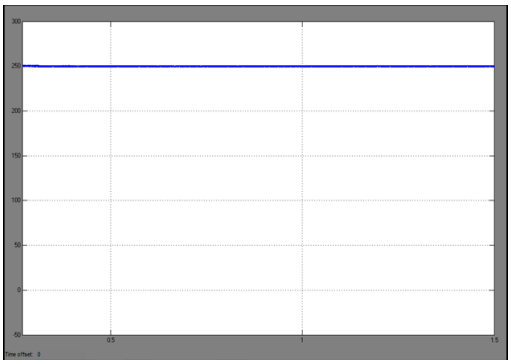

Fig. 9. Open loop v/f control IM drive Top to bottom: Floating DC link Voltage

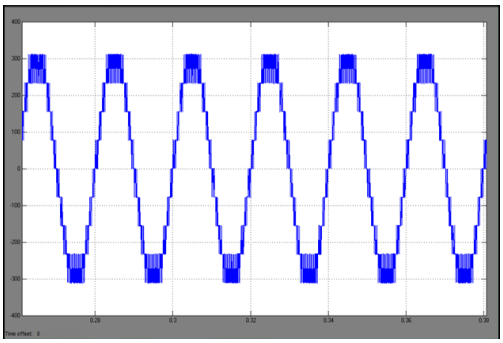

Fig. 10. Open loop v/f control IM drive Top to bottom: Phase Voltage

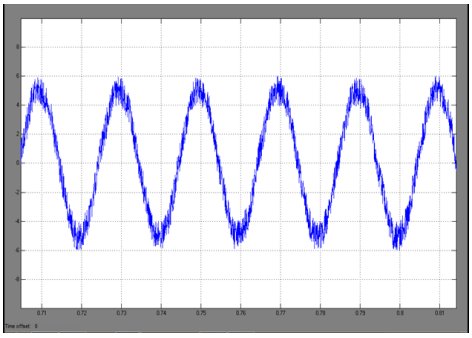

Fig. 11. Open loop v/f control IM drive Top to bottom: Phase current

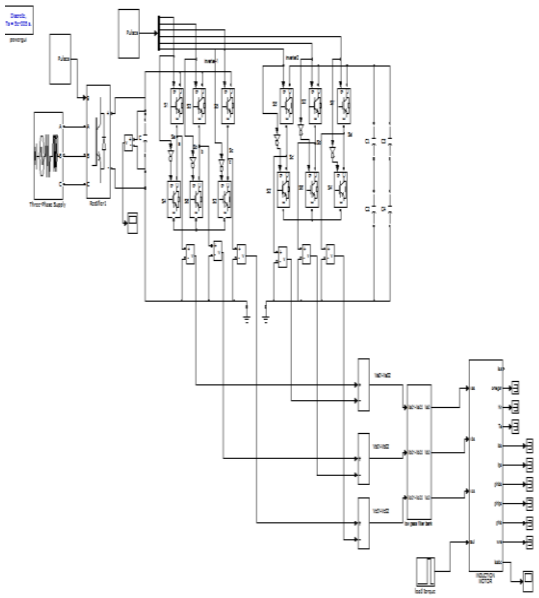

Fig. 12. Open loop v/f control IM drive Top to bottom: Simulink Model

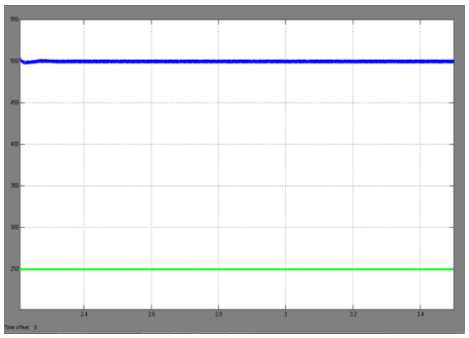

Fig. 13. Open loop v/f control IM drive Top to bottom: Main DC link Voltage (Blue) and Floating Dc Link voltage (Green)

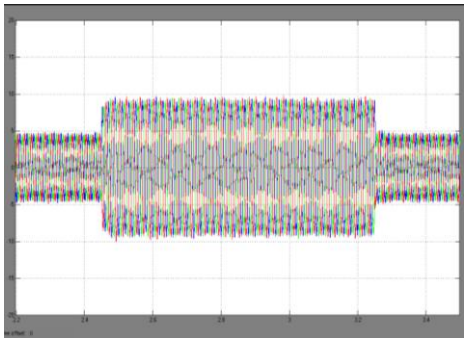

Fig. 14. Open loop v/f control IM drive Top to bottom: Three Phase current

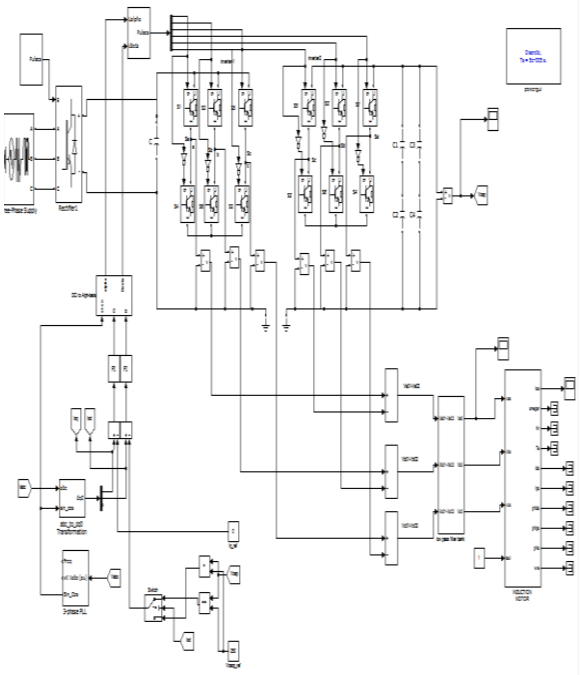

Fig. 15. Vector control when machine is loaded. Top to bottom: Simulink Model

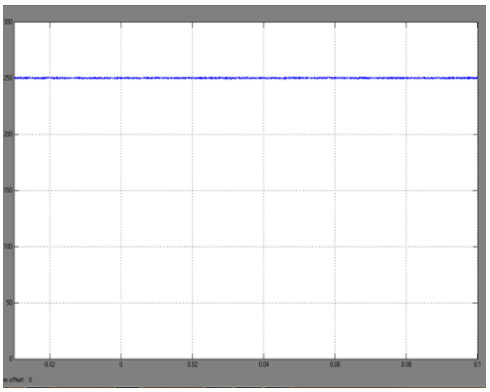

Fig. 16. Vector control when machine is loaded. Top to bottom: Floating DC link Voltage

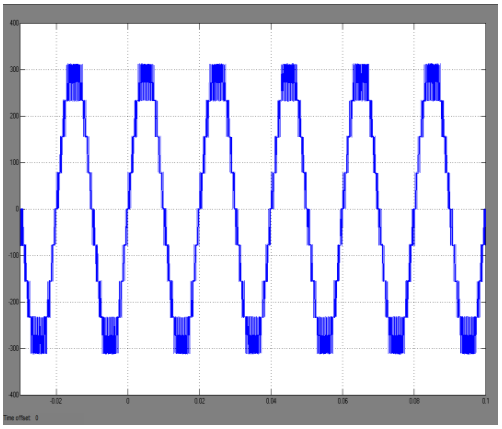

Fig. 17. Vector control when machine is loaded. Top to bottom: : Phase Voltage

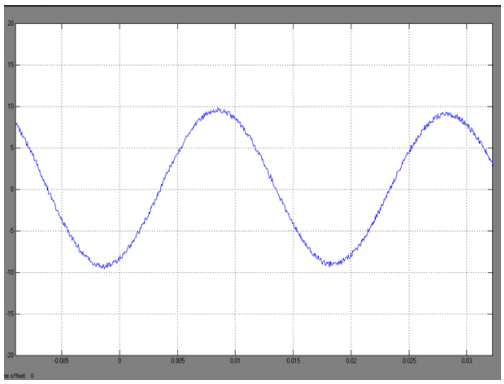

Fig. 18. Vector control when machine is loaded. Top to bottom: Phase current

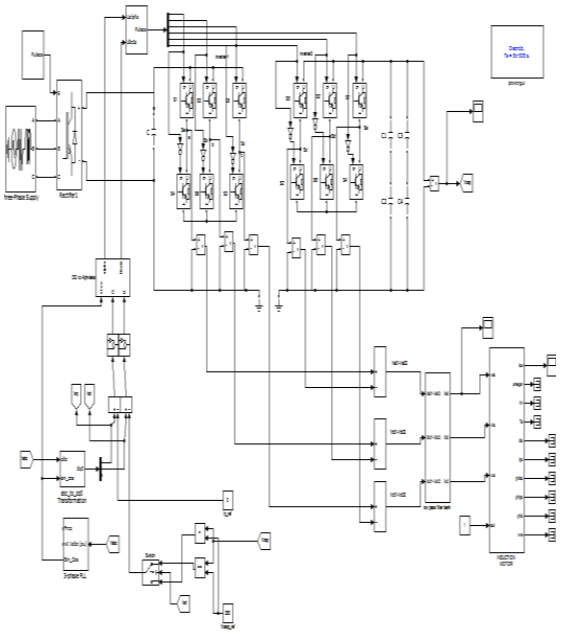

Fig 19. Extension Simulink Model

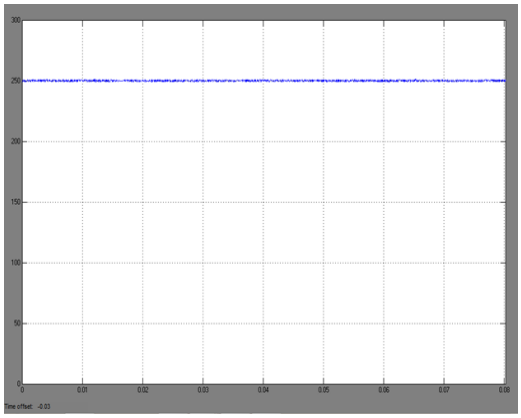

Fig 20. Extension: Floating DC link Voltage

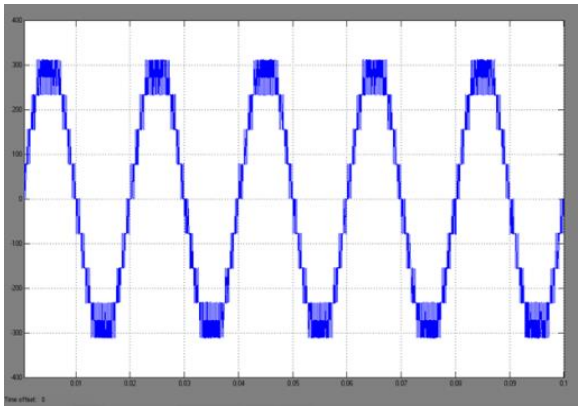

Fig 21. Extension: Phase Voltage

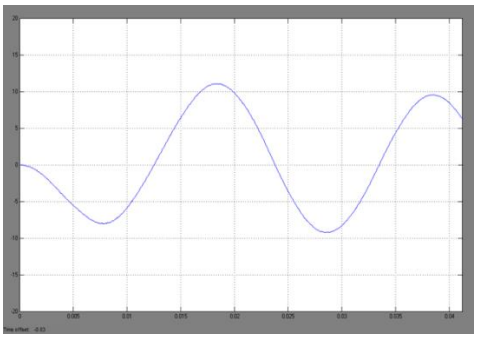

Fig 22. Extension: Phase current

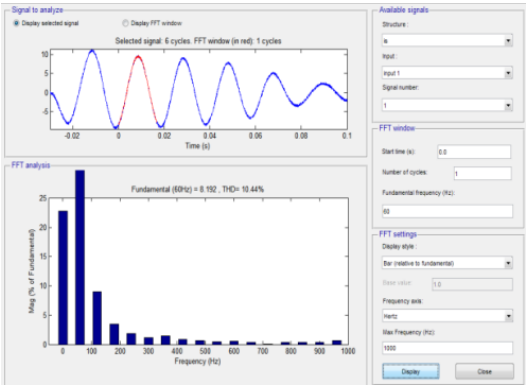

Fig 23. Vector control THD of Current Is

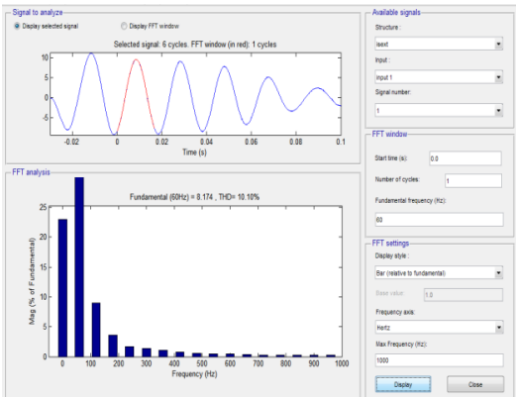

Fig 24. Extension THD of Current Is

IV. CONCLUSIONS

An motor drive utilizing open stator winding induction machine and a dualbridge inverter topology with a floating capacitor bridge has been broke down and pragmatic outcomes are illustrated. The proposed system charges the floating bridge capacitor to a proportion of 2:1 as for principle bridge DC interface voltage abundance. This specific DC bridge voltage proportion enables the converter to accomplish multi-level output voltage waveform. The floating DC interface voltage is kept at a consistent voltage by the methods for charging and releasing the floating bridge

capacitor. This is accomplished by choosing between the charging and releasing repetitive conditions of the converter. The fuzzy logic control plot has been planned and actualized in a less demanding and faster path than an established fundamental control strategy. The adjustment of recurrence deviation in a three zone interconnected system were recreated utilizing fuzzy logic controller.

A changed space vector modulation methodology is embraced to dispose of the undesirable voltage levels during the dead-time interims, in this manner enhanced the waveform quality for this floating bridge topology. An open loop v/f control drive was executed to approve the execution of the capacitor control. At last, the dynamic execution of the proposed system was assessed utilizing a nearby loop field oriented controlled motor drive, the outcomes demonstrated that the proposed topology accomplishes multi-level output voltage waveforms. The outcomes show that this topology has potential for applications where estimate, weight, losses and excess are critical, for instance in aviation, EV or HEV motor drives.

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