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Design and Implementation of High Speed Area Efficient Carry Select Adder Using Spanning Tree Adder Technique

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ABSTRACT

In this paper, we propose Carry Select Adder (CSLA) architecture with parallel prefix adder. Instead of using 4-bit Brent Kung Adder (BKA), another parallel prefix adder i.e., 4-bit spanning Tree (ST) adder is used to design CSA. Because Adders are key element in digital design, which are not only performing addition operation, but also many other function such as subtraction, multiplication and division. A Ripple Carry Adder (RCA) gives the most complicated design as-well-as longer computation time so that we may gone for parallel prefix adders. This time critical application we use Spanning tree parallel prefix adder to drive fast results but they lead to increase in area. Proposed Carry Select Adder understands between RCA and BKA in term of area and delay. Delay of Existing adders is larger therefore we have replaced those with Brent Spanning Tree parallel prefix adder which gives fast result. This paper describes comparative performance of 4-bit RCA and 4-Bit BK parallel prefix adders with Our Proposed Spanning Tree adder based carry select adder designed using Xilinx ISE tool.

Keywords : Parallel prefix adders, Spanning Tree (ST) adder, Brent Kung (BK) Adder, Carry Select Adder (CSLA)

I. INTRODUCTION

Design of less consumed area, more accurate and fastest adder logic systems is a very important aspect in the VLSI. In adders propagation of carry signal requires a more amount of time when compared with the final summation output; hence it limits the operation of an adder. One of the important components in the digital circuitry is the adder. It performs an addition operation between two operands by bit-by-bit and generates a carry and sum. The summation and carry output mainly depends upon the delay i.e. no. of transistors present in a circuit, if the circuit occupies a less no of transistors one can easily said that the circuit has less delay and more area efficient. Surprisingly this is one of the important aspects in any digital circuits. In digital circuits each and every component mainly depend upon the power and area, hence most of the circuits are made with less power and more area efficient.

In now day's scenario, Design of power-efficient high-speed logic systems in VLSI design techniques. In digital adders, the speed of addition is limited time required by the carry to generate through the adder. In present scenario, where Computations need to be performed using low-power circuit that must operate at high speed which is achievable with lesser delay that's why this paper describes

comparative performance of 4-bit RCA and 4-Bit BK parallel prefix adder designs with our proposed Parallel Prefix spanning tree adder.

Parallel Prefix Adders are one of the most important techniques to reduce area and delay of the circuit. It can take the help of a Carry Look Ahead adder. Designing of more accurate and high speed adder is called the Carry Select Adder (CSLA). To solve delay propagation problems, CSLA are used in many digital circuits. It can solve the problem by providing multiple carries and then select the proper carry to produce the final summation. The problem with the CSLA is it is not a less area consumed architecture because presence of multiple Adders for both the carries.

In CSLA architecture the summation and carry outputs are calculated for both Cin= 0 and Cin= 1. Depend upon the generated carry the summation output and their respective carry output is selected, and also with the help of a previous carry output the multiplexer (MUX) output is determined by using it as a selection input.

The conventional CSLA contains a two Ripple Carry Adders because of the availability of two RCA's in the circuit the transistor count is increases and due to this the delay also increases, this affects the performance of the circuit badly. Hence, the adder output will be delayed by a more amount of time. The main aim of this work is to design the architectures which consume less area and delay of an adder, the area can be reduced by interchanging the Ripple Carry Adders one with BK adder and another RCA with BEC add-one mechanism.

The Binary-to-Excess-1 converter (BEC) is one of the add-one schemes. The basic idea behind the BEC is it can add a binary one to the input bits and the output of BEC is given to the multiplexer and another input of the multiplexer is direct input bits. The selection of one of the input bits can be done by the multiplexer (MUX) with the help of a control signals. In modified regular linear CSLA the Ripple Carry Adder is interchanged with a Binary-to-Excess-1 (BEC) converter because of this the transistor count gradually decreases so; the area occupied by the adder is also reduced. Hence the modified regular linear CSLA gives the final summation and carry outputs within less amount of time. Obviously this is the main aim of any digital circuits.

Rest of the paper is Organization as follows: Section II describes the operation of parallel prefix adder. Section III explains the regular linear CSLA of 16-Bit Brent-Kung (BK) adder and delay evaluations. Section IV gives the idea about the proposed CSLA of 16-Bit Spanning tree adder and delay calculations. Section V explains the ST adder simulation results, both Technological and RTL schematics of Spanning Tree Adder and the performance characteristics of the Regular and Proposed CSLA. Finally the paper is concluded in Section VI.

II. PARALLEL PREFIX ADDER

Parallel Prefix Adder used to improve the speed of an addition. These are used to improve the performance of arithmetic circuits in industries due to the improved performance. The design of Parallel Prefix Adder is based upon the three steps:

- Pre-Processing stage
- Carry Generation stage
- Post Processing stage.

Pre-Processing Stage

In this stage generate and propagate signals are calculated for each and every inputs A and B. The signals for this stage are computed by using the equations:

$$P_i = A_i \text{ xor } B_i \quad (1)$$

$$G_i = A_i \text{ and } B_i \quad (2)$$

Carry Generation Stage

At this stage the carries are calculated for every bit and the entire operation at this stage is carried out parallel. At last these generated signals are bisected into smaller pieces. These signals are used as intermediate signals and computed by using the Equations 3 and 4.

$$CP_{i:j} = P_{i:k-1} \text{ and } P_{k:j} \quad (3)$$

$$CG_{i:j} = G_{i:k} \text{ or } (P_{i:k} \text{ and } G_{k-1:j}) \quad (4)$$

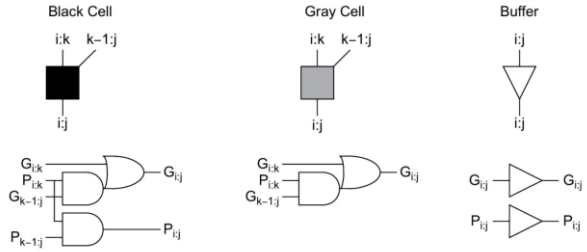

Figure 1. Various cells used within carry generation stage

Post Processing Stage

This is the last stage in the Parallel Prefix Adder which is used to calculate the total summation of each and every input bit and it is the final stage for all the adders and these are calculated by using logical Equations 5 and 6.

$$C_{i-1} = (P_i \text{and } C_{in}) \text{or } G_i \quad (5)$$

$$S_i = P_i \text{ xor } C_{i-1} \quad (6)$$

The AND, OR and Inverter (AOI) are the basic building blocks of any logic circuit. The calculation of an area is obtained by simply counting5 the no. of gates in a circuit. The AND, OR and Inverter occupies a one unit area, while the XOR gate and MUX occupies a 5 and 4 units of delay respectively.

III. EARLIER WORK DONE

In electronics, a carry-select adder is a particular way to implement an adder which is a logic element that computes the (n+1)-bit sum of two n-bit numbers.

The carry select adder includes in the category of conditional adder .Here sum and carry are calculated by assuming input carry as 0 and 1 separately which are fed to a multiplexer whose select signal is the carry out of previous stage. The conventional carry select consists of k/2 bit adder for the upper half most significant bit's (MSB) two k bit adders. This technique of dividing adder into stages increases the area utilization but also speeds up the addition operation. The block diagram of conventional k CSA adder is shown in figure below

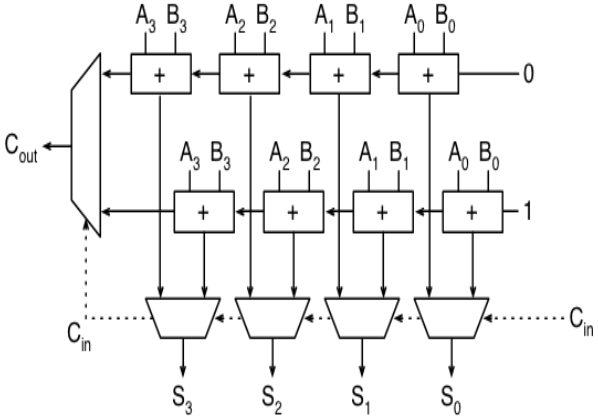

Figure 2. 4-bit Carry Select Adder

Brent-Kung adder is a very popular and widely used adder which can be used in place of the adders used in the carry select adder where carry input is fixed to zero. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders. It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent Kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders is 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Figure below

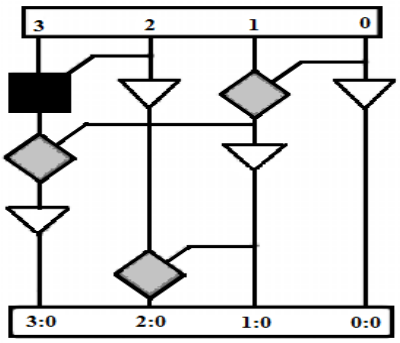

Figure 3. 4-bit Brent Kung Adder

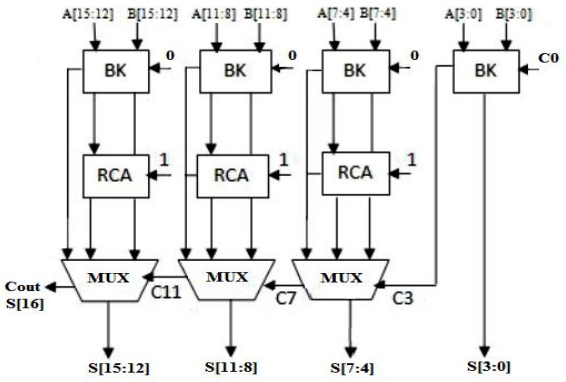

Figure 4. Carry Select adder Using Brent Kung Adder

IV. PROPOSED CARRY SAVE ADDER USING SPANNING TREE

Design of area and power efficient high speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. The CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0and Cin=1, then the final sum and carry are selected by the multiplexers (mux).

In our idea of this work is BEC instead of RCA with Cin=1 in the regular CSLA to achieve lower area and delay. The main advantage of this BEC logic comes from the less number of gate count than the n-bit Full Adder (FA) structure.

Structure of BEC Logic

The delay and area evaluation considers all gates to be made up of AND, OR and inverter. Each having delay equal to 1 unit and area equal to 1unit .Then add up the number of gates in the longest path of a logic block but contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach the CSLA adder blocks of 2:1 mux of adder(HA) and FA are evaluated the basic work is to use binary to Excess 1 converter(BEC) Instead of RCA with cin=1 in the Regular CSLA to achieve lower area and power consumption.

The main advantage of this BEC logic comes from the lesser number of logic gates than the n bit full adder structure. As stated above the main idea of this work is to use BEC instead of the RCA with cin=1 in order to reduce the area and power consumption of the Regular CSLA to replace the n bit RCA, an n+1 bit BEC is required.

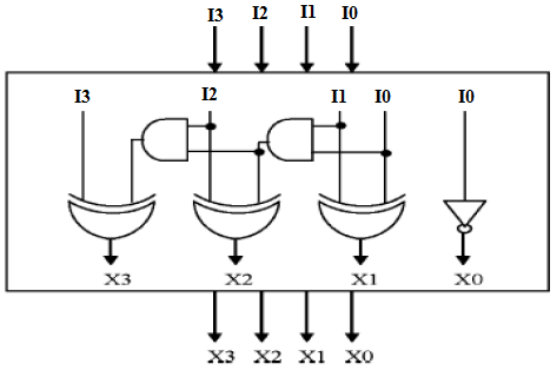

Fig. 2 4-Bit BEC

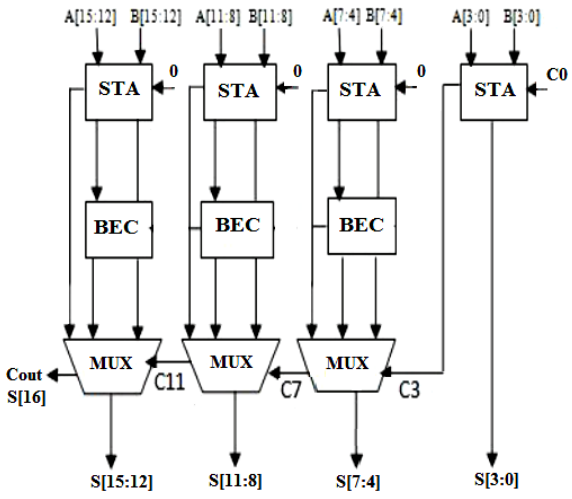

Fig. 3 Proposed 16-bit CSLA with STA

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=1 and Brent Kung adder for Cin=0 and so it consumes more area. To solve this problem add-one schemes like Binary to

Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified into spanning tree CSA in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here ripple carry adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less.

V. SIMULATION RESULTS

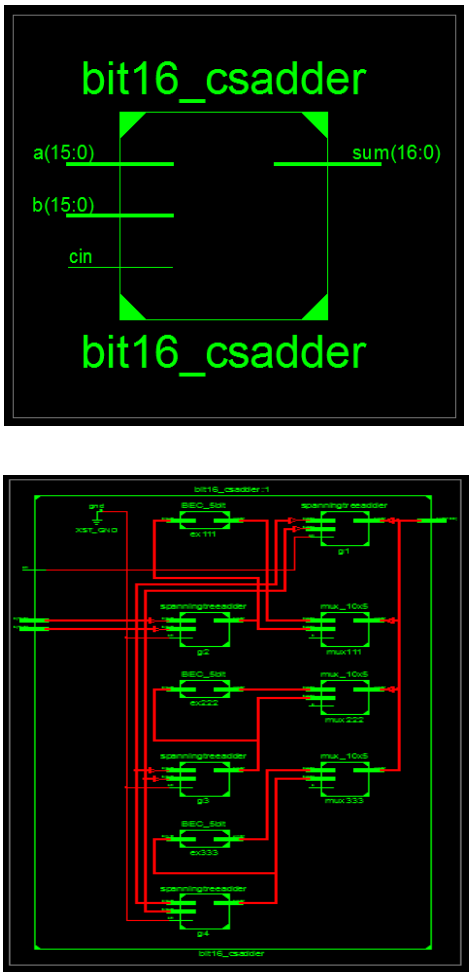

Figure 4. Block Diagram and RTL Schematic of CSA With STA

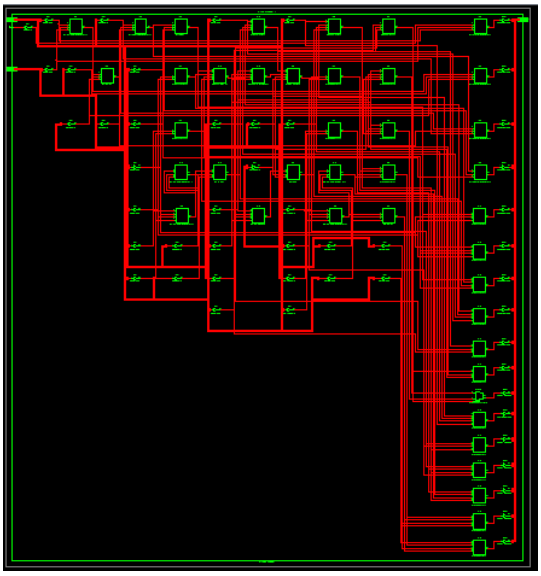

Figure 8. Technology schematic Of Proposed CSA with STA

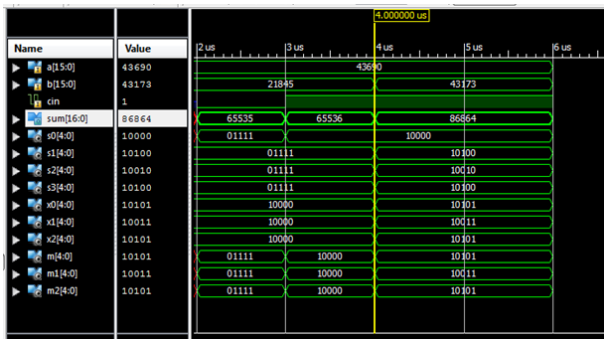

Figure 9. Simulation output of proposed CSA with STA

Table 1 Comparison of Existing CSA with Proposed CSA

Parameter	Existing system	Proposed system
Area (LUTs)	50	41
Delay (ns)	15.851	15.241

VI. CONCLUSION

This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore spanning tree adder is used. The calculated

results conclude that Spanning tree adder based Carry Select Adder is better in terms of power consumption and high speed when compared with Brent Kung adder architectures and can be used in different applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse Reponses etc.

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