

# Grid Interconnecting Solar Generation System Using Transformer Less Cascaded Seven Level Inverter

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## ABSTRACT

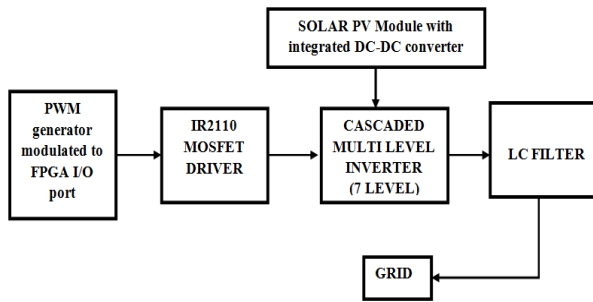
Multilevel inverter is a power electronic device that is used for high voltage and high power applications and has many advantages like, low switching stress, low total harmonic distortion (THD). Hence, the size and bulkiness of passive filters can be reduced. This paper proposes three topologies of a 7-level cascaded multilevel inverter with reduced number of switches with the 5-level cascaded multilevel inverter and 3-level inverter. The topologies consist of circuits with 9 switches for 7-level CMLI, 8 switches for the 5-level CMLI and 6 switches for the 3-level inverter. Apart from the reduction in switch count this paper also includes minimization of leakage currents and comparative analysis of levels of CMLI's in every inverter connected to PV source. The control scheme based on Sinusoidal Pulse Width Modulation (SPWM) is adopted due to its ease of implementation. More number of levels results in reduced THD and nearly sinusoidal output. Simulation is performed using Matlab/Simulink.

**Keywords :** WM (Pulse Width Modulation).Total Harmonic Distortion (THD)

## I. INTRODUCTION

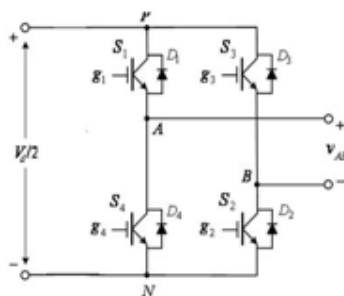
Utilization of renewable energy resources is the demand of today and the necessity of tomorrow. With advancement in power electronic technology, the solar photovoltaic energy has been recognized as an important renewable energy resource because it is clean, abundant and pollution free. The PV power supplied to the utility grid is gaining more and more visibility, while the world's power demand is Increasing [1]. Not many PV systems have so far been placed into the grid due to the Relatively high cost, compared with more traditional energy sources such as oil, gas, coal, nuclear, hydro, and wind. Solid-state inverters have been shown to be the enabling technology for putting PV systems into the grid. PV inverter, the heart of the grid connected and standalone PV system, is used to convert dc power obtained from PV modules into ac power to be fed

into the grid. Improving the output waveform of the inverter reduces its respective harmonic content and hence the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation of the inverter. In recent years, multilevel inverters have become more attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width-modulated (PWM) inverters. They offer improved output waveforms, smaller filter size, and lower EMI, lower total harmonic distortion (THD).

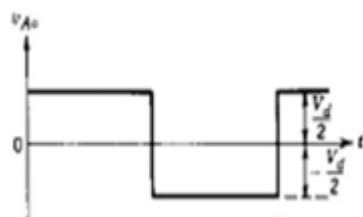


**Fig 1.** The basic schematic model of the standalone PV system.

Multilevel inverter are designed based on basic inverter model [4] which is shown in Fig.2 and its output is shown in Fig.3. Multilevel inverters can be used to interface with renewable energy and distributed energy resources because several batteries, fuel cells, PV cells, wind turbines, and micro turbines can be connected through a multilevel inverter to supply a load or the ac grid without voltage balancing problems [5]. Generally, the battery requires a large capacity transformer for connecting to the power system. As a result, the whole system becomes large, heavy and has low efficiency. Recently, a transformer less battery energy storage system based on a cascaded multilevel inverter has been proposed [6]. A cascaded multilevel inverter has a simple structure that has promoted its application at megavolt level.



**Fig.2.** Basic Inverter.



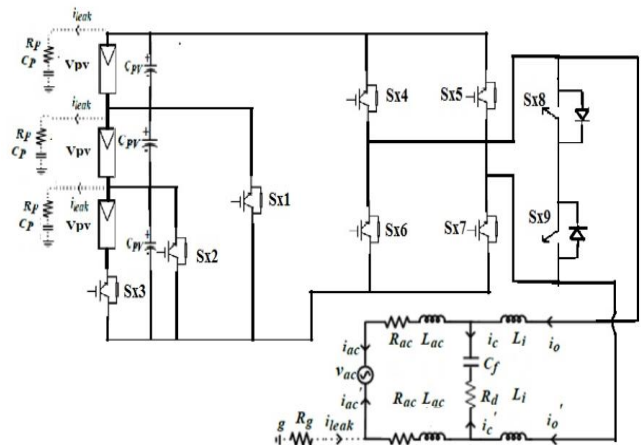
**Fig.3.** Output waveform.

In the case of minimisation of leakage currents there so many configurations were proposed all these configurations employ two methods for minimization of the leakage current [8]. One method is based on maintaining the common-mode voltage (CMV) constant, while the other method is based on the minimization of the high-frequency transitions in the terminal and common-mode voltages.

## II. METHODS AND MATERIAL

### SEVEN LEVEL MULTI LEVEL INVERTER

The 7-level multilevel inverter topology is introduced incorporating the least number of unidirectional switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. The new topology is well suited for drives and renewable energy applications. The performance quality in terms of THD and switching losses of the new MLI is compared with conventional cascaded MLI and other existing 7-level reduced switch topologies using carrier-based PWM techniques.



**Fig 4.** seven-level grid-connected CMLI with PV and parasitic elements.

Coming to the operation of seven level cascaded multilevel inverter only one switch will be

conducting at every instant and thus making the operation very simple. For example, we get output  $V_{pv}$  only when  $S_{x1}$  is conducting. The switching sequence for different voltage levels is shown below in the table. Each voltage source is  $V_{pv}$ .

### OPERATION OF SEVEN LEVEL CASCADED FIVE-LEVEL MLI

The schematic circuit diagram of the proposed five-level CMLI for PV system is shown in Fig. 1. The given configuration consists of two converters. Converter one is a inverter comprising three switches  $S_{x1}, S_{x2}$  and  $S_{x3}$ . The Converter2 comprises of a highly efficient and reliable inverter configuration [15] with six switches ( $S_{x4}$  to  $S_{x9}$ ). Among the six switches, four switches ( $S_{x4}$  to  $S_{x7}$ ) in Converter 2 constitute an H-bridge circuit.

The remaining two switches  $S_{x8}$  and  $S_{x9}$  in Converter-2 are bi-directional switches. The switches in the Converter-1 are used to generate the voltage levels of  $3V_{pv}, 2V_{pv}$  and  $V_{pv}$ . When switch  $S_{x1}$  is turned ON, the voltage  $V_{pv}$  is applied at the terminals of output and when switch  $S_{x2}$  ON the output voltage attains  $2V_{pv}$ . Similarly, the terminals of output attains the voltage  $3V_{pv}$  when switch  $S_{x3}$  is turned ON. The switches  $S_{x1}, S_{x2}$  and  $S_{x3}$  are complementary in nature. The generated voltage levels at the terminal n of Converter1 are given as an input to the Converter2.

The Converter-2 generates the positive, negative and zero levels of corresponding input voltage of the converter-2 to the load. The bi-directional switches  $S_{x8}$  and  $S_{x9}$  provide the free-wheeling path during zero voltage state. The output of the seven-level CMLI is connected to the grid through an LCL filter as shown in Fig. 1. It consists of inverter side inductance  $L_i$ , capacitance  $C_f$  and grid side inductance  $L_{ac}$ .

The resistance  $R_d$  in the shunt branch of the filter is used as a damping resistor. The resistance  $R_{ac}$  refers to the grid side resistance, and the resistance  $R_g$  indicates resistance in the ground path. The variable  $v_{ac}$  refers to instantaneous grid voltage. The variables  $R_p$  and  $C_p$  refer to the parasitic resistance and capacitance in the PV system, respectively shown with dotted lines.

The switching operation of the seven level CMLI is shown in the table.

$S_{x1}$	$S_{x2}$	$S_{x3}$	$S_{x4}$	$S_{x5}$	$S_{x6}$	$S_{x7}$	$S_{x8}$	$S_{x9}$	Output Voltage
1	0	0	1	0	0	1	1	0	$+V_{pv}$
0	1	0	1	0	0	1	1	0	$+2V_{pv}$
0	0	1	1	0	0	1	1	0	$+3V_{pv}$
1	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0
1	0	0	0	1	1	0	0	1	$-V_{pv}$
0	1	0	0	1	1	0	0	1	$-2V_{pv}$
0	0	1	0	1	1	0	0	1	$-3V_{pv}$

Table 1. switching states for 7- level CMLI with their respective output voltage

From the table 1. The output voltage of the 7- level CMLI getting as  $\pm 3V_{pv}$ ,  $\pm 2V_{pv}$ ,  $\pm V_{pv}$ . These output can be expressed in terms of equations as

$$V_1 = S_{x3} (S_{x4} * S_{x7} - S_{x5} * S_{x6}) (3V_{pv}) \dots(1)$$

$$V_2 = S_{x2} (S_{x4} * S_{x7} - S_{x5} * S_{x6}) (2V_{pv}) \dots(2)$$

$$V_3 = S_{x1} (S_{x4} * S_{x7} - S_{x5} * S_{x6}) (V_{pv}) \dots(3)$$

And the resultant output voltage

$$V = V_1 + V_2 + V_3$$

From (1),(2) and (3)

$$V = (S_{x3})(S_{x4} * S_{x7} - S_{x5} * S_{x6})(3V_{pv}) + (S_{x2})(S_{x4} * S_{x7} - S_{x5} * S_{x6})(2V_{pv}) +$$

$$(S_{x1})(S_{x4} * S_{x7} - S_{x5} * S_{x6})(V_{pv}) \dots (4)$$

From equation (4),

Whenever  $S_{x4}, S_{x7}$  were ON and if  $S_{x3}$  ON  $+3V_{pv}$  as output voltage, if  $S_{x2}$  ON  $+2V_{pv}$  and if  $S_{x1}$  ON  $+V_{pv}$  as output voltages.

Similarly,

whenever  $S_{x5}, S_{x6}$  ON and if  $S_{x3}$  ON  $-3V_{pv}$  as output voltage, if  $S_{x2}$  ON  $-2V_{pv}$  and if  $S_{x1}$  ON  $-V_{pv}$  as output voltages.

Coming to the minimization of leakage current in the cascaded seven level multi level inverter is achieve by making common mode voltage of the cascaded multi level inverter constant.

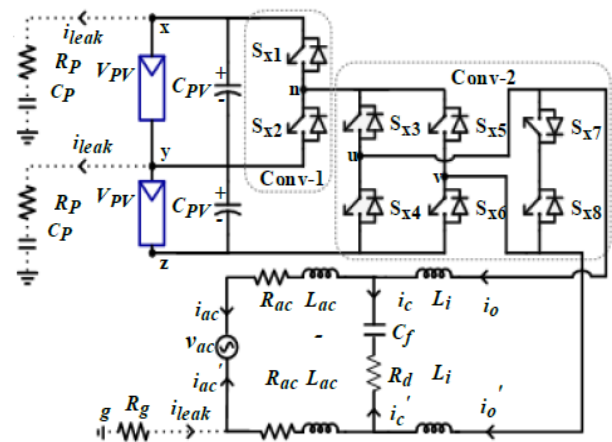
## 5-LEVEL CASCADED MULTI LEVEL INVERTER

The generalized topology for  $2m+1$  levels can also be obtained for the proposed five-level CMLI. The number of PV sources in CMLI is denoted by the term  $m$ . The value of  $m$  is always an integral multiple of 2 (i.e.,  $m = 2, 4, \dots$ ). The extended version of the proposed CMLI for  $2m+1$  levels is presented in Fig. 4. The generalized topology is obtained by cascading the basic units consisting of half-bridge and H-bridge. The bi-directional switches are connected in between the output terminals for the free-wheeling period.

The schematic circuit diagram of the proposed five-level CMLI for PV system is shown in Fig. 1. The given configuration consists of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter comprising two switches  $S_{x1}$  and  $S_{x2}$ . The Conv-2 comprises of a highly efficient and reliable inverter configuration [15] with six switches ( $S_{x3}$  to  $S_{x8}$ ).

The schematic circuit diagram of the proposed five-level CMLI for PV system is shown in Fig. 1. The given configuration consists of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter comprising two switches  $S_{x1}$  and  $S_{x2}$ . The Conv-2

comprises of a highly efficient and reliable inverter configuration [15] with six switches ( $S_{x3}$  to  $S_{x8}$ ).



**Fig.5.** five-level grid-connected CMLI with PV and parasitic elements.

Among the six switches, four switches ( $S_{x3}$  to  $S_{x6}$ ) in Conv-2 constitute an H-bridge circuit. The remaining two switches  $S_{x7}$  and  $S_{x8}$  in Conv-2 are bi-directional switches. The switches in the Conv-1 are used to generate the voltage levels of  $V_{pv}$  and  $V_{pv}/2$ . When switch  $S_{x1}$  is turned ON, the voltage  $V_{pv}$  is applied at the terminal  $n$  with respect to the terminal  $z$ . Similarly, the terminal  $n$  attains the voltage  $V_{pv}/2$  when switch  $S_{x2}$  is turned ON.

The switches  $S_{x1}$  and  $S_{x2}$  are complementary in nature. The generated voltage levels at the terminal  $n$  of Conv-1 are given as an input to the Conv-2. The Conv-2 generates the positive, negative and zero levels of corresponding input voltage (voltage between the terminals  $n$  and  $z$ ) across the load.

$S_{x1}$	$S_{x2}$	$S_{x3}$	$S_{x4}$	$S_{x5}$	$S_{x6}$	$S_{x7}$	$S_{x8}$	$V_{out}$
1	0	1	0	0	1	1	0	$+2V_{pv}$
0	1	1	0	0	1	1	0	$+V_{pv}$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{pv}$
1	0	0	1	1	0	0	1	$-2V_{pv}$

Table 2. switching states for 5- level CMLI with their respective output voltage

The cascaded multilevel inverter uses set of series connected full-bridge inverters with separate DC sources in a modular setup to create the stepped waveform. A full bridge inverter is in itself a 3 level cascaded multilevel inverter and every module added in cascade to that extends the inverter with two more voltage levels, which then increases the number of steps in the waveform. The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output Waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated.

From the table 2. The output voltage of the 7- level CMLI getting as +/- 2PV, +/-PV. These output can be expressed in terms of equations as

$$V1 = Sx1( Sx3 * Sx6 - Sx4 * Sx5 )( 2Vpv) .....(5)$$

$$V2 = Sx2 ( Sx3 * Sx6 - Sx4 * Sx5 )(Vpv).....(6)$$

And the resultant output voltage

$$V = V1 + V2$$

From (5),(6)

$$V = Sx1( Sx3 * Sx6 - Sx4 * Sx5 )( 2Vpv) + Sx2 ( Sx3 * Sx6 - Sx4 * Sx5 )(Vpv) ....(7)$$

From equation (7),

Whenever Sx3,Sx6 were ON and if Sx1 ON +2Vpv as output voltage and if Sx2 ON +Vpv as output voltages.

Similarly,

whenever Sx4,Sx5 were ON and if Sx1 ON -2Vpv as output voltage and if Sx2 ON -Vpv as output voltages.

### 3-LEVEL INVERTER

The 3 level inverter is like the basic full bridge inverter, having the pulses from the PWM technique. The pulses were generated as per the output requirement. The inverter connected to grid from the PV source. PV source gives constant DC to the inverter and inverter converts DC to AC and connected to grid. The basic circuit diagram for the 3 level inverter connected to the grid from the PV source. The switching operations for the 3 level inverter is given in the table 3. There are 6 switches in 3-level inverter. The two switches (Sx1,Sx4) operated at one instant i.e. for positive output and another two switches (Sx2,Sx3) operate for the negative output. The bi-directional switches Sx5 and Sx6 provide the free-wheeling path during zero voltage state.

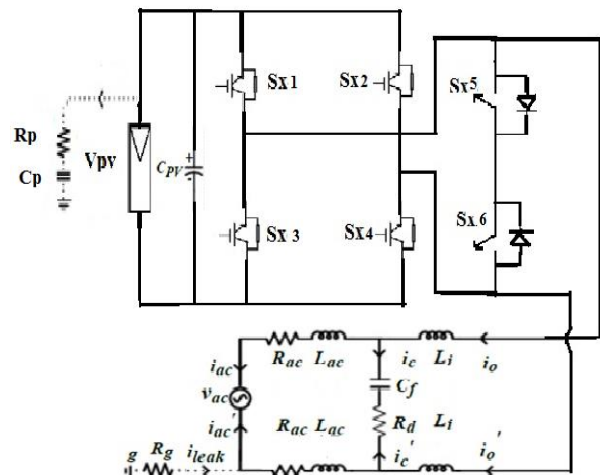


Fig. 6. Three-level grid-connected Inverter with PV and parasitic elements.

Sx1	Sx2	Sx3	Sx4	Sx5	Sx6	Output voltage
1	0	0	1	1	0	+V <sub>pv</sub>
0	0	0	0	1	0	0
0	0	0	0	0	1	0
0	1	1	0	0	1	-V <sub>pv</sub>

Table 3. switching states for 3 level inverter with their respective output voltage.

From the table 3. The output voltage of the 3- level CMLI getting as +/-PV. These output can be expressed in terms of equations as

$$V1 = Sx1 * Sx4 \quad \dots \dots (8)$$

$$V2 = Sx2 * Sx3 \quad \dots \dots (9)$$

And the resultant output voltage

$$V = V1 + V2$$

From (8),(9)

$$V = Sx1 * Sx4 - Sx2 * Sx3 \quad \dots \dots (10)$$

Whenever Sx1,Sx4 were ON +V<sub>pv</sub> as output voltages. Similarly,

Whenever Sx2,Sx3 were ON, -V<sub>pv</sub> as output voltages.

### III. SIMULATION RESULTS

The simulation results includes comparison of the three different inverters connected by PV panels and supplied to grid. It also consists comparison of the three different inverters with their levels of output, leakage current and THD of the grid current by using MATLAB/SIMULINK software.

#### Cascaded Seven level Inverter

The simulation model of Reduced Switches Cascaded 7- level MLI of designed using MATLAB/SIMULINK

Software. The gating signals for the inverter are generated by using multicarrier modulation technique. The circuit was simulated with grid connected to CMLI., Here in this section simulation results and observations of Photovoltaic Application based 7- level Cascaded MLI with Reduced No. of Switches is presented. The different parameters (like voltage, current, THD) are observed.

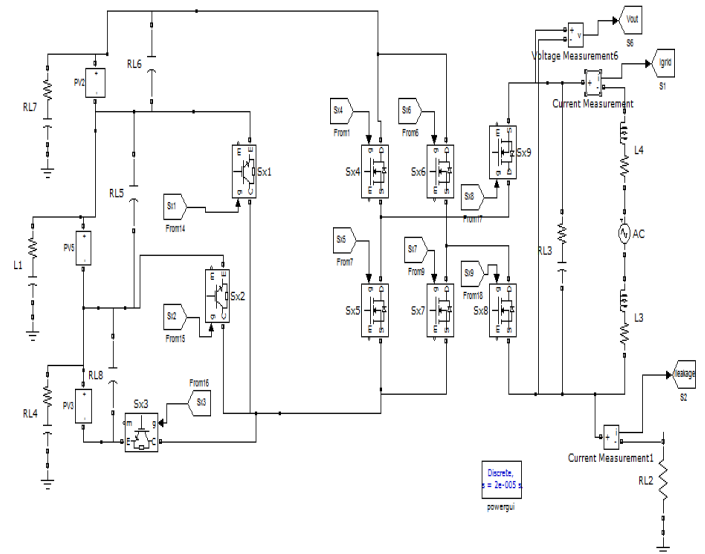


Fig 7. MATLAB Model of Photovoltaic based 7- level Cascaded MLI with reduced no. of switches.

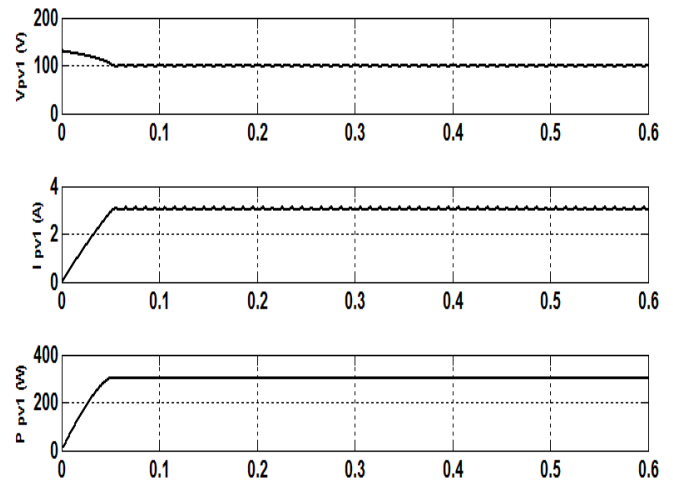
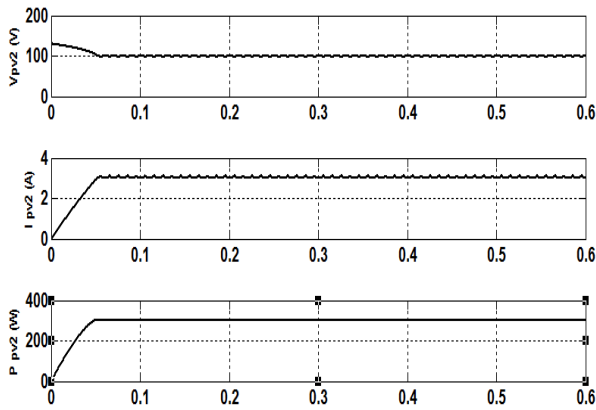
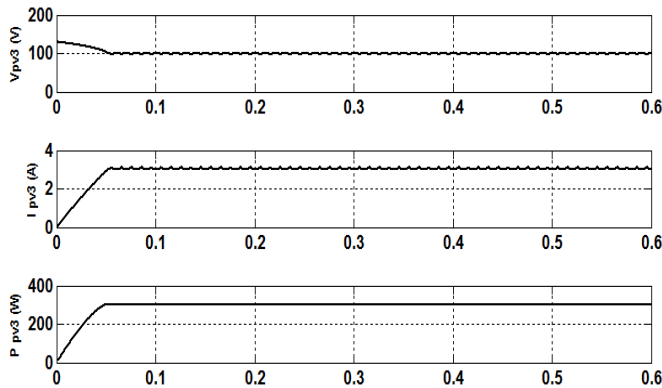


Fig 8. Simulation waveforms of the PV Panel 1 Voltage (V), Current (A), and Power (W).





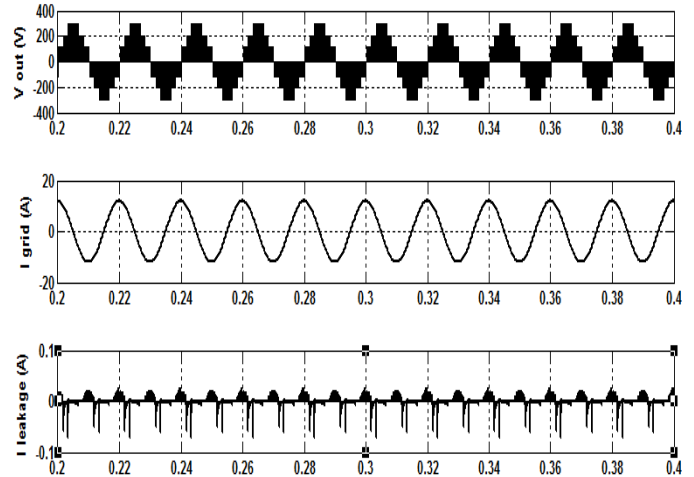
**Fig 9.** Simulation waveforms of the PV Panel 2  
Voltage (V), Current (A), and Power (W).



**Fig.10.** Simulation waveforms of the PV Panel 3  
Voltage (V), Current (A), and Power (W).

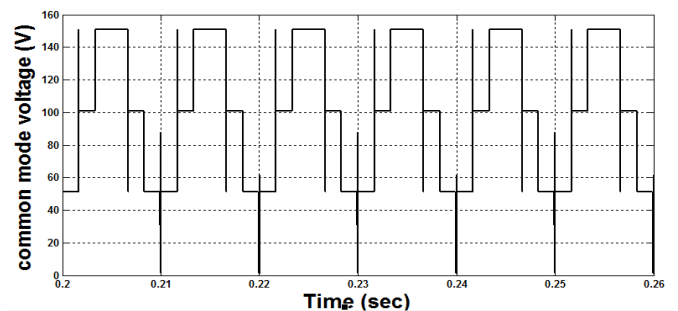
The input parameters of the seven level cascaded multilevel inverter is taken as the three PV sources with each of 100 volts as the PV voltages and power as 300 watts each. The output voltage obtained by the seven level cascaded multi level inverter is three stepped wave form with the peak of 300 volts. The inverter connected to grid and the grid current is nearly 10 amperes, coming to the leakage current the frequency of common mode voltage is reduced by the sinusoidal pulse width modulation technique and if frequency of the common mode voltage reduced then the leakage current reduced. The leakage current of the seven level cascaded multi level inverter is below the 0.1 amp i.e. 0.08 amps. The THD of the seven level multi level inverter is 0.07%.

In the case of the leakage current minimization of seven level inverter, there is a variation in the common mode voltage but it is in the constant range of variation i.e. it is in between 100 and 200. The leakage current will appear in the variation in the common mode voltage.



**Fig 11.** Simulation waveforms of the seven level CMLI Output Voltage (V), Grid Current (A) and Leakage Current (A).

Coming to the minimization of leakage current in the seven level inverter is achieve by the common mode voltage to constant value. The common mode voltage waveform is shown in the below figure 12.



**Fig 12.** The common mode voltage of the cascaded seven level inverter.

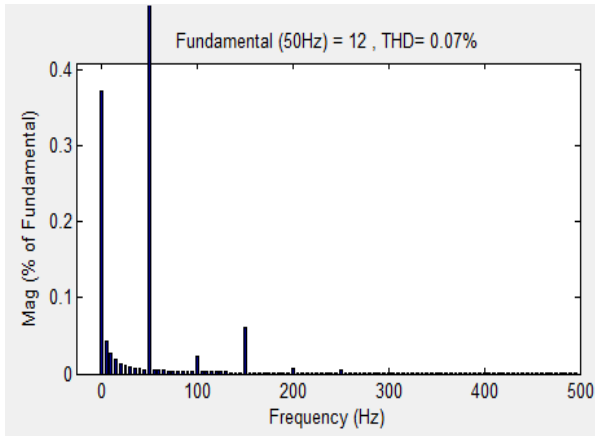


Fig 13. Total Harmonic Distortion of seven level inverter Output Current in %

### Cascaded 5 – Level Inverter

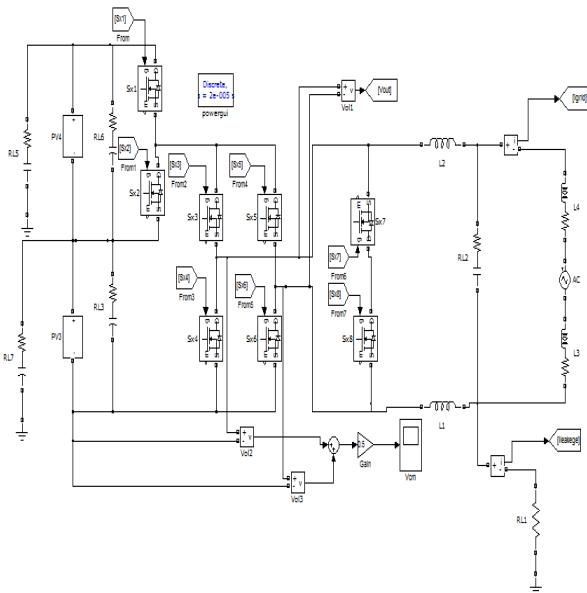


Fig 14 : MATLAB Model of Photovoltaic based 5-level Cascaded MLI with reduced no. of switches.

The input parameters of the five level cascaded multilevel inverter is taken as the three PV sources with each of 200 volts as the PV voltages and power as 1000 watts each. The output voltage obtained by the five level cascaded multi level inverter is three stepped wave form with the peak of 400 volts. The inverter connected to grid and the grid current is nearly 5 amperes, coming to the leakage current the frequency of common mode voltage is reduced by the sinusoidal pulse width modulation technique and if frequency of the common mode voltage reduced then

the leakage current reduced. The leakage current of the five level cascaded multi level inverter is 0.15 amps. The THD of the five level cascaded multi level inverter is 1.29%.

In the case of the leakage current minimization of five level inverter, there is a variation in the common mode voltage but it is in the constant range of variation i.e. it is in between 100 and 200. The leakage current will appear in the variation in the common mode voltage.

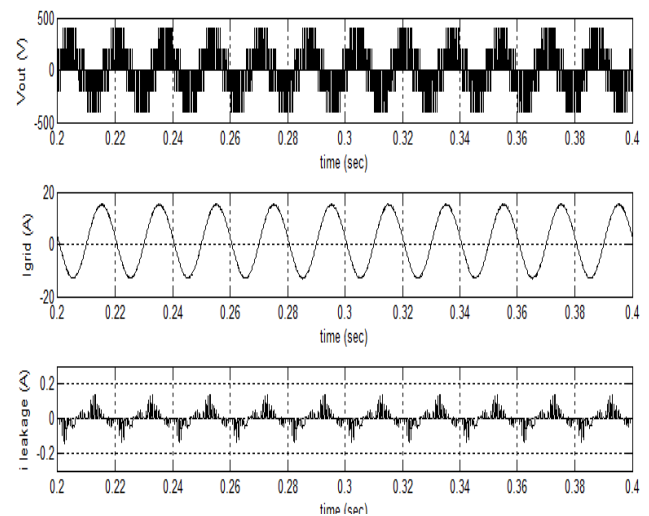


Fig 15. Simulation waveforms of the Five level CMLI Output Voltage (V), Grid Current (A) and Leakage Current (A).

Coming to the minimization of leakage current in the cascaded five level inverter is achieved by the common mode voltage to constant value. The common mode voltage waveform is shown in the below figure 16.

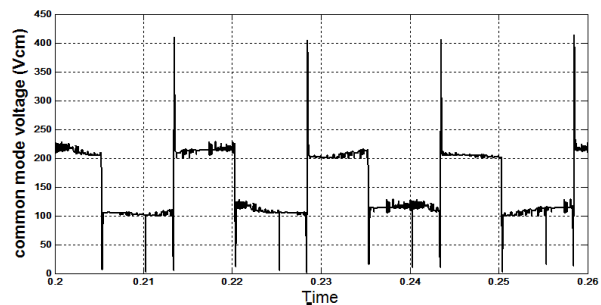
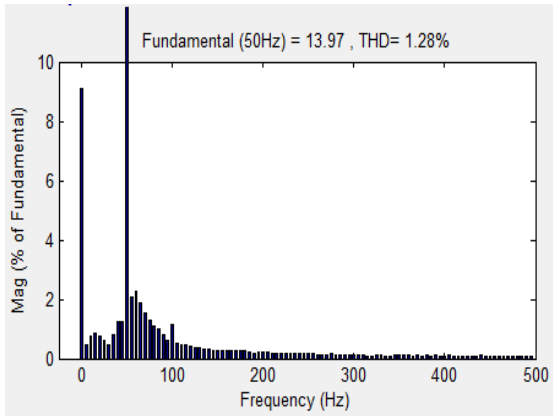


Fig 16. The common mode voltage of the cascaded five level inverter.

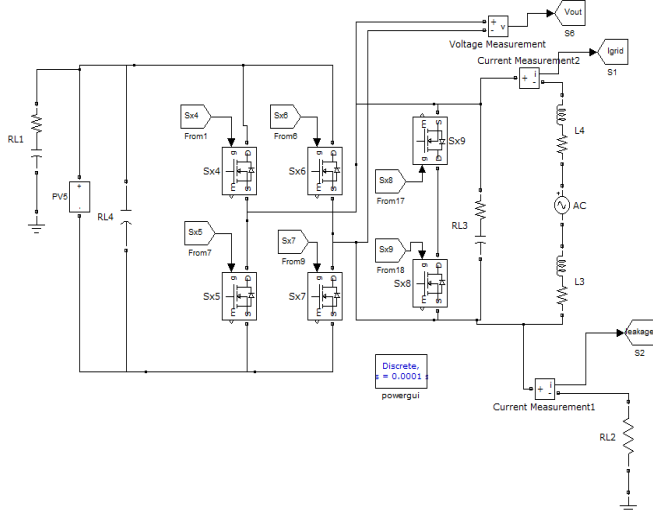




**Fig 17.** Total Harmonic Distortion of five level inverter Output Current in %

### Three level inverter

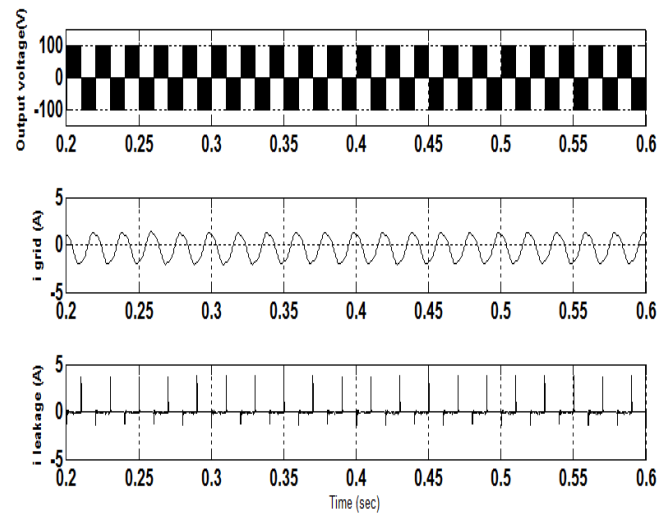
The input parameters of the three level inverter is taken as the three PV sources with each of 100 volts as the PV voltages and power as 300 watts each. The output voltage obtained by the three level inverter is one stepped wave form with the peak of 100 volts.



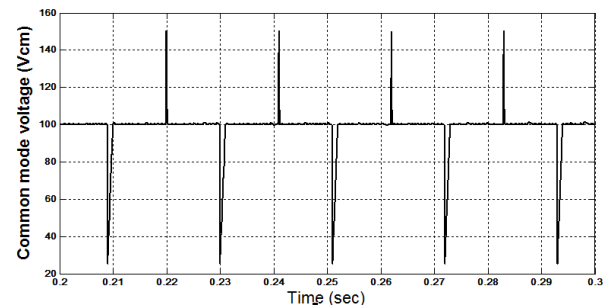
**Fig 18.** MATLAB Model of Photovoltaic based 3-level Cascaded MLI with reduced no. of switches

The inverter connected to grid and the grid current is nearly 3 amperes, coming to the leakage current the frequency of common mode voltage is reduced by the sinusoidal pulse width modulation technique and if frequency of the common mode voltage reduced then the leakage current reduced. The leakage current of

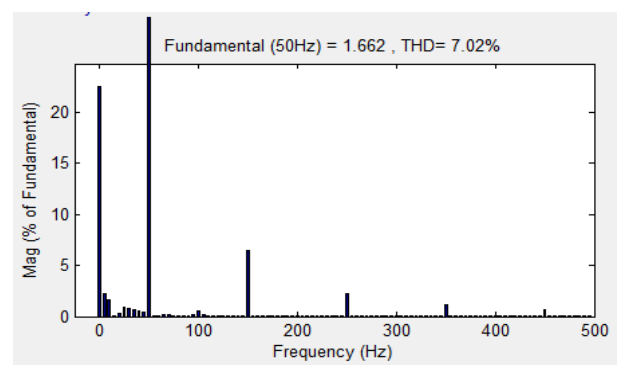
the three level inverter is below the 5 amps. The THD of the three level inverter is 7.02%.



**Fig 19.** Simulation waveforms of the three level CMLI Output Voltage (V), Grid Current (A) and Leakage Current (A).



**Fig 20.** The common mode voltage of the cascaded three level inverter.



**Fig 21.** Total Harmonic Distortion of three level inverter Output Current in %

#### IV. CONCLUSION

Photovoltaic based applications are increasing day by day. Since most of the electrical application are in AC, so some efficient Power Electronics DC to AC converters are required for converting photovoltaic DC output to AC. The proposed system having a Photovoltaic application based Cascaded 7- level Inverter has been shown to produce an increased stepped output with less number of semiconductor switches, and due to which controlling the overall circuit becomes less complex, the size and installation area reduced. Also included comparison of leakage currents and THD's of the 7-level, 5-level and 3-level inverters using MATLAB/SIMULINK. It is inferred with the help of simulation results the Multicarrier PWM techniques produced a lower THD.

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