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A High-Performance FIR filter Architecture for Reconfigurable Applications

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ABSTRACT

Transpose form finite-impulse response (FIR) filters are characteristically pipelined and support multiple constant multiplications (MCM) procedure that results in significant saving of calculation. However, transpose form configuration does not specifically support the block performing not like direct-form configuration. In this paper, we investigate the possibility of realization of block FIR filter in transpose shape configuration for area-delay efficient realization of huge order FIR filters for both fixed applications. Based on a detailed computational investigation of transpose form configuration of FIR filter, we have derived a flow diagram for transpose shape block FIR filter with reduced register complexity. A detailed block formulation is detailed for transpose form FIR filter. We have inferred a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A reduced-complex design using multiple constant multiplications scheme is also showed for block implementation of fixed FIR filters. The proposed architecture obtains less area, less delay and less power consumption compared with the existing architecture of direct form structure for medium or long filter lengths. For this project analysis for determining area, power and delay it uses Xilinx.

Keywords : Finite-Impulse Response (FIR), Block Processing, Reconfigurable Architecture, Multiple Constant Multiplications (MCM).

I. INTRODUCTION

Finite-impulse response filter is mostly used in several digital signal processing (DSP) applications like, loud speaker equalization, echo cancellation, adaptive noise cancellation, speech processing and different communication applications like software-defined radio (SDR). Huge numbers of these applications require FIR filters of extensive request to meet the recurrence specifications [2] – [4]. These filters need to help high inspecting rate for rapid computerized correspondence [5]. The number of multiplications and additions required for each filter output notwithstanding, increments straight with the filter arrange.

Since there is no repetitive calculation accessible in the FIR filter algorithm, real-time execution of a large order FIR filter in a resource constrained environment is a challenging task. Filter coefficients frequently stay steady and known *apiaria*n signal processing applications. This feature has been used to diminish the unpredictable for the realization of multiplications. A few designs have suggested by various researchers for efficient realization of FIR filters (having fixed coefficients) utilising distributed

arithmetic (DA) [18] and multiple constant multiplication (MCM) methods [7], [11]–[13].DA-based plans utilises lookup tables to store recomputed results to decrease the calculations complexity. The MCM technique then again decreases the number of additions essential for the implementations of multiplications by common sub expression sharing, when a given input is multiplied with a group of constants. The MCM technique is most effective, when the common operand was multiplied by more Number of constants. In this way, the MCM scheme is suitable for the realization of large order finite impulse response filters with fixed coefficients. In any case, MCM blocks can be formed only in the transpose form configuration of FIR filters.

Block-processing method was widely used to infer high-throughput hardware structures. It not only gives throughput-scalable design yet additionally enhances the area-delay efficiency. The inference of block-based FIR structure is very clear when direct-form configuration is utilised [16], though the transpose form configuration does not directly support block preparing. Be that as it may, to take the calculations advantage of the MCM, FIR filter is required to be figured it out by transpose form configuration. Aside from that, transpose form structure is innately pipelined and expected to offer higher working recurrence to support higher sampling rate

II. IMPLEMENTATION

To investigate the likelihood for implementing block FIR filter in transpose form configuration with a specific goal to exploit the MCM schemes and the inherent pipelining of area-delay efficient implementation of the large order Finite impulse response filters for fixed applications.

The main contributions are given below.

1. Computational examination of transpose form analysis of finite impulse response filter and dedication of flow chart for transpose form block finite impulse response filter with decreased register complications.
2. Block formulation development for transpose form FIR fixed filter.
3. A reduced-complexity analysis method utilising MCM scheme for block development of fixed finite impulse response filters.

III. EXISTING SYSTEM

Computational Analysis

Suppose in every cycle, the block FIR filter takes a block of L new input samples, and processes those to produce a block of L output samples. The k^{th} block of filter output y_k is computed using the relation

y_k=X_k.h

The computation can be expressed in a recurrence form as

$$Y(Z)= S^0(z)[z^{-1}(\dots(z^{-1}(z^{-1}c_{M-1} + c_{M-2}) + c_{M-3}) + \cdots) + c_1) + c_0]$$

The block transpose form configuration can be derived using this recurrence relation. The delay operator z^{-1} represents a delay for a block of data in transpose form structure that stores the product of S_k^0 and c_m.

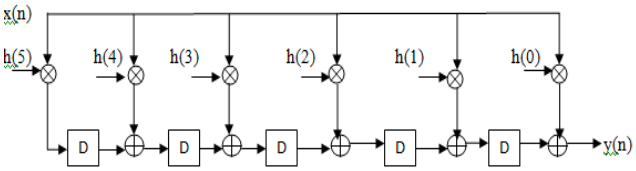

Figure 1. DFG of transpose form structure for output y(n) of length n=4

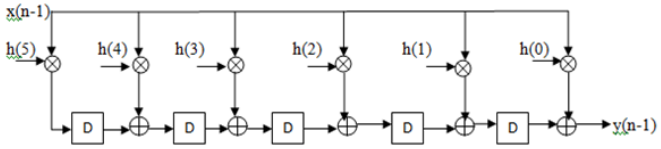

Figure 2. DFG of transpose form structure for output y(n-1) of length n=4

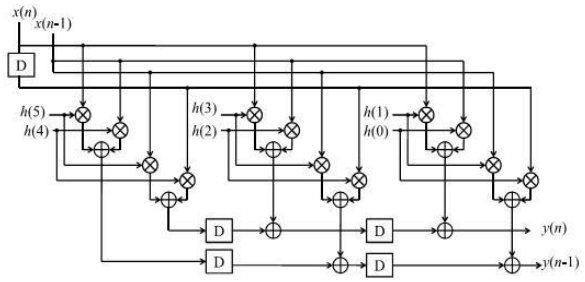

Figure 3. Block Formulation for Transpose Form FIR Filter

IV. PROPOSED SYSTEM

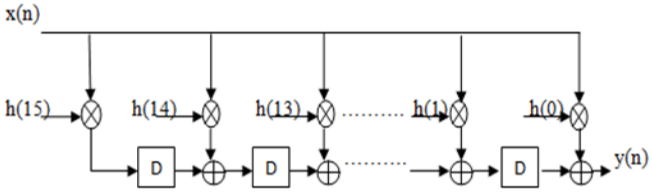

Figure 4. DFG of transpose form structure for output y(n) of length n=16

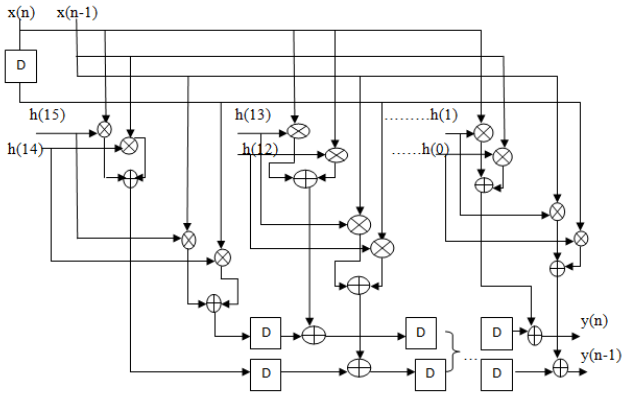

Figure 5. Block Formulation for Transpose Form FIR Filter length n=16

This is the block transpose form configuration of FIR filter with 16 coefficients. The data flow transfer of multipliers of this transpose form configuration of FIR filter is shown in above figure. This is the DFG of block FIR filter of 16 coefficients. It is used to implement proposed structure for reconfigurable applications.

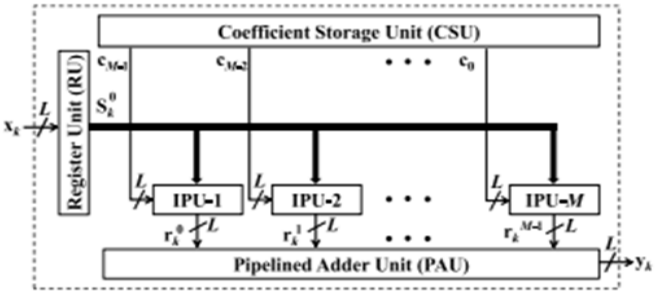

Figure 6. Block transpose of FIR filter for reconfigurable application Simulation results.

WAVEFORMS FOR EXISTING DFG of N=4:

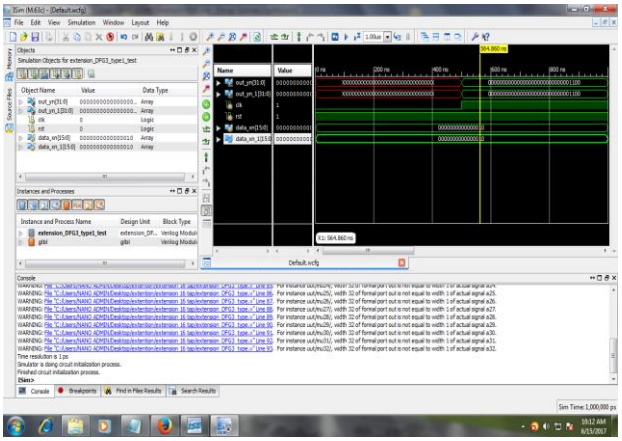

Figure 7. Waveforms for block transpose form configuration for reconfigurable application of n=6

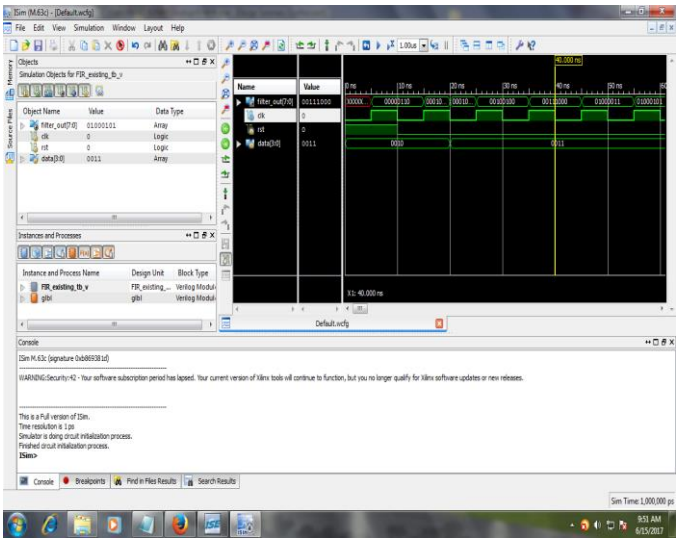

Figure 8.

WAVEFORMS FOR PROPOSED DFG OF N=16:

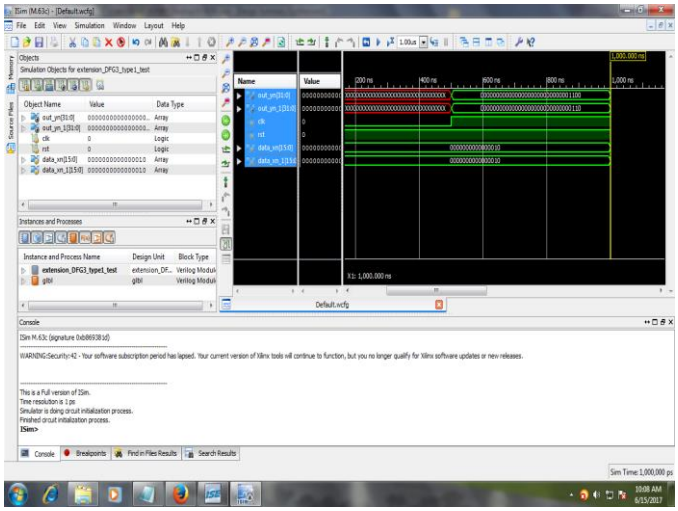

Figure 9. Waveforms for proposed block transpose form configuration for reconfigurable application of n=16

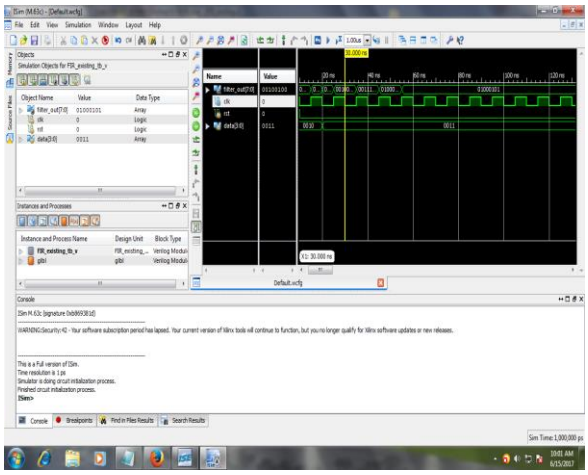

Figure 10.

V. SYNTHESIS RESULTS

Table1 : Comparison of existing DFG and proposed DFG

Parameter	Existing system	Proposed system
No.of 4 input LUTs	295	271
No. of slices	173	149
Time delay	13.226ms	4.90ms

Table 2. Comparison of existing and proposed reconfigurable FIR filter

parameter	Existing system of order(6)	Proposed system of order(16)
No. of 4 input LUTs	12	11
Time delay	3.724ms	3.724ms

VI. CONCLUSION

In this, block transpose form configuration of FIR filter is implemented with a greater number of coefficients. This block FIR filter is used to implement reconfigurable applications.

The delay efficient FIR filter in transpose form configuration is implemented in Xilinx and synthesized report has been generated. The synthesis results show that, the delay of the block transpose form configuration of reconfigurable FIR filter with higher order is similar to that of block transpose configuration of reconfigurable FIR filter with lower order. By using a greater number of coefficients, the performance of the system is increased.

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