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Design and Simulation of CMOS Four Quadrant Analog Multiplier

Priyesh P. Gandhi, Ph. D
Principal, Sigma Institute of Engineering, Vadodara, Gujarat, India

ABSTRACT

This paper represents design and simulation of CMOS Four Quadrant Analog Multiplier. The modified design demonstrates low control dissemination and higher data transfer capacity when contrasted with different models of the simple multiplier. The CMOS multiplier is planned and simulated in Generic 130nm and 90nm Technology.

Keywords : Flipped Voltage Follower (FVF), Four Quadrant Analog Multiplier (FQAM), FVF differential structure (DFVF), Analog Multiplier , CMOS Four Quadrant Analog Multiplier

I. INTRODUCTION

Out surrounding world is analog in nature. Digital systems require analog to digital conversion at the front of the system and digital to analog conversion at its end. Analog computation and signal processing make it simpler and faster [1]. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [2]. In this thesis, the new smaller size process technologies offer opportunities to operate at higher frequencies consuming less power. For analog circuits, this fact partially applies since it is often the case that additional current needed to keep the same performance when the power supply voltage is decreased. Furthermore, for submicron technology it would not be possible to use voltage doublers to enhance the circuit performance due to low breakdown voltage of the transistors. The main motivation for choosing Analog multiplier is its importance in nonlinear analog signal processing function finding application of a wide variety in adaptive filtering, modulation, frequency translation, automatic gain controlling, neural network, fuzzy integrated systems, etc. The linearity, speed, supply voltage and power dissipation are the main goal of design.

The Main specifications of a multiplier are:

Linearity:
It indicates the factor by which the output is dependent on the input parameters linearly for a multiplier the error in linearity should be very less so that for any change in the inputs output changes linearly.

Supply Voltage and Power Consumption:
This factor tells us the amount of power supply required for the whole circuit and according to the power supply requirements and the components used power consumption can be determined. For a multiplier low power supply voltage is required and

minimum no of transistors should be used so that power consumption is less.

Bandwidth:

The range of frequencies for which the gain of a circuit is constant gives the bandwidth of the system. For a multiplier the bandwidth should be high so that it works properly for high frequencies.

The total harmonic distortion [THD], of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the allows the components in a loudspeaker, amplifier or microphone or other equipment to produce a more accurate reproduction by reducing harmonics added by electronics and audio media. A THD rating < 1% is in high-fidelity and inaudible to the human ear.

Analog multipliers are used in communication circuits as well as in neural networks and fuzzy logic applications. Phase detector, adaptive filter, function generators, frequency doubling and amplitude modulation are some applications of analog multipliers in communications industry. Voltage gain amplifier, signal squarer, RMS signal estimator and weight-input multiplication in neural networks are some application in signal processing. Phase detector is an essential element in phase locked loops. PLLs are widely used in frequency synthesizers, demodulators, clock generation circuits, clock recovery circuits and spread spectrum PLLs. Analog multipliers as part of automatic gain control circuits used in AM radio receivers and radar systems. Analog multiplier is also work as sub-circuit for many applications such as adaptive.

II. METHODS AND MATERIAL

Filters and frequency modulators.

1. Existing Design & Analysis of Four Quardant Analog Multiplier

The multiplier has two inputs, therefore there are four combination of two differential signals, i.e. (x, y), (x,-y), (-x, y), (-x, -y). The topology of Fig. 1 is based on single quadrant multipliers.

$$[(X + x)(Y + y) + (X - x)(Y - y)] - [X - x)(Y + y) + (X + x)(Y - y)] = 4xy \quad (1)$$

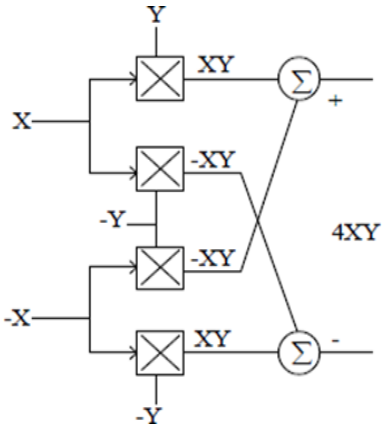

Figure 1. FQAM using Single Quadrant Multiplier

Fig 2 is based on Square law devices. These topologies achieve multiplication and simultaneously cancel out all the higher order and common mode components (X and Y) based on the following equalities

$$[(X + x)(Y + y)^2 + (X - x)(Y - y)^2] - [X - x)(Y + y)^2 + (X + x)(Y - y)^2] = 8xy \quad (2)$$

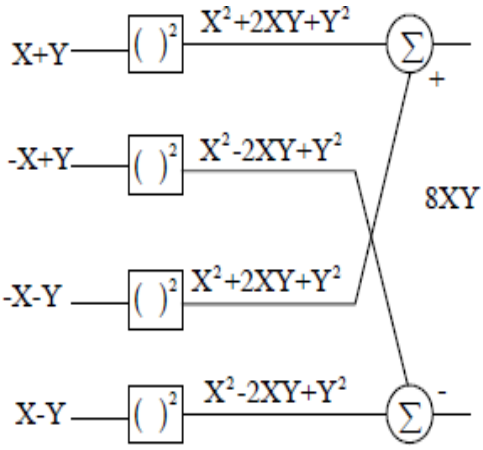

Figure 2. FQAM using Square Devices

III. Proposed Four Quadrant Analog Multiplier

A CMOS multiplier employing a multiplying quad (M1 - M4) is shown in Fig. 3 the multiplying quad operates in the triode region, and thus MOSFETs MI-M4 can be thought of as resistors. For this moment we will not consider the biasing of the quad. The negative output voltage of the multiplier is given by

$$V_{o-} = -R.\ (I_{D1} + I_{D2}) \qquad (3)$$

While the positive output voltage is

$$V_o = -R.\ (I_{D3} + I_{D4}) \qquad (4)$$

The output voltage of the multiplier is

$$V_{out} = R\ (I_{D1} + I_{D2} - I_{D3} - I_{D4}) \qquad (5)$$

A schematic of the multiplying quad with biasing is shown in Fig.3. The input signals have been broken into two parts (e.g., Vx /2 and -vx /2) to maintain generality. In practice, the minus inputs can be connected directly to the bias voltages.

Using, saturation drain current equation and noticing that the DC gate-source voltage of all MOSFETs is the same, the drain currents can be written as:

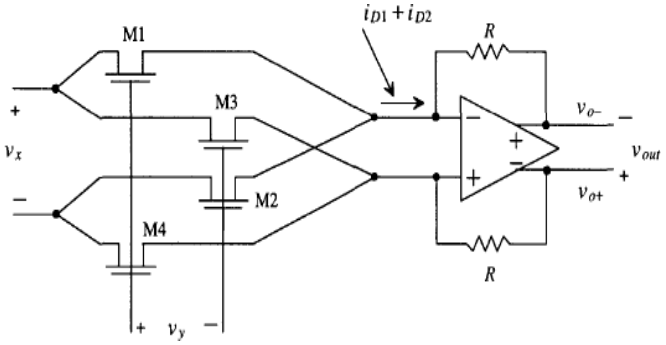

Figure 3. Analog Multiplier without Biasing

The source of a MOSFET (the terminal we label "source" depends on which way current flows in the MOSFET) in the multiplying quad is connected either to the op-amp or to the x inputs. When the sources of the MOSFETs are connected to the op-amp, all the MOSFETs in the multiplying quad have the same threshold voltage. (Since the source of each MOSFET is tied to the same potential, the body effect changes each MOSFET's threshold voltage by the same amount.) If the "+" X input is sinking a current, then the sources of Ml and M3 are the "+" X input and thus $V_{THN1} = V_{THN2}$ In any case, the threshold voltages of the MOSFETs cancel and Eq. $V_{out} = R\beta.\ V_xV_y$

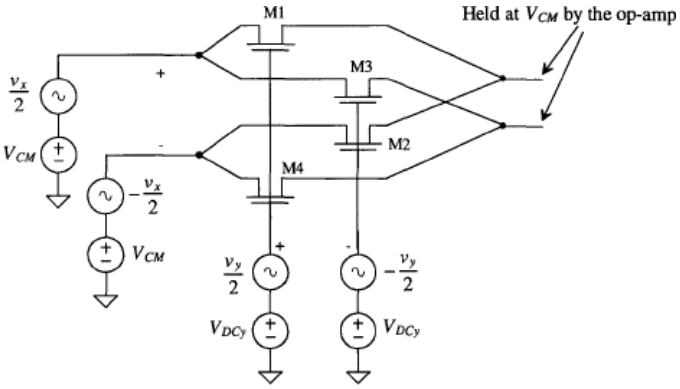

Figure 4. Biasing of the Multiplying Quad.

3.1 Operation of the Proposed Four Quadrant Analog Multiplier

The design of a multiplier consists of designing the op-amp, selecting the sizes of the multiplying quad and designing the biasing. In order to simulate the performance of a multiplier the sum of the multiplying factors associated with the voltage-controlled voltage sources, El and E2, is the open-loop gain of the op-amp.

3.2 Performance Analysis of Flipped Voltage Follower (FVF)

It is essentially a cascade amplifier with negative feedback where the gate terminal of M1 is used as an input terminal and its source as the output terminal. It is characterized by a very low output impedance due shunt feedback provided by M2, high low supply requirement closes to a transistor threshold voltage VTH, low static power dissipation and high gain bandwidth. The flipped (inverted) voltage follower

name is since FVF is applied on the drain side than on the side of the source. Variation of the output current is absorbed by transistor M2 which is current sensing transistor, while the current remains constant M1, because of this source voltage of the gate of M1 is constant and remains low distortion even at high frequency. A practical limitation of the FVF cell is that it gives very small input and output signal swing.

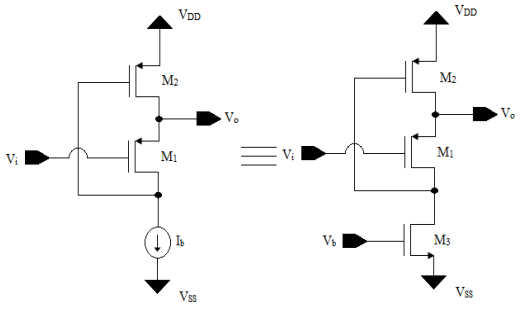

Figure 5. Flipped Voltage Follower

The voltage swing is especially important for analog circuits with the trend of supply voltage becoming smaller and the noise almost the same. In order to obtain an acceptable dynamic range, the output swing should be sustained as high as possible. The output headroom of flipped voltage follower is decreased to V_{GS} -$2V_{Dsa}$t which serious limits the output swing performance in deep sub-micron CMOS process.

3.3 Offset Analysis FVF differential structure (DFVF)

The first differential structure based on the FVF cell can be built by adding an extra transistor connected to node X, as it is shown in Fig. 6. It will be called the "FVF differential structure (DFVF)." As indicated in the previous section, the impedance at node X is very low and its voltage remains approximately constant for large currents through M3.

If we consider quiescent condition when V1 = V2, and assuming the same transistor sizes for M1 and M3, the condition $I_{DM1} = I_{DM3} = I_B$ is satisfied. A differential voltage V1 - V3 generates current variations in M3 that follow the MOS square law.

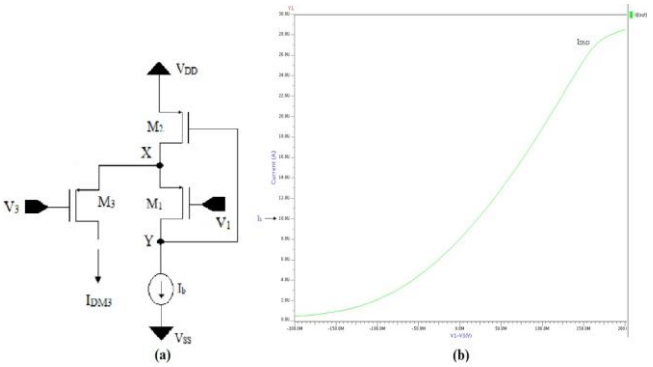

Figure 6. (a) Basic implements of DFVF (b) DC response of DFVF

This is a very interesting property of the DFVF as the maximum output current can be much larger than the quiescent current I_B. Figure 6 shows the dc transfer characteristic for I_{DM3} versus V1 = V3. The typical class-AB behavior can be observed. Another characteristic of the DFVF is that the output is available as both a current (I_{DM3}, or the current though M2 replicated by means of a current mirror), and a voltage (node Y). This feature can be advantageously employed to simplify the circuit implementations reducing both noise and number of poles and zeros. Finally, the DFVF can also be operated with very low supply voltage. The minimum supply voltage is, as in the case of the FVFCS, $V_{DD} = |V_{tp}| + 2V_{DSsat}$. Once again, with a supply of V_{DD} there would be no room for variation of the input signals V1 and V3. It is easy to obtain an expression relating the expected variation of V1 and V3 with the minimum supple voltage which maintains the DFVF cell properly biased [16].

3.4 Voltage Controlled Square-Rooting Circuit

The square-rooting circuit shown in Fig. 7 consists of an MOS transistor (M3) and the flipped voltage follower (M1 and M2). The transistor M3 in fig.7 is used as a simple current-to-voltage converter. When

source terminal voltage of M3 is equal to -VTN therefore, the current of equation shown as In dynamic comparator power is expressed as below [17].

$$I_{in} = I_{d3} \quad (6)$$

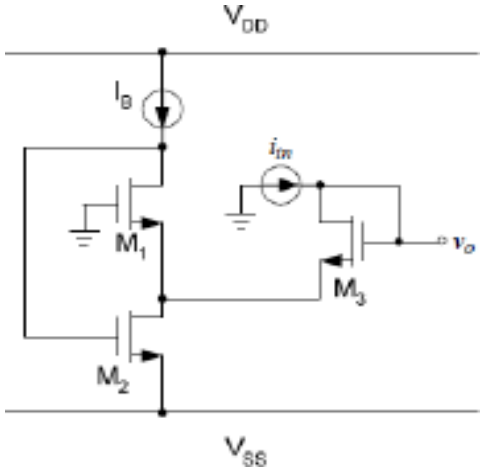

Figure 7. Square-rooting Circuit

IV. Simulation Result

4.1 Simulation Results of DDC

The simulation results are shown in Figure 8 to Figure 15.

The DC transfer characteristics of the FVF cell are shown in Figure 10.

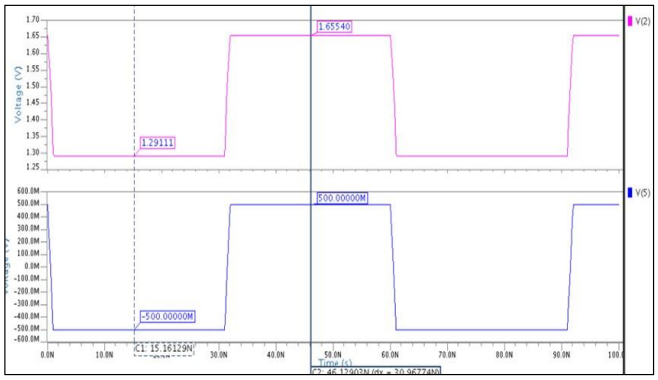

Figure 8. Transient analysis of FVF cell

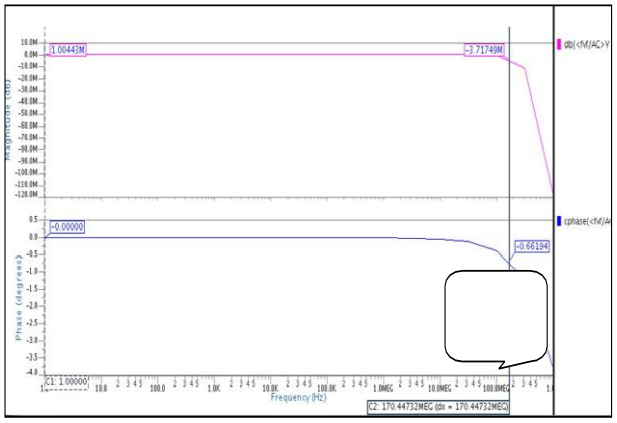

Figure 9. Frequency response of FVF Cell

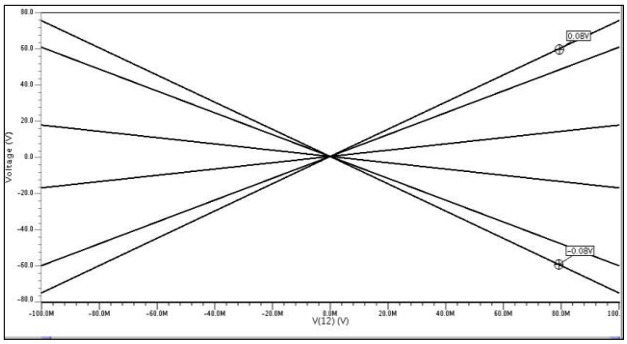

Figure 10. DC Characteristic of Multiplier based on FVF cell

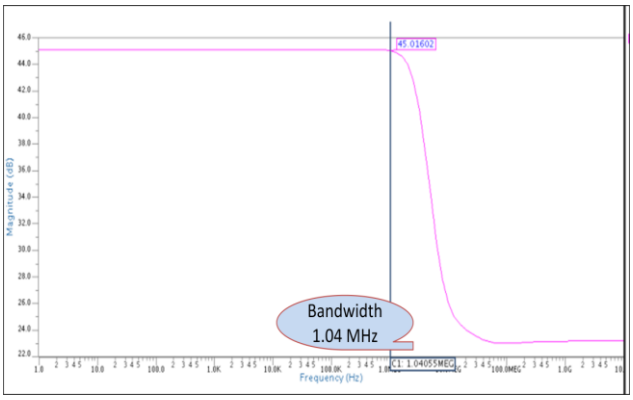

Figure 11. AC analysis of multiplier based on FVF cell.

4.2 Simulation Results Simulation Results in Generic 130nm Technology

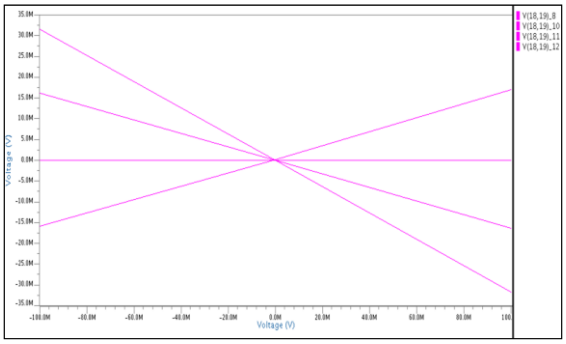

Figure 12. DC Characteristics of Analog Multiplier

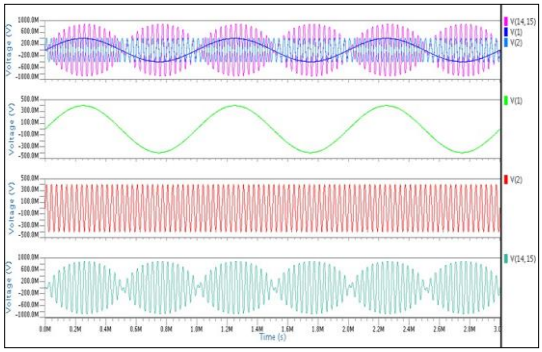

Figure 13. Transient Analysis of Analog Multiplier

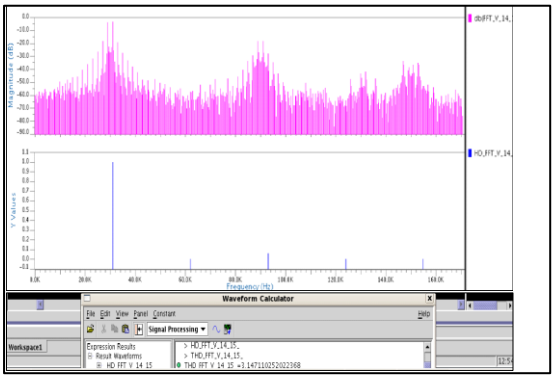

Figure 14. Total Harmonic Distortion of Analog Multiplier.

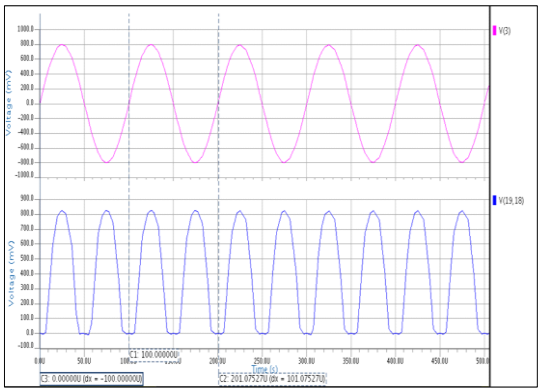

Figure 15. Frequency Dubeller of Analog Multiplier

Table 1 evaluates the performance of the Simulated Results of Modified Architecture of Analog Multiplier for Different Generic Technologies.

Table 1. Simulated Results of Modified Architecture of Analog Multiplier.

Parameters	Technology	
	130nm (Generic)	90nm (Generic)
V_{DD}	1.3V	1V
Bandwidth (GHz)	2.88	4.16
Power Dissipation (mW)	3	5
THD (%)	3.14	2

V. CONCLUSION

The postulation basically centered on the plan and reenactment of different sort of Four Quadrant Analog Multiplier. Here, predominantly three kind of simple multiplier design reproduced, first is utilizing Differential pair, second is utilizing square-establishing gadgets and last one is altered engineering utilizing viper and subtractor square. The all multiplier design is simulated in Generic 130nm and 90nm advances. Essential simple

multiplier engineering makes with multiplier quad and operation Amplifier. This engineering has more power scattering and moderate transfer speed. This trademark improved by second engineering utilizing FVF cell with square gadgets which work on low supply voltages, low control utilization and wide information rang however transfer speed acquire is extremely less. The adjusted engineering of simple multiplier which given high data transmission in GHz term and have a less control dissemination then other design and examine absolute symphonious contortion of circuit. It can likewise fill in as Analog modulator and Frequency doublers.

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