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Design Implementation of Successive Approximation Register A/D Converter

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ABSTRACT

This paper presents design implementation of Successive Approximation Register ADC. The ADC is the main building block in modem signal processing and communication systems. Main purpose of the ADC is to convert analog input into an equivalent digital output. There are many ADCs depending on the application like Sigma Delta ADC, Pipelined ADC, SAR ADC. The Successive Approximation Register (SAR) ADC is the most widely used converter in industrial control applications. It has good ratio of speed/power and has compact size that make this converter into an inexpensive device. A low power 8-bit 200MS/s Successive Approximation Register Analog to Digital Converter is designed and implemented in 180nm TSMC CMOS VLSI process. To reduce the complexity of design TG based D Flip-flop and charge scaling DAC are used. To increase the conversion rate and reduce the overall power dissipation of ADC Dynamic Latch Comparator is used.

Keywords : Analog to Digital Converters (ADCs), Successive Approximation (SAR), Flash ADC, Propagation delay, Offset Voltage, Power Dissipation Spurious Free Dynamic Range (SFDR).

I. INTRODUCTION

High-performance applications like as broadband communication systems require high-performance analog-to-digital converters (ADCs). Due to advantages given by the digital systems, they are mostly used in many fields such as instrumentation, control, communication and computers. In many such applications they are not available in digital form. Most of the physical quantities such as temperature, pressure, displacement, vibrations etc. are available in analog form. These quantities are represented accurately in analog form, but it is difficult to process, store or transmit the analog signal because error gets introduced easily, due to noise. Hence to reduce these errors it is always better to express these physical quantities in the digital form. The digital representation of signal makes storage possible, processing simpler and transmission easier. Hence A to D conversion is necessary.

II. METHODS AND MATERIAL

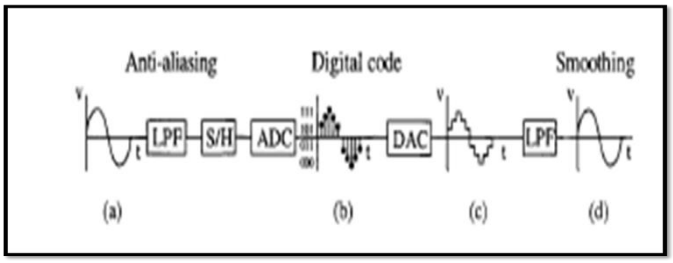

Figure 1. Signal Characteristics caused by A/D and D/A Conversion

ADC converts analog signals into discrete time or digital signals. DAC performs the reverse operation. Figure 1

illustrates these two operations. The original analog signal is filtered by an anti-aliasing filter to remove any high-frequency harmonics that may cause an effect known as aliasing. The signal is sampled and held and then converted into a digital signal. Next the DAC

converts the digital signal back into an analog signal. Note that the output of the DAC is not as "smooth" as the original signal. A low-pass filter returns the analog signal back to its original form after eliminating the higher order harmonics caused by the conversion. This example illustrates the main differences between analog and digital signals. Whereas the analog signal is continuous and infinite valued, the digital signal in is discrete with respect to time and quantized. The term continuous-time signal refers to a signal whose response with respect to time is uninterrupted. Simply stated, the signal has a continuous value for the entire segment of time for which the signal exists. By referring to the analog signal as infinite valued, we mean that the signal can possess any value between the parameters of the system. The digital signal, on the other hand, is discrete with respect to time. This means that the signal is defined for only certain or discrete periods of time. A signal that is quantized can only have certain values for each discrete period [14].

There are many ADC architectures are available like flash ADC, sigma delta ADC, folding and interpolating ADC, two-step ADC, pipelined ADC, SARADC etc. Comparison of various ADC architectures is shown in Table 1 and its application based on resolution is also shown in Figure 2.

Among various ADC architectures, the SAR ADC has the attractive feature of maintaining high accuracy at medium conversion rate. For this reason, it is used extensively in acquisition systems and high performance digital communication systems where both precision and smaller area is critical.

Table 1 shows the comparisons among various ADC Architectures.

Table 1. Comparison of ADC Architectures

Architecture	Latency	Speed	Accuracy
Flash	No	High	Low
Folding/interpolating	No	Medium-High	Low-Medium
Delta-Sigma	Yes	Low	High
Pipeline	Yes	Medium	Medium-High
SAR	Yes	Low	Medium-High

The steep rise in the demand of compact devices has revolute the world. To reconstruct the exact signals in high quality better converters are needed. Apart from the problem of technology scaling and reduced supply voltages, another important aspect of use of ADCs are converting analog signals in the digital to store them for the future use. In different types of ADCs available like flash ADC, folding and interpolating ADC, two-step ADC, pipeline ADC, successive-approximation-register (SAR) ADC, delta-sigma ADC, integrating ADC etc; SAR ADC optimize the design which is the reason to choose SAR ADC. The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. The Successive Approximation (SAR) architecture is very suitable for data acquisition; it has resolutions ranging from 8 bits to 18 bits and sampling rates ranging from 50 KHz to 50 MHz.

Flash or parallel converters have the highest speed of any type of ADC. As seen in Figure 2, they utilize one comparator per quantization level (-1) and resistors. The reference voltage is divided into values, each of which is fed into a comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code will exhibit all zeros for each resistor level if the value of is less than the value on

the resistor string, and ones if is greater than or equal to voltage on the resistor string. A simple -1: N digital thermometer decoder circuit converts the compared data into an N-bit digital word. The advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word. The advantage of having high speed, however, is counterbalanced by the doubling of area with each bit of increased resolution. For example, an 8-bit converter requires 255 comparators, but a 9-bit ADC requires 511! The flash converters have traditionally been limited to 8-bit resolution with conversion speeds of 10 - 40 Ms/s using CMOS technology. The disadvantages of the Flash ADC are the area and power requirements of the -1 comparators. The speed is limited by the switching of the comparators and the digital logic [14].

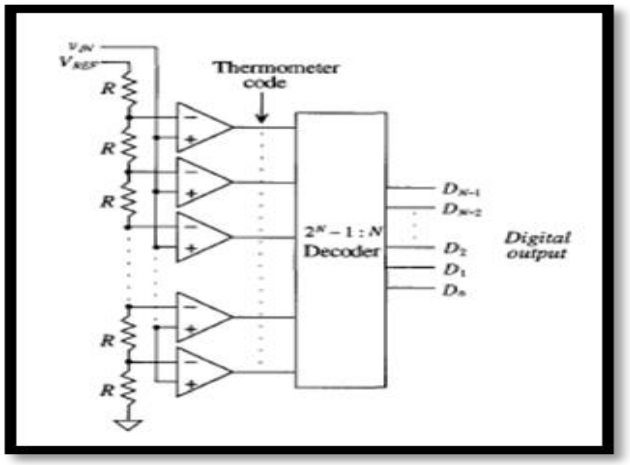

Figure 2. Block Diagram of Flash ADC

Another type of Flash converter is called the two-step Flash converter or a parallel, feed-forward ADC. The basic block diagram of a two-step converter is shown in Figure3 [14].

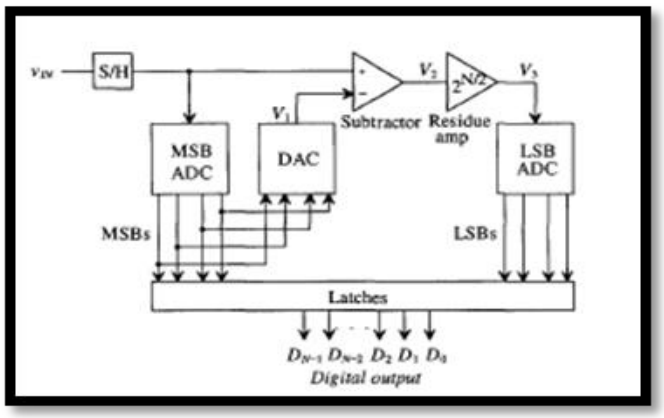

Figure 3. Block Diagram of Two Step Flash ADC

The converter is separated into two complete Flash ADCs with feed-forward circuitry. The first converter generates a rough estimate of the value of the input, and the second converter performs a fine conversion. The advantages of this architecture are that the number of comparators is greatly reduced from that of the Flash converter. For example, an 8-bit Flash converter requires 255 comparators, while the two-step Flash requires only 30. The tradeoff is that the conversion process takes two steps instead of one, with the speed limited by the bandwidth and settling time required by the residue amplifier and the summer.
The conversion process is as follows:

1. After the input is sampled, the most significant bits (MSBs) are converted by the first Flash ADC.
2. The result is then converted back to an analog voltage with the DAC and subtracted with the original input.
3. The result of the subtraction, known as the residue, is then multiplied by and input into the second ADC. The multiplication not only allows the two ADCs to be identical, but also increases the quantum level of the signal input into the second ADC.
4. The second ADC produces the least significant bits through a Flash conversion.

This type of ADC is an improvement of flash ADC. The folder basically folds the conventional linear I/O response to be sandwiched in between a smaller voltage range, so that they require a lesser number of comparators. When the number of comparators is

reduced, it automatically reduces the circuit's power demand. A typical block diagram of a folding ADC is shown in Figure 4. The analog preprocessor, in front of the fine quantizer, consists of folding amplifiers that generate the folded signals. The folded signal is like the residue signal in a sub ranging ADC, except for the fact that the residue signal is not generated from the output results of the coarse quantizer. A high conversion rate is achieved because the coarse and fine quantizers are in parallel. The open-loop design of the folding amplifiers also speeds up the converter. Ideally, an analog preprocessor should generate a saw tooth waveform, but this is difficult to implement. Instead, a triangle waveform is used in actual implementation, but sharp corners remain difficult to realize. The actual waveform is more sinusoidal and causes nonlinearity errors in the ADC. This type of architecture would suit a medium resolution of 4-8-bit for the sampling frequency ranges above 100 MHz [14].

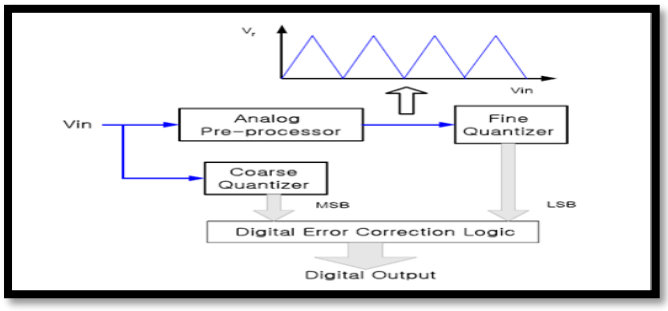

Figure 4. Block Diagram of Folding ADC

1. Existing Architectures of Successive Approximation Register (SAR) ADC

It consists of a comparator, a DAC and a successive approximation register (SAR). The successive approximation ADC uses a binary search algorithm to find the closest digital code for an input signal. When an input signal is applied to the converter, the comparator simply determines whether the input signal is larger or smaller than the DAC output and produces one digital bit at a time starting from the MSB. The SAR stores the produced digital bit and uses the information to change the DAC output for the next comparison. This operation is repeated until all the bits in the DAC are decided. In order to achieve N-bit resolutions, a successive approximation ADC requires N clock cycles. Because the performance is limited by DAC linearity, the calibration of the DAC is needed to achieve high resolution.

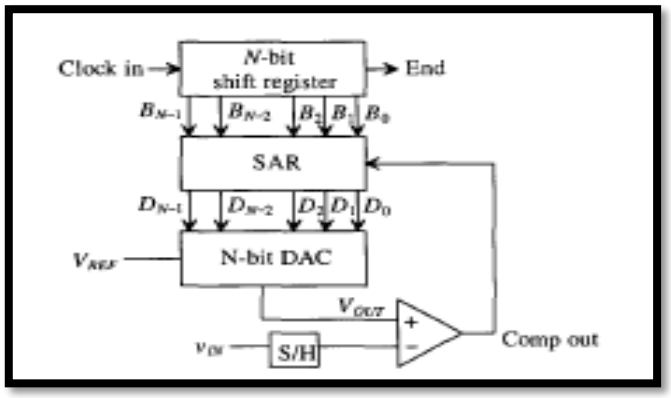

Figure 5. Architecture of SAR ADC.

The SAR ADC uses a binary search mechanism to convert the analog signal to the digital signal. It has several advantages. It uses fewer analog components in its design making its design compact. It also has a very low latency compared to other circuits. Figure 5 shows the block diagram of a SAR ADC [14].

2. Proposed Successive Approximation Register (SAR) ADC

2.1 SAR Logic

The successive approximation register (SAR) is based on ring counter and shift register. In Figure 6, numbers of D Flip-flop (DFF) with set and reset are the major part of SAR.

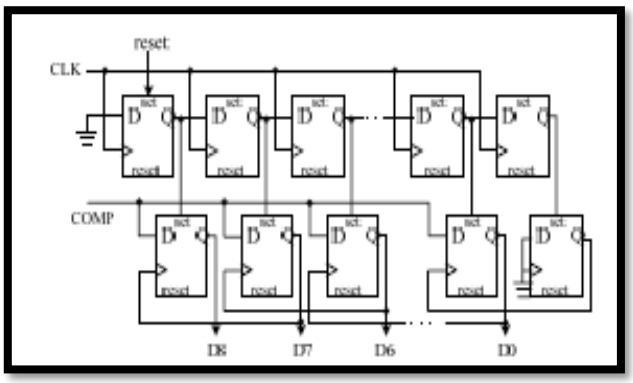

Figure 6. SAR Block Diagram

SAR logic consists of a ring counter and a shift register. At least 2N-1 flip flops are employed in this kind of SAR. SAR control logic determines the value of bits sequentially based on the result of the comparator. Each conversion takes 9 clock cycles. In the first clock cycle, SAR is in the reset mode and all the outputs are zero. In the next 8 clock cycles, data is converted, and each bit is determined sequentially. The last cycle is for storing the results of the complete conversion. In each cycle of clock, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of Flip Flop is used as the clock signal for the previous Flip Flop. At rising edge of the clock, this Flip Flop loads the result from the comparator.

2.2 DAC Logic

The digital to analog converter (DAC) converts the digital word at the output of the SAR logic to an analog value. Then in the comparator, this value is compared to the input signal. A wide variety of DAC architectures exist, ranging from very simple to complex. Each, of course, has its own merits. Some use voltage division, whereas others employ current steering and even charge scaling to map the digital value into an analog quantity. In the following three different architectures of capacitive DAC are presented. Resister string DAC, R-2R Ladder DAC, Current string DAC, Cyclic DAC, Pipeline DAC, Charge Scaling DAC.

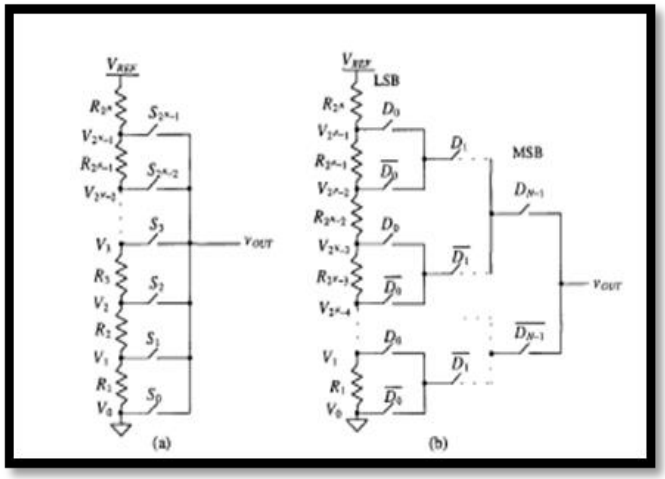

Figure 7. (a) A Simple Resistor String DAC
(b) use of a Binary Switch Array

The most basic DAC is seen in Figure 7(a) Comprised of a simple resistor string of 2N identical resistors and switches, the analog output is simply the voltage division of the resistors at the selected tap. Note that a N:2N decoder will be required to provide the 2N signals controlling the switches. This architecture typically results in good accuracy, provided that no output current is required and that the values of the resistors are within the specified error tolerance of the converter. One big advantage of a resistor string is that the output will always be guaranteed to be monotonic.

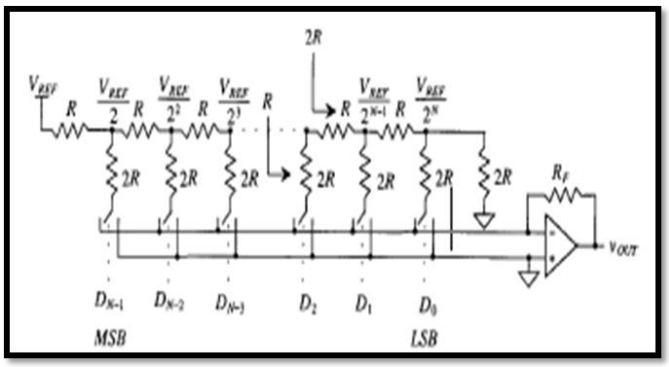

Figure 8. An R-2R Digital-to-Analog converter

Another DAC architecture that incorporates fewer resistors is called the R-2R ladder network [14]. This configuration consists of a network of resistors alternating in value of Rand 2R. Figure 8. illustrates an N-bit R-2R ladder. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R. The digital input determines whether each resistor is switched to ground (non inverting input) or to the inverting input of the Op-Amp. Each node voltage is related to V_{REF}, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from V_{REF} is constant, since the potential at the bottom of each switched resistor is always zero volts (either ground or virtual ground). Therefore, the node voltages will remain constant for any value of the digital input.

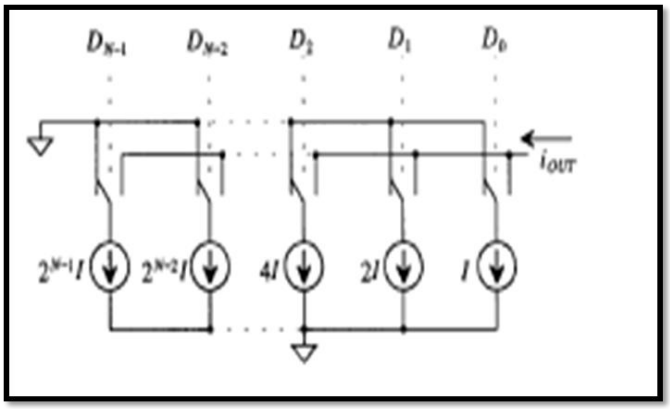

Figure 9. A Generic Current Steering DAC

Figure 9 illustrates a generic current steering DAC. This configuration requires a set of current sources, each having a unit value of current, I. Since there are no current sources generating i_{out} when all the digital inputs are zero, the MSB, DZN_Z, is offset by two bits instead of one. For example, for a 3-bit converter, seven current sources will be needed, labeled from Do to D_6. The binary signal controls whether the current sources are connected to either i_{out} or some other summing node. The output current, i_{OUT}> has the range of

$0 \leq i_{out} \leq (2^N-1)$ -----(1)

and can be any integer multiple of I in between. An interesting issue to note is the format of the digital code required to drive the switches. Since there are 2^N-1 current source, the digital input will be in the form of a thermometer code. This code will be all 1's from the LSB up to the value of the k^{th} bit, D_k , and all O's above it. The point at which the input code changes from all l's to all D's "floats" up or down and resembles the action of a thermometer, hence the name. Typically, a thermometer encoder is used to convert binary input data into a thermometer code.

2.3 CMOS Switch

This CMOS switch converts the 1-bit digital to an analog signal. Fig.10 shows the circuit level diagram of 1-bit DAC. It is made using 2×1 multiplexer. As the number of bits is only 1-Bit, the corresponding analog output will also have two levels and like the digital output. The present 1-Bit digital-to-analog converter has two reference voltages as shown in Fig.10. A positive reference voltage of $+V_{REF}$ and a negative reference voltage of $-V_{REF}$ or ground. It must select Volt or 0 Volt depending on the output of each bit of D Flip-flop which acts as a selection line. Mux is implemented using two TGs.

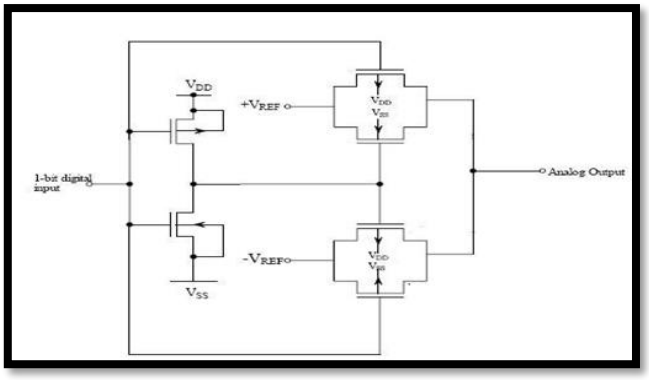

Figure 10. 1-Bit CMOS Switch

III. Simulation Result

2.4 Simulation Results of SAR ADC

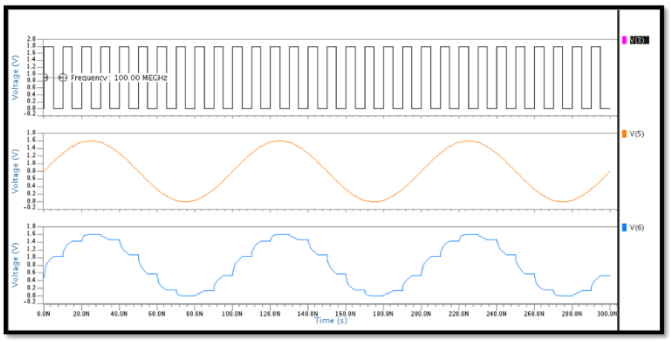

Figure 11. Transient Simulation of Sample and Hold

(Fm= 10MHz, Fs = 100MHz)

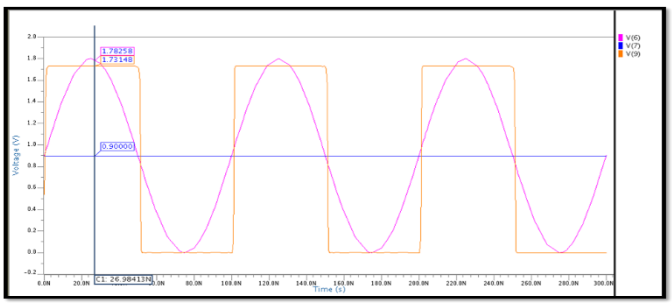

Figure 12. Transient Simulation of Comparator

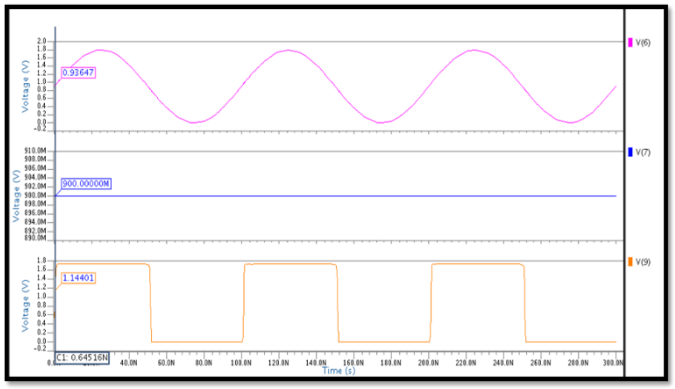

Figure 12. Propagation Delay of Comparator

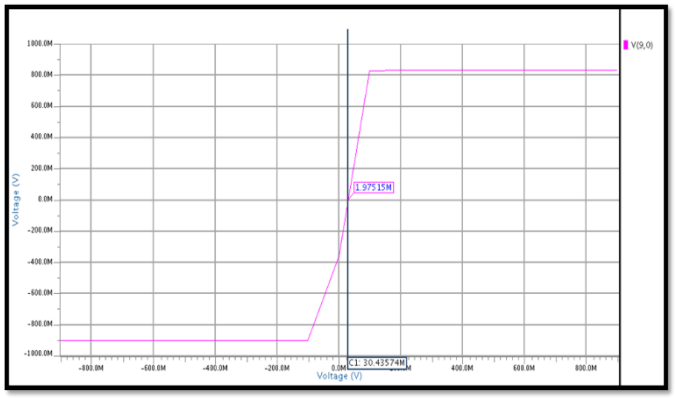

Figure 13. Offset of Comparator

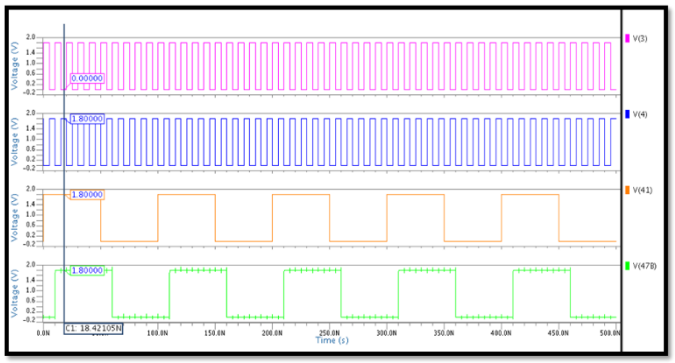

Figure 14. Transient response of D Flip-Flop

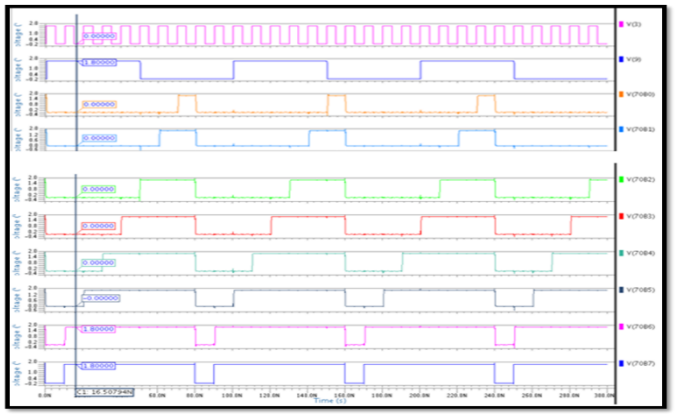

Figure 15. Output of 8 bit SAR Logic

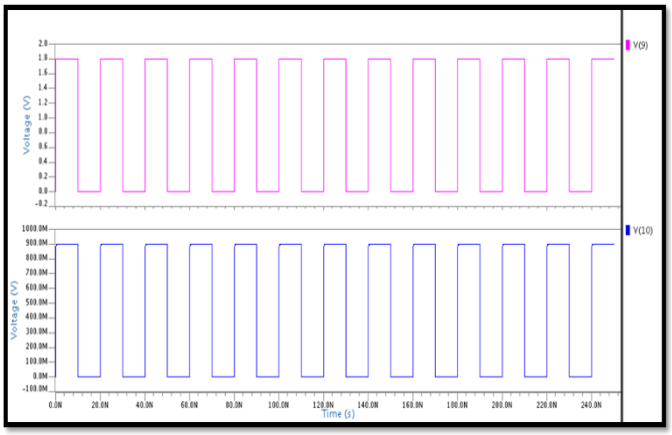

Figure 16. Transient Simulation of CMOS Switch

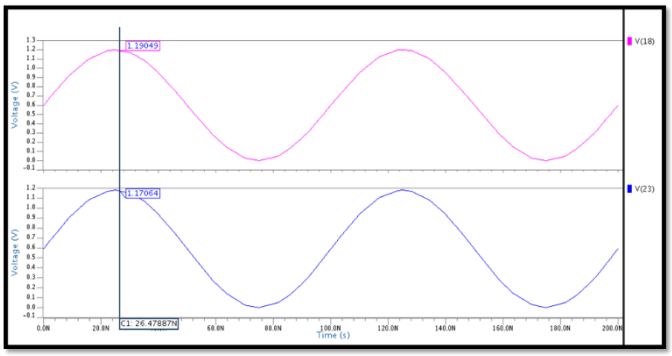

Figure 17. Transient Simulation of OPAMP as Buffer

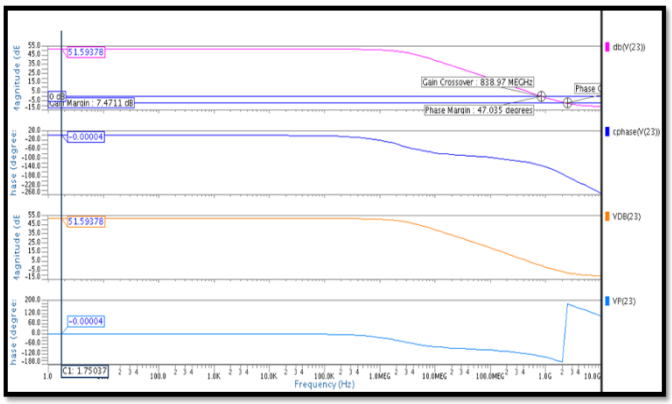

Figure 18. Frequency Response of Two Stage Op-Amp

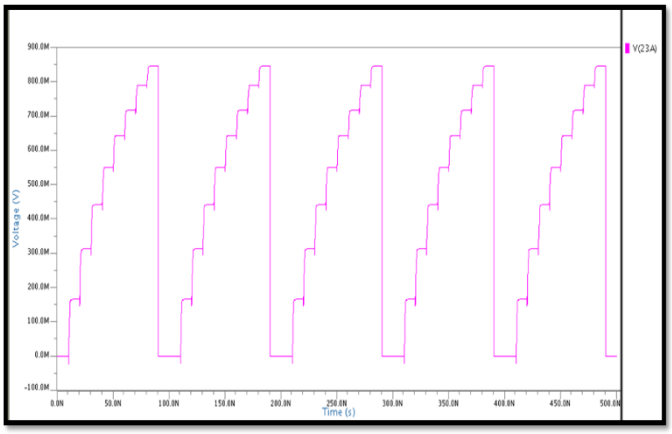

Figure 19. Simulation of 8- Bit Charge Scaling DAC

2.5 Simulation Results of 8- Bit SAR ADC

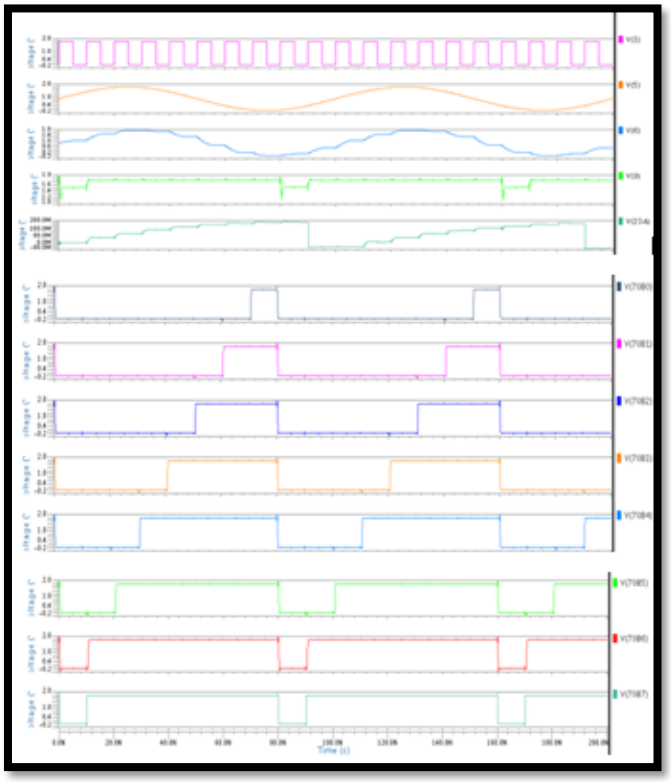

Figure 20. Simulation Result of 8- Bit SAR ADC

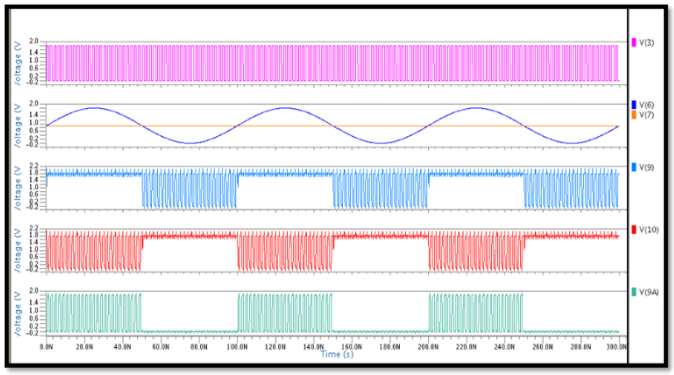

Figure 21. Transient Simulation of Dynamic Latch Comparator

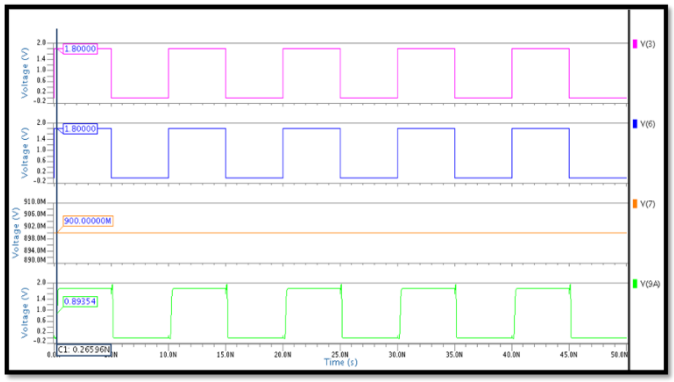

Figure 22. Propagation Delay of Dynamic Latch Comparator

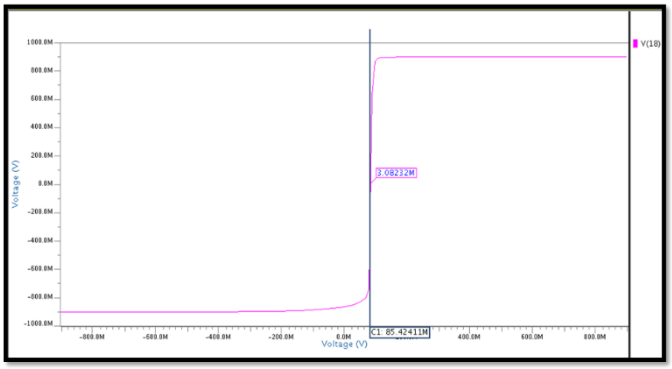

Figure 23. Offset of Dynamic Latch Comparator

2.6 Simulation Results of 8 - Bit SAR ADC using Dynamic Latch Comparator

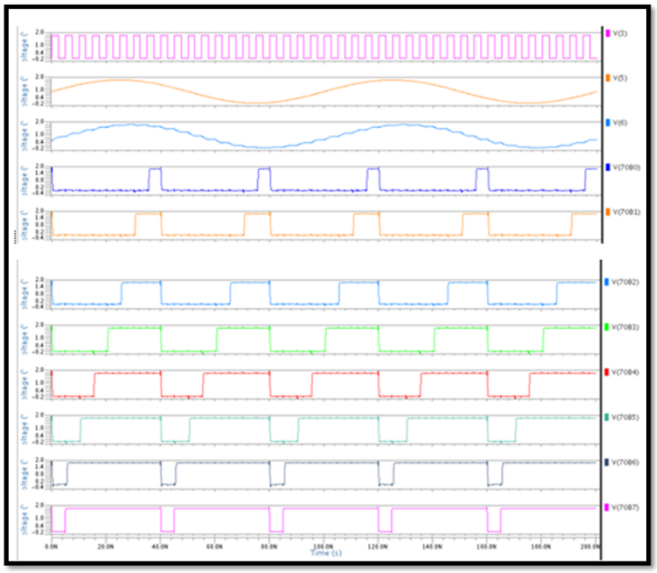

Figure 24. Simulation Results of 8- Bit SAR ADC using Dynamic Latch Comparator

Table 2 illustrates the comparison of SAR ADC based on different comparator design. Table 3 illustrates the comparative design analysis for SAR ADC Designs for the circuit designers to fully explore the trade-offs in SAR ADCs.

Table 2. Comparison of SAR ADC based on different Comparator

Parameter/Value	SAR ADC using Open Loop Comparator	SAR ADC using Dynamic Latch Comparator
Technology	180nm	180nm
Supply voltage	1.8v	1.8v
Samples	100MS/s	200MS/s
Input Frequency	10 MHz	10 MHz
Resolution	8bit	8bit
Power dissipation	788µW	12.3nW

IV. CONCLUSION

This paper showcase the implementation of high performance SAR ADC with its key building blocks such as sample and hold, comparator, SAR register and DAC. The 8-Bit 100MSPS low power SAR ADC is designed in TSMC 180nm CMOS process digital. This design is supported by necessary simulation results of selected building blocks and whole ADC. The main block comparator is characterized for Offset, Propagation Delay and Power Consumption. To increasing the conversion speed of ADC Dynamic Latch Comparator is simulated and characterized for Offset, Propagation Delay and Power Consumption and by using this Dynamic Latch Comparator 8 Bit SAR ADC has been implemented with Conversion Rate of 200 MSPS.

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Table 3. Comparative Design Analysis of SAR ADC

Parameter /Value	[2]	[13]	[7]	This Work
Technology	180nm	180nm	180nm	180nm
Supply voltage	1.8V	1.2V	0.5V	1.8V
Samples	80kS/s	50MS/s	4kS/s	200MS/s
Resolution	8 bit	10 bit	8bit	8 bit
Power Consumption	164.97mW	980µW	100mW	12.3nW