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Photovoltaic Grid-connected Power System with Common Mode Leakage Current Elimination using an Improvised Transformer less Inverter

Mohammed Safique[1], Dr. Harikumar Naidu[2]

*[1]Department of Electrical Engineering, Anjuman College of Engineering and Technology, Sadar, Nagpur, Maharashtra, India
[2]Department of Electrical Engineering, T.G.P. College of Engineering & Technology, Nagpur Maharashtra, India

ABSTRACT

To remove the common-mode leakage current in the transformer less photovoltaic grid-connected system, an improved single-phase inverter topology is presented. The improved transformer less inverter can use the same low input voltage as the full-bridge inverter and guarantee to completely meet the condition of eliminating common-mode leakage current. Both the unipolar sinusoidal pulse width modulation (SPWM) along with the double frequency SPWM control strategy can be used to implement the three-level output in the presented scheme. The high efficiency and convenient thermal design are achieved due to the decoupling of two extra switches connected to the dc side. Moreover, the higher frequency and lower current ripples are achieved by using the double-frequency SPWM, and thus the total harmonic distortion of the grid-connected current are minimised. Furthermore, the effect of the phase shift between the output voltage and current, and the influence of the junction capacitances of the power switches are studied in detail. Simulation for unipolar and bipolar SPWM are being carried out to validate the result.

Keywords: Common-Mode Leakage Current, Junction Capacitance, Phase Shift, Photovoltaic (PV) System, Sinusoidal Pulse Width Modulation (SPWM) Strategy, Transformer Less Inverter.

I. INTRODUCTION

Of late the gird-connected photovoltaic (PV) systems, especially the low-power single-phase systems, call for high efficiency, small size, light weight, and low-cost grid connected inverters. Most of the commercial PV inverters use either line-frequency or high-frequency isolation transformers. However, line-frequency transformers are large and heavy, making the whole system bulky posing difficulty in installation. Topologies with high-frequency transformers commonly include many power stages, increasing the complexity at a reduced efficiency [1]–[6]. Consequently, the transformer less configuration for PV systems is developed to offer the advantages of high efficiency, high power density, and low cost. Unfortunately, there are some safety issues because a galvanic connection between the grid and the PV array exists in the transformer less systems. A common-mode leakage current flows through the parasitic capacitor between the PV array and the ground once a variable common-mode voltage is generated in transformer less grid-connected inverters [7]–[12].

The common-mode leakage current increases the system losses,reducing the current quality and induces high degree of electromagnetic interference posing hazards [7], [13]. To avoid the common-mode leakage current, As a solution the half-bridge inverter or the full-bridge inverter with bipolar sinusoidal pulse width modulation (SPWM), is used eliminating the common-mode voltage . However, the half-bridge inverter requires a high input voltage which is greater than, approximately, 700V for 220-Vac applications. As a result, either large numbers of PV modules in series are involved or a boost dc/dc converter with extremely high-voltage conversion ratio is required as the first power processing stage. The full-bridge inverter just needs half of the input voltage demanded by the half-bridge topology, which is about 350V for 220-Vac applications. But the main drawback is that the full bridge inverter can only employ the bipolar SPWM strategy with two levels, which induces high current ripple, large filter inductor, and low system efficiency. Furthermore, the half-bridge neutral point clamp (NPC) inverter is applied to achieve three or more level output. However, NPC inverter also demands the high input voltage the half-bridge inverter does [8], [14]. Therefore, many advanced inverter topologies for transformerless PV applications were developed such as H5 inverter, HERIC inverter, etc. [17]–[25], as shown in Fig. 1. These topologies need the same low input voltage as the full-bridge inverter and can adopt the unipolar SPWM strategy with three levels. The conclusion drawn from [17]–[25] is that various solutions are being researched and employed in transformer less inverters to minimize the common-mode leakage current and improve the efficiency, weight, and size of the whole PV grid-connected power system.

In this paper, an improved grid-connected inverter topology for transformerless PV systems for three phase is presented, which can sustain the same low input voltage as the full-bridge inverter and guarantee not to generate the common-mode leakage current. Furthermore, both the unipolar SPWM and the double-frequency SPWM with three-level output can be applied in the presented inverter. The high efficiency and convenient thermal design are achieved by adopting the unipolar SPWM.

Moreover, the higher equivalent frequency and lower current ripples are obtained by using the double-frequency SPWM. Therefore, a smaller filter inductor can be employed and the harmonic contents and total harmonic distortion (THD) of the output current are reduced greatly, and the grid-connected power quality is improved accordingly.

This paper is organized as follows. The condition of eliminating common-mode leakage current is analyzed in Section II. The improved inverter topology and correlative operation modes under two SPWM control strategies are introduced in Section III. The influence of the power switches' junction capacitances is illustrated in Section IV. The simulated and experimental results are shown in Section V to explore the performance of the presented inverter. Section VI summarizes the conclusions drawn from the investigation.

II. CONDITION OF ELIMINATING COMMON MODE LEAKAGE CURRENT

Common mode voltage of three phase transformer less z source inverter for PV based grid connected system has been discussed and based on the equation presented there the common mode voltage (CMV) can be calculated in same manner. The proposed method is a transformer less grid connected system. There is possibility to flow of leakage current to ground from a PV panel because of a galvanic connection between PV cell and grid.

The common mode voltage (CMV) of three phase inverter can be calculated.

$$v_{CM} = \frac{v_{An} + V_{Bn} + v_{Cn}}{3} \quad \text{-------(1)}$$

The common mode voltage of inverter with refer to negative terminal is expressed as

$$v_{Nn} = -\frac{v_{An} + V_{Bn} + v_{Cn}}{3} \text{h-} \quad \text{---------(2)}$$

III. IMPROVED INVERTER TOPOLOGY AND OPERATION MODES

Fig. 1 shows the improved grid-connected inverter topology, which can meet the condition of eliminating common-mode leakage current. In this topology, two additional switches $S5$ and $S6$ are symmetrically added to the conventional full-bridge inverter, and the unipolar SPWM and double-frequency SPWM strategies with three-level output can be achieved.

A. Unipolar SPWM Strategy

Like the full-bridge inverter with unipolar SPWM, the improved inverter has one phase leg including $S1$ and $S2$ operating at the grid frequency, and another phase leg including $S3$ and $S4$ commutating at the switching frequency. Two additional switches $S5$ and $S6$ commutate alternately at the grid frequency and the switching frequency to achieve the dc-decoupling states. Accordingly, four operation modes that generate the voltage states of $+U$dc, 0, $-U$dc are shown in Fig. 4.

Fig. 5 shows the ideal waveforms of the improved inverter with unipolar SPWM. In the positive half cycle, *S*1 and *S*6 are always ON. *S*4 and *S*5 commutate at the switching frequency with the same commutation orders. *S*2 and *S*3 , respectively, commutate complementarily to *S*1 and *S*4 .

Accordingly, *Mode 1* and *Mode 2* continuously rotate to generate+*U*dc and zero states and modulate the output voltage. Likewise, in the negative half cycle, *Mode 3* and *Mode 4* continuously rotate to generate –*U*dc and zero states as a result of the symmetrical modulation.

Mode 1: when *S*4 and *S*5 are ON, *u*AB = +*U*dc and the inductor current increases through the switches *S*5 , *S*1 , *S*4 , and *S*6 .

Mode 2: when *S*4 and *S*5 are turned OFF, the voltage *u*AN falls and *u*BN rises until their values are equal, and the antiparallel diode of *S*3 conducts. Therefore, *u*AB = 0V and the inductor current decreases through the switch *S*1 and the antiparallel diode of *S*3 .

Mode 3: when *S*3 and *S*6 are ON, *u*AB = −*U*dc and the inductor current increases reversely through the switches *S*5 , *S*3 , *S*2 , and *S*6 .

Mode 4: when *S*3 and *S*6 are turned OFF, the voltage *u*AN rises and *u*BN falls until their values are equal, and the antiparallel diode of S4 conducts. Similar as to *Mode 2*, *u*AB = 0V and the inductor current decreases through the switch *S*2 and the antiparallel diode of *S*4 . The common-mode voltage *u*cm also keeps *U*dc/2 referring to (9). From (8) to (10), the common-mode voltage can remain a constant *U*dc/2 during the four commutation modes in the improved inverter with unipolar SPWM. The switching voltages of all commutating switches are half of the input voltage*U*dc /2, and thus, the switching losses are reduced compared with the fullbridge inverter. Furthermore, in a grid period, the energies of the switching losses are distributed averagely to the four switches *S*3 , *S*4 , *S*5 , and *S*6 with high-frequency commutations, and it benefits the thermal design of printed circuit board and the life of the switching components compared with H5 inverter.

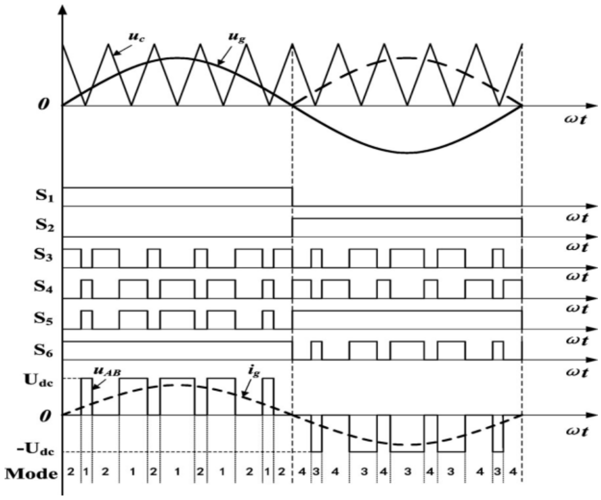

Figure 1. Ideal waveforms of the improved inverter with unipolar SPWM

B. Double-Frequency SPWM Strategy

The improved inverter can also operate with the double frequency SPWM strategy to achieve a lower ripple and higher frequency of the output current. In this situation, both phase legs of the inverter are, respectively, modulated with 180◦ opposed reference waveforms and the switches *S*1–*S*4 all acting at the switching frequency. Two additional switches *S*5 and *S*6 also commutate at the switching frequency cooperating with the commutation orders of two phase legs. Accordingly, there are six operation modes to continuously rotate with double frequency and generate +*U*dc and zero states or −*U*dc and zero states, with double-frequency SPWM.

In the positive half cycle, *S*6 and *S*1 have the same commutation orders, and *S*5 and *S*4 have the same orders. *S*2 and *S*3 , respectively, commutate complementarily to *S*1 and *S*4 . Accordingly, *Mode 1*, *Mode 2*, and *Mode 5* continuously rotate to generate +*U*dc and zero states and modulate the output voltage with double frequency. In the negative half cycle, *Mode 3, Mode 4* and *Mode 6* continuously rotate to generate −*U*dc and zero states with double frequency due to the completely symmetrical modulation.

Mode 5: when *S*1 and *S*6 are turned OFF, the voltage *u*AN falls and *u*BN rises until their values are equal, and the anti parallel diode of *S*2 conducts. Therefore, *u*AB = 0V and the inductor current decreases through the switch *S*4 and the antiparallel diode of *S*2 . The common-mode voltage *u*cm keeps a constant *U*dc/2 referring to (9).

Mode 6: similarly, when*S*2 and*S*5 are turned OFF, the voltage *u*AN rises and *u*BN falls until their values are equal, and the antiparallel diode of $S1$ conducts. Therefore uAB = 0V and the inductor current decreases through the switch $S3$ and the antiparallel diode of $S1$. The common-mode voltage $u$cm still is a constant Udc/2 referring to (9). Under the double-frequency SPWM strategy, the commonmode voltage can keep a constant Udc/2 in the whole switching process of six operation modes. Furthermore, the higher frequency and lower current ripples are achieved, and thus, the higher quality and lower THD of the grid-connected current are obtained, or a smaller filter inductor can be employed and the copper losses and core losses are reduced.

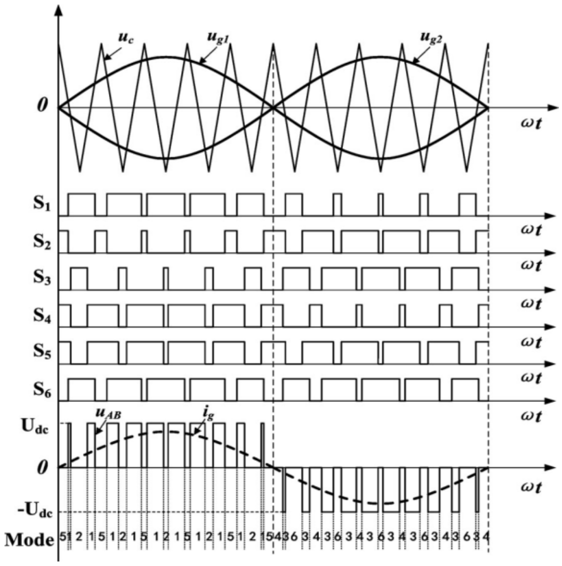

Figure 2. Ideal waveforms of the improved inverter with double-frequency SPWM.

IV. SIMULATION

Simulation have been carried out for unipolar and bipolar SPWM control strategies.

A) Simulations employing Unipolar SPWM

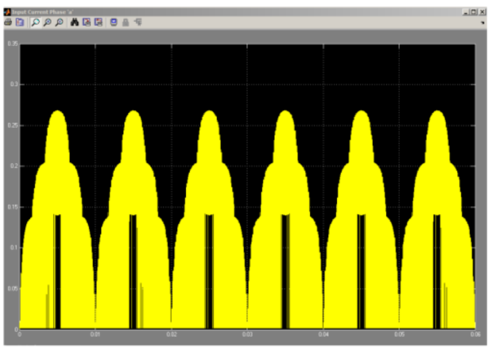

Figure 3. Input current phase A

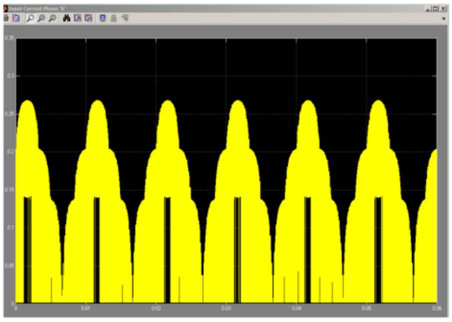

Figure 4. Input current phase B

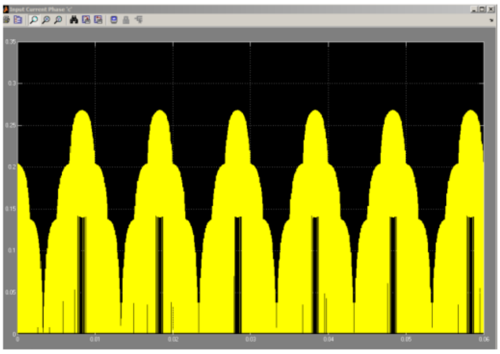

Figure 5. Input Current Phase C

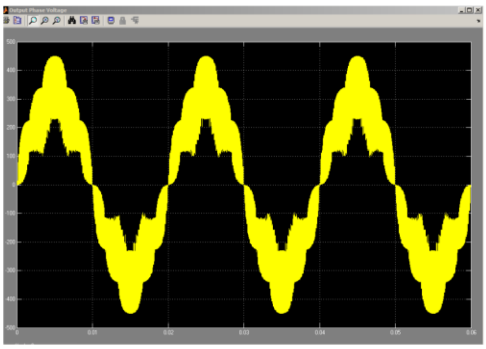

Figure 6. Output phase voltage

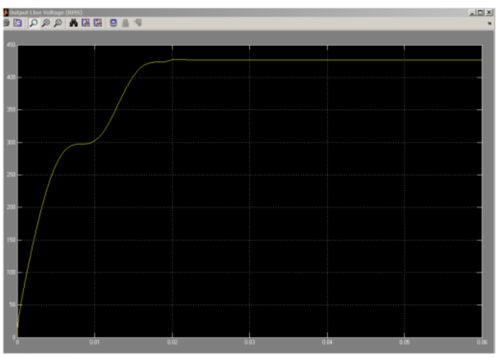

Figure 7. Output line voltage (rms)

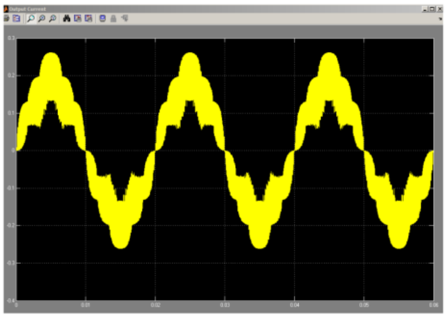

Figure 8. Output current

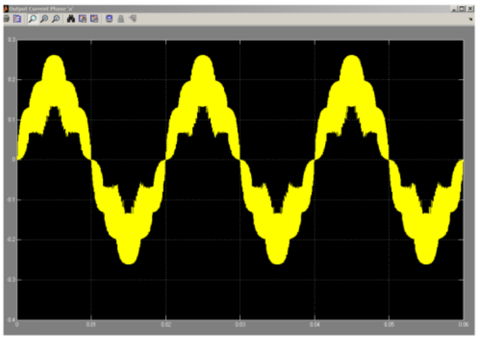

Figure 9. Output current phase A

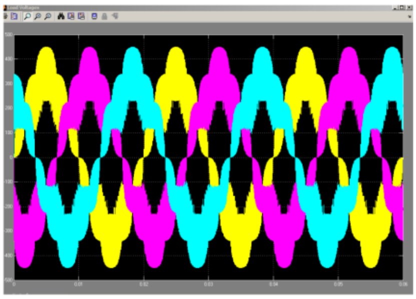

Figure 10. Load voltages

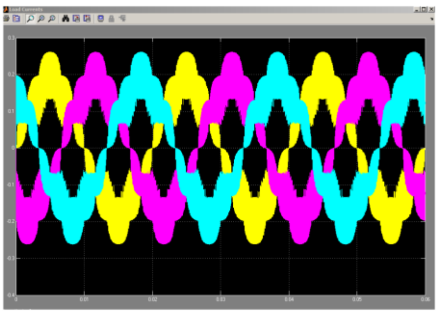

Figure 11. Load currents

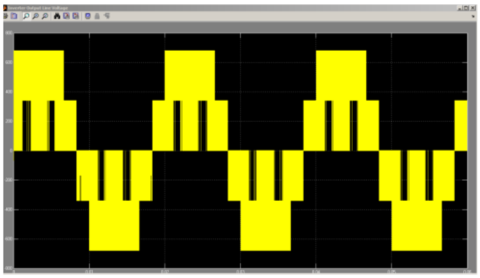

Figure 12. Inverter output line voltage

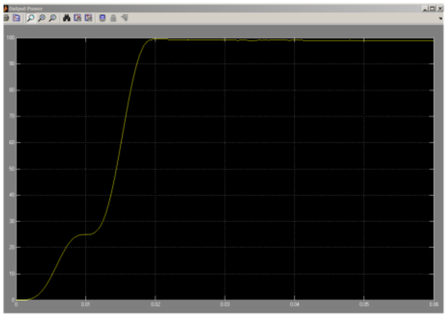

Figure 13. Output power

A) Simulations employing Bipolar SPWM

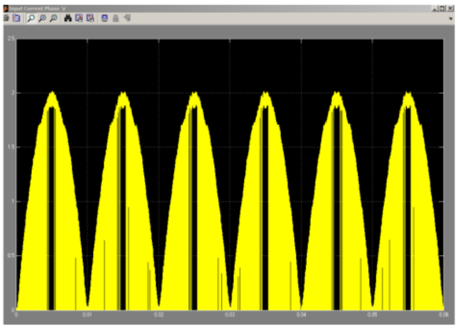

Figure 14. Input Current Phase A

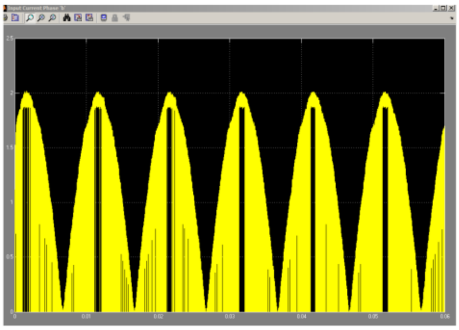

Figure 15. Input Current Phase A

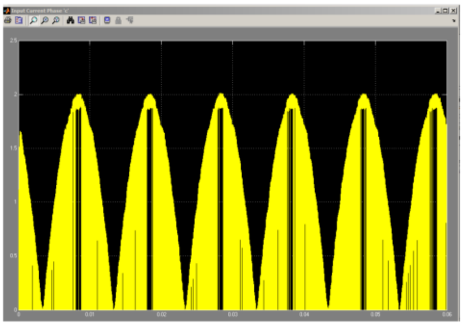

Figure 16. Input Current Phase C

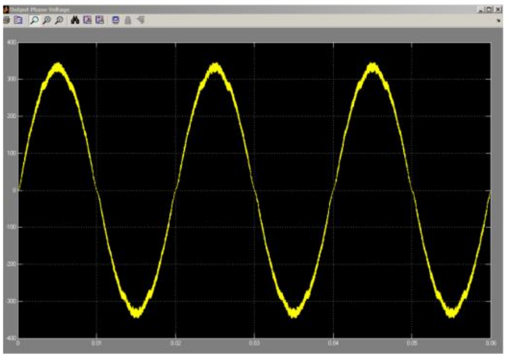

Figure 17. Output Phase Voltage

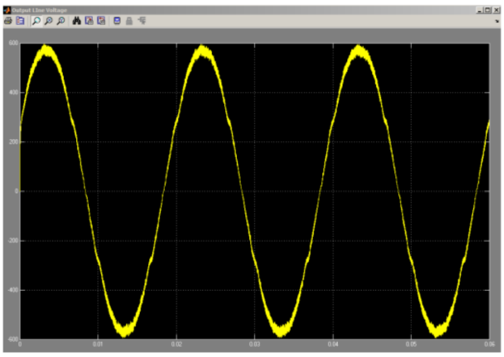

Figure 18. Output Line Voltage

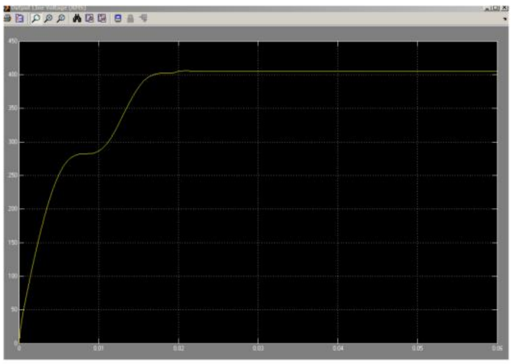

Figure 19. Output Line Voltage(rms)

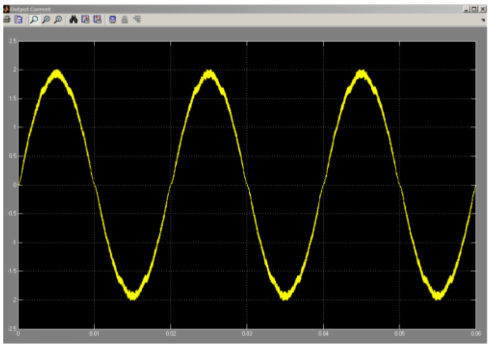

Figure 20. Output power

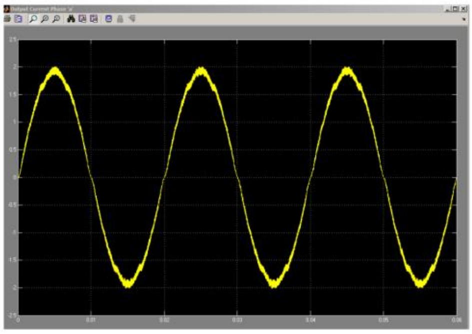

Figure 21. Output Current Phase A

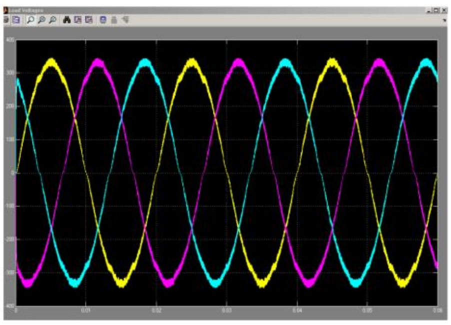

Figure 22. Load Voltages

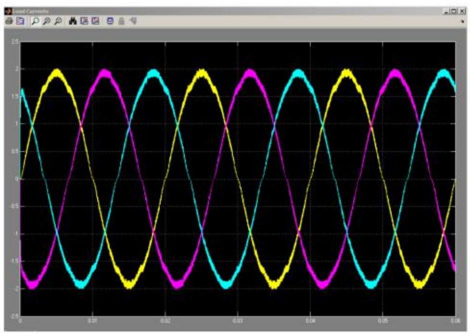

Figure 23. Load Current

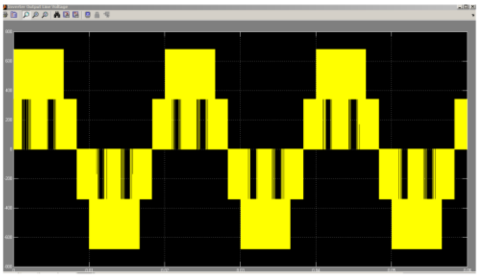

Figure 24. Inverter Outpur Line Voltage

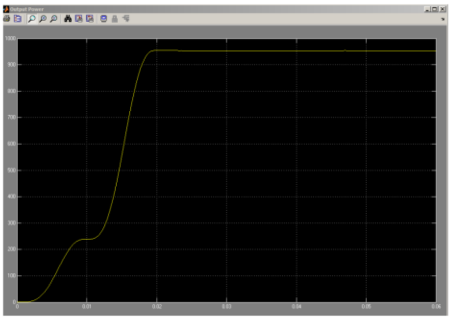

Figure 25. Output Power

Table I. Measured Efficiency of the Improved Inverter

Output power		10%	25%	50%	75%	100%
		100W	250W	500W	750W	1000W
Unipolar SPWM	Efficiency(%)	89.29	96.31	97.24	97.51	97.64
Double Frequency SPWM		87.11	93.6	96.65	96.66	96.61
Unipolar SPWM	THD(Ig)	25.42	14.5	7.96	5.46	4.19
Double Frequency SPWM		16.99	8.23	4.73	3.58	2.84

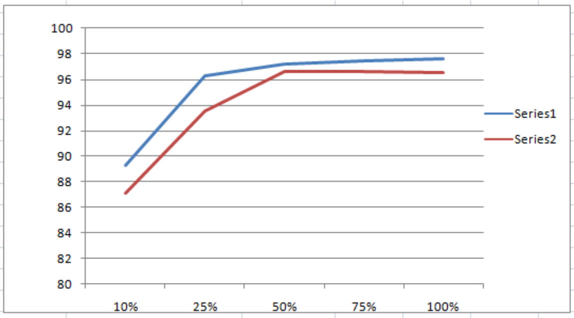

Figure 26. Measured Efficiency

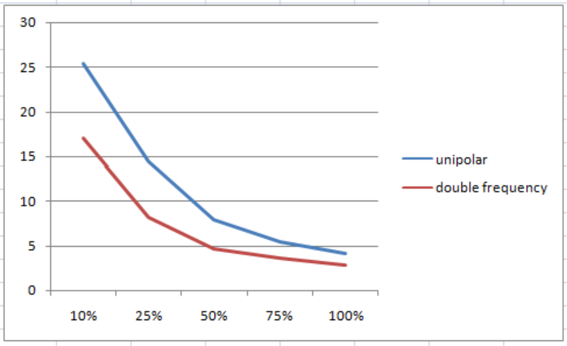

Figure 27. Measured THD

V. CONCLUSION

This paper presented to eliminate common mode leakage current problem in transformer less inverter is solved by using the improved transformer less inverter. The improved topology has decoupling of two additional switches S5 and S6 connected in the dc side of the inverter topology for transformer less PV systems. The unipolar SPWM control strategies is implemented with three-level output in the presented inverter, which can eliminate the common-mode leakage current because the condition of eliminating common-mode leakage current is met.

The unipolar scheme gives a better efficiency for different values of rated output but gives a poor THD as compared to the Bipolar scheme.

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