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Evaluation of Canny and Sobel Edge Detection Technique using Xilinx System Generator

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ABSTRACT

Edge detection is the first step in many computer vision applications. Edge detection of image significantly reduces the amount of data and filters out unwanted or insignificant information and gives the significant information in an image. This information is used in image processing to detect objects in which there are some problems like false edge detection, missing of low contrast boundaries, problems due to noise etc. The aim of this paper is to develop an edge detection which automatically detects edges of digital image. The complete design of sobel edge algorithm using sobel filter and canny edge detector algorithm followed by the Gaussian filtering and gradient filter is done on Xilinx System Generator (XSG).The complete design combines MATLAB, Simulink and XSG. The VHDL code is generated by using Xilinx system generator (XSG). Further the generated VHDL code is synthesize in Xilinx ISE Design Suit 13.1. The Edge Detection method has been verified successfully with no visually perceptualerrors in the resulted images and also comparing theboth filters with an individually performance is justified clearly with Practical and Theoretical

Keywords : XSG, Canny, Sobel, VHDL,Gaussian Filter

I. INTRODUCTION

In lower level image processing edge detection plays very important role. Quality of detected edges has significant role in image segmentation, scene analysis, focused area Selection, object recognition. For accurate edge extraction, both changes in the colour and changes in the brightness between neighboring pixels should be demoralized. Many forceful and complex edge detection techniques have been presented in the previous literatures. These provide different outputs and particulars to the same input image. Here Sobel operator based edge detection technique is used and is extended for real-time applications. Due to the property of counteracting the noise sensitivity Sobel operator for edge detection over other gradient operators are chosen. The Sobel operator commonly known as Sobel filter is used for image processing and computer vision, which creates an image which focuses edges and transitions. It is discrete differentiation operator that calculates the gradient approximation of the image intensity function. The result of the Sobel operator is the corresponding gradient vector at that particular point. The Sobel operator convolves the image with an integer valued filter in vertical and horizontal direction so it is thus relatively cheaper in terms of computations. The gradient estimation that it produces is relatively simple for high frequency variations in the image. A Xilinx tool, the System Generator for DSP offers an efficient and straight forward method for transitioning from a PC-based model in Simulink to a real-time FPGA based hardware implementation. The system model can be simulated in the Simulink environment. This higher abstraction level reduces the analysis and debugging time. For real hardware testing, Xilinx System Generator supports the possibility to perform hardware in-the-loop co-simulation [2].This methodology provides easier hardware verification and implementation compared to HDL based approach. The Simulink simulation and hardware-in-the loop approach presents a far more cost efficient solution than other methodologies. The ability to quickly and directly realize control system design as a real-time embedded system greatly facilitates the design process. The goal of this project was to implement an

image processing algorithm applicable to Edge Detection system in a Xilinx FPGA using System Generator for DSP, with a focus on achieving overall high performance, low cost and short development time.

II. LITRATURE SURVEY

Qian Xu, Chaitali Chakrabarti and Lina J. Karam, "A Distributed Canny edge detector and its implementation on FPGA". This paper describe the Canny edge detector and its implementation on FPGA.Edge detection is one of the key stages in image processing and object recognition. The Canny edge detector is one of the most widely-used edge detection algorithm due to its good performance. We present a distributed Canny edge detection algorithm that results in significantly reduced memory requirements, decreased latency . this results in a significant speed up without ssecrificing the edge detection performance. The computational cost of the proposed algorithm is very low compared to the original Canny edge detection algorithm.[1].

F. M. Alzahrani and T. Chen "A real-time edge detector algorithm and VLSI architecture, this paper present an absolute different mask (ADM) edge detection algorithm and its pipelined VLSI architecture for real time application .But the edge detector in offers a trade-off between precision cost and speed, and its capability to detect edges is not as good as the Canny algorithm. There is another set of work on Deriche filters that have been derived using Canny criteria. [2]

D. V. Rao and M. Venkatesan, "An efficient reconfigurable architecture and implementation of edge detection algorithm using Handle-C," the approach of this paper is to operates on two rows of pixel at a time ,this reduces the memory requirement at the expense of a decrease in the throughput. Furthermore it is known that the original Canny edge detection algorithm needs two adaptive image dependent high and low thresholds to remove false edges. However, the algorithm in just fixes high and low thresholds in order to overcome the dependency between the blocks which results in a decreased edge detection performance.[4]
S . Varadarajan , C. Chakrabarti, L. J. Karam, and J. M. Bauza, "A distributed psycho-visually motivated Canny edge detector ;" In this paper we proposed a new threshold selection algorithm based on the distributed of pixel gradients in a block of pixel to overcome the dependency between the blocks ,however in hysteresis thresholds calculation is based on a very finely and uniformly quantized 64 bit gradient magnitude histogram, Which is use in real time implementation.[5]

III. SYSTEM DESIGN AND FUNCTION

Architecture of Sobel and Canny Algorithm

The purpose of the design phase is to plan a solution of the problem specified by the requirement document. This phase is the first step-in moving from the problem domain to the solution domain. The design of the system is perhaps the most critical factor affecting the quality of the hardware implementation. Here we build the System Block Diagram that is helpful to understand the behavior of the system. In the proposed work entire system is divided into following:

1. Input image from image block MATLAB
2. Convert RGB to Gray block
3. Image Edge detection using Sobel & Canny Operator.
4. Conversion of image in MATLAB

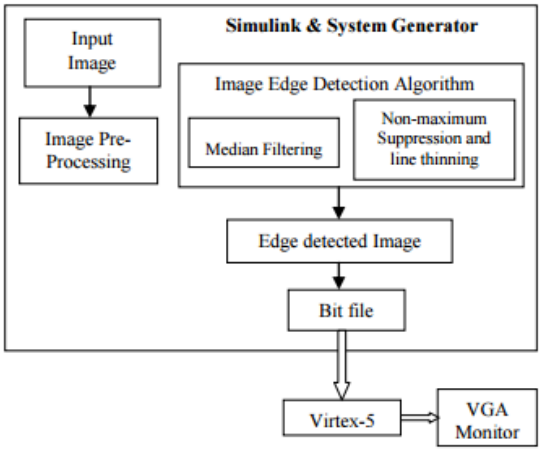

Figure 1. System Block Diagram

The overall system consists of following blocks image input, image pre-processing, image edge detection algorithm, FPGA board, Output on VGA monitor. The Simulink models are generated for system using Simulink block sets, which are present in MATLAB/Simulink. Input image used is image stored in memory. Then the resizing and preprocessing is done using the median filtering on the image to reduce noise which is present in the input image. After preprocessing

the edge detection of the image is done and then the post processing is done using the non-maximum suppression and line thinning. The edge image is then detected with the help of Matlab/Simulink model. The Xilinx Platform Studio (XPS) is used to interface peripherals [4]. Then XPS along with xillinx ISE 14.1 generate a .bit file for the edge image and then downloaded to FPGA.

1) Input Image: Input image is a digital image which is of different formats such as .jpg, .bmp, .jpeg, .tiff, .gif, .png which are stored in memory. These images are color as well as black and white images. These images are converted from RGB to gray colour using the MATLAB code. These images are selected in the Simulink model using the 'image from file/workspace' block. The size of the stored image is resized to 512X512 in the MATLAB code.

2) Image edge detection Algorithm: Here Canny edge detection algorithm is implemented on FPGA board, which is implemented in following steps: pre-processing, gradient calculation, non-maximum suppression, double thresholding, hysteresis. These steps are explained in detailed in next section.
The Virtex-5 ML506 evaluation board is user friendly which is used to realize this system. For this system awfully fewer hardware is required such as RS232, JTAG cable and VGA monitor. The downloading process of Virtex-5 is easy to understand. This FPGA board gives especially rapid results.

A. Software Design In this paper, image edge detection algorithm is used for the detection of edges of object. The Fig. 2 shows the flow of the Canny edge detection algorithm.

1) Image pre-processing: Basically in many image processing applications input image is colour image. Here also input image is colour image. For edge detection purpose no any colour information is required so second step to minimize this unnecessary colour data. For this data reduction image is converted into grayscale image. This grayscale image containing some noise in it so filtering is applied. Median filter is preferred for this purpose.

2) Convolution with masks, Gradient and direction Calculation: Here, suppose G (x, y) is a 2D Gaussian mask and I(x, y) is the image, the first-order derivative of Gaussian is gx(x, y) and gy(x, y). Then the gradient of vertical direction Ex(x, y) and horizontal direction Ey (x, y) can be computed by the following equations:

$$G(x,y) = \frac{1}{2\pi\sigma^2}\{e^{(\frac{x^2+y^2}{2\sigma^2})}\} \quad (1)$$

$$gx(x,y) = \frac{\partial G}{\partial x} = \frac{1}{\pi\sigma^2}x\{e^{(-\frac{x^2+y^2}{2\sigma^2})}\} \quad (2)$$

$$gy(x,y) = \frac{\partial G}{\partial y} = \frac{1}{\pi\sigma^2}y\{e^{(-\frac{x^2+y^2}{2\sigma^2})}\} \quad (3)$$

$$Ex(x,y) = gx(x,y) * I(x,y) \quad (4)$$

$$Ey(x,y) = gy(x,y) * I(x,y) \quad (5)$$

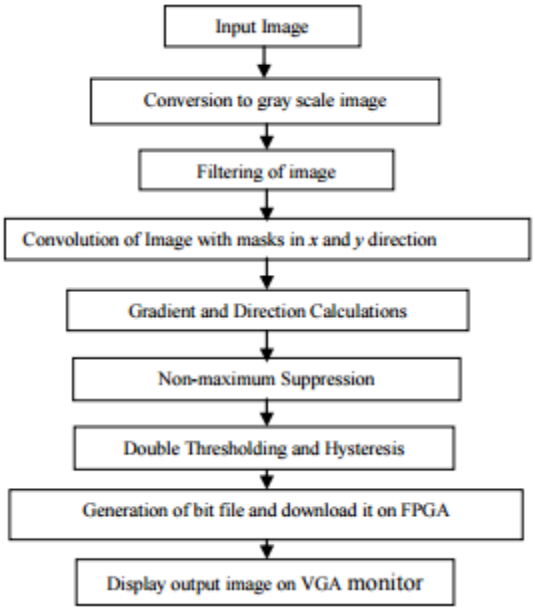

Figure. 2 Flow of Canny Edge Detection Algorithm

IV. RESULT

The proposed work is implemented by using MATLAB Simulink and XSG (Xilinx System Generator) with Xilinx blocksets. The method was tested on standard test image like „cameraman". The output results show an image filtered from Gaussian filtering, another output is hysteresis throsholding output which removes streaking form an image. Final image is of Canny Edge Detected Syed Sameer Rashid et al VHDL Based Canny Edge Detection Algorithm 752 |International Journal of Current Engineering and Technology, Vol.4, No.2 (April 2014) image. The generated system is targeted for VIRTEX 5 starter kit. Further the VHDL code is generated by using System Generator token, this code is perfectly synthesized in ISE 13.1 Design Suit. After synthesis the device resource usage summary was produced for the targeted device.

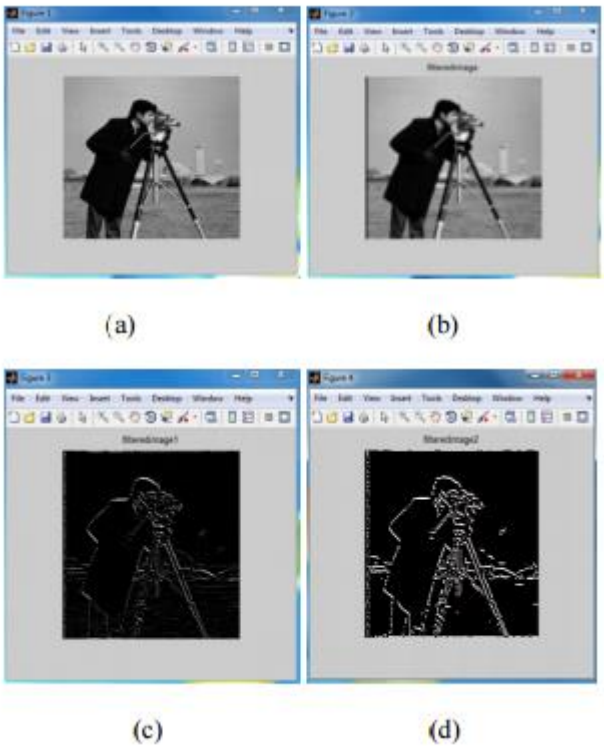

Figure 3 : (a) Original Image (c) Gaussian Filtering Result (c) Hysteresis Throsholding Result (d) Canny Edge Detection

Result The device utilization summary is estimated for the proposed design. Performance of this architecture implemented in Vertex5 (xc5vsx50t-1ff1136) as shown in Table. The proposed architecture provides lower complexity as well as improves efficiency in area. It also provides good choice in terms of low cost hardware

V. CONCLUSION

This paper is present of Xilinx System. Generator development tools Edge Detection For Images Processing System .Comparing the results using matlab with two familiar edge detection methods Sobel and Canny . By observing the synthesis results we concluded that Canny edge detection method gives sharp edge image compare to sobel method.Future works include the use of the Xilinx System. Generator development tools for the implementation of other blocks used in computer vision like feature extraction and object detectionon Xilinx Programmable Gate Arrays (FPGA)

VI. REFERENCES

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