International Journal of Scientific Research in Science and Technology
Available online at : www.ijsrst.com
Print ISSN: 2395-6011 | Online ISSN: 2395-602X
doi : https://doi.org/10.32628/IJSRST

Design And Analysis of Low Power Single Exact Adder Dual Approximate Adder

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ARTICLEINFO

Article History:

Accepted: 10 March 2024
Published: 23 March 2024

Publication Issue :
Volume 11, Issue 2
March-April-2024
Page Number :
313-320

ABSTRACT

The notion of approximation computing has attracted a great deal of interest and recognition, primarily because of its noteworthy benefits with respect to energy efficiency in a variety of applications that are somewhat error-tolerant. The current study offers a suggested adder that is ideal for processor integration since it can execute dual approximate addition (SEDA) and n-bit single exact addition. In this study, approximate adders with dynamic runtime reconfigurability between accurate and approximate modes at the circuit level are designed. In this paper, we present the idea of highly configurable Single Exact Single Approximate (SESA) adders, which provide fine control over the trade-off between exact and approximate computing modes. Furthermore, we introduce the Single Exact Dual approximation (SEDA) adder, which provides the option to adjust the granularity level between exact and approximation modes. The SEDA adder, as opposed to SESA adders, makes it easier to carry out two approximation computations simultaneously. For both the SESA and SEDA adders, the maximum bounded error is present. After being installed at a 32nm technology node, the Tanner EDA tool was used to evaluate the SESA and SEDA adders.

Keywords : Mirror adder, SEDA adder, Power consumption, Voltage scaling, Error mitigation

I. INTRODUCTION

Because approximate computing offers enormous energy and performance improvements for error-tolerant applications, it has become more important in the last ten years. We discuss approximation adders in this study and offer a novel approach to designing runtime configurable approximate adders. The creation of approximation mirror adders was among the earliest achievements in the field of approximate

circuits. Pass transistor logic (PTL) has been used in other works on approximate adders, but because of their limited noise margins, PTLs are especially unsuitable for lower technology nodes. We used the mirror adder as the foundation for our study.

Throughout the history of single bit approximate adder design, runtime configurability has not been taken into account in any of the prior works. Nonetheless, having both exact and approximate additions with a knob to switch between them is preferable in a realistic setting. The goal of approximation designs is defeated by the expense in energy, time, and area associated with having both exact and approximate adders. In this work, we present a revolutionary methodology that uses only 30% energy usage and 13% delay to develop an approximate adder alongside a 1-bit accurate adder. The contributions of our work are, the Single Exact Dual Approximate (SEDA) adder's design is what we suggest. On the same hardware, SEDA can execute two n-bit approximation additions or a single n-bit accurate addition. The motivation behind SEDA arises from the increasing demand for energy-efficient computing systems, particularly in battery-powered devices, Internet of Things (IoT) applications, and portable electronics. Traditional adders, while accurate, often consume a significant amount of power due to their precise computation processes. On the other hand, approximate adders sacrifice accuracy for power efficiency by providing slightly erroneous results.

The organizational framework of this study divides the research work in the different sections. The Literature survey is presented in section 2. In section 3 and 4 discussed about Existing and proposed system methodologies. Further, in section 5 shown Simulation Results is discussed and Conclusion and future work are presented by last sections 6.

II. LITERATURE SURVEY

The paper titled "Algorithm and VLSI Architecture Designs of a Lossless Embedded Compression Encoder for HD Video Coding Systems" by **Lee** et al. (2021) focuses on the design and implementation of a lossless embedded compression encoder tailored for HD video coding systems. The primary objective of the research is to develop an efficient lossless embedded compression encoder suitable for HD video coding applications [1].

The paper titled "Design and Area Optimization of CMOS Operational Amplifier Circuit Using Hybrid Flower Pollination Algorithm for IoT End-node Devices" by **Sasikumar** et al. (2022) focuses on the design and optimization of a CMOS operational amplifier circuit specifically tailored for IoT (Internet of Things) end-node devices. The primary objective of the research is to design and optimize a CMOS operational amplifier circuit suitable for IoT end-node devices. Operational amplifiers play a crucial role in various analog and mixed-signal applications, including sensor interfaces, signal conditioning, and data acquisition [2].

The paper titled "Comparison of Approximate Computing with Sobel Edge Detection" by **Chung** and Kim (2021) explores the application of approximate computing techniques in the context of Sobel edge detection, a widely used image processing algorithm for detecting edges in images, the primary objective of the research is to compare the performance and effectiveness of approximate computing techniques when applied to Sobel edge detection. Approximate computing aims to trade off accuracy for improvements in speed, power consumption [3].

The paper titled "Comprehensive Study of 1-bit Full Adder Cells: Review, Performance Comparison, and Scalability Analysis" by **Hasan** et al. (2021) conducts a thorough investigation into various 1-bit full adder cells, providing a comprehensive review, performance comparison, and scalability analysis. The primary objective of the research is to conduct an in-depth

study of 1-bit full adder cells. Full adder cells are fundamental building blocks in digital circuits, used in arithmetic operations, data processing, and computing systems [4].

The paper titled "Sam: A Segmentation Based Approximate Multiplier for Error Tolerant Applications" by **Pandey** et al. (2021) presents a novel approach to approximate multiplier design tailored for error-tolerant applications. The primary objective of the research is to propose new approximate multiplier architecture suitable for applications where a certain level of error tolerance is acceptable. Multipliers are fundamental arithmetic units extensively used in digital signal processing, machine learning, and other computational tasks [5].

"High-performance and energy-area efficient approximate full adder for error tolerant applications", by **Mohammadi** et al. (2022), proposes a novel design for a full adder cell that achieves high performance, energy efficiency, and low area usage. This design is particularly well-suited for applications where some errors can be tolerated [6].

"Fault-Free: A Fault-Resilient Deep Neural Network Accelerator Based on Realistic ReRAM Devices" by **Shin** et al. (2021), tackles a critical challenge in deep neural network (DNN) accelerators that utilize Resistive Random-access Memory (ReRAM). The issue lies in inherent device-level imperfections in ReRAM, known as Stuck-At-Faults (SAFs), which can significantly reduce the accuracy of DNN inference [7].

"Reconfigurable and hardware efficient adaptive quantization model-based accelerator for binarized neural network" by **Sasikumar** et al. (2022), proposes a reconfigurable accelerator design for binarized neural networks (BNNs). BNNs are a type of neural network that uses binary weights, which can significantly reduce the memory footprint and computational complexity compared to traditional neural networks with full-precision weights [8].

"Design and Analysis of Majority Logic-Based Approximate Adders and Multipliers" by **Liu** et al. (2019), explores a new design approach for arithmetic circuits used in emerging nanotechnologies. The design leverages the inherent properties of majority logic to create approximate adders and multipliers. This approach potentially reduces circuit complexity and operational delay compared to conventional designs [9].

"Systematic synthesis of approximate adders and multipliers with accurate error calculations" by **Nojehdeh** and Altun (2020) focuses on designing approximate adders and multipliers with a systematic approach. This research proposes a systematic method to design approximate adders and multipliers. They build these circuits from basic building blocks - approximate single-bit adders with various error profiles [10].

III. EXISTING METHOD

An exact mirror adder is a type of digital circuit designed using complementary metal-oxide-semiconductor (CMOS) logic for performing addition. It utilizes the concept of current mirroring to achieve the sum operation. Similar to a traditional full adder, an exact mirror adder takes two binary input bits (A and B) and a carry-in bit (Cin) and outputs the sum (Sum) and carry-out (Cout) of the addition operation. The core idea behind an exact mirror adder is exploiting the ability of transistors in CMOS logic to mirror currents. Specific configurations of transistors are used to create a proportional relationship between the currents flowing through them. The Exact Mirror Adder is a type of digital adder circuit used in binary arithmetic. It's designed to perform addition by exploiting the symmetry in the binary representation of numbers. In binary addition, a carry bit is generated when the sum of two bits in a column exceeds 1. The Exact Mirror Adder exploits the symmetry in binary addition, meaning that for every possible combination

of input bits, there's a mirror combination that produces the same output. This property allows the Exact Mirror Adder to compute the sum of two binary numbers by simultaneously generating the mirror inputs and using an appropriate selection circuit to determine the correct output. By taking advantage of this symmetry, the number of transistors and logic gates required can be reduced compared to traditional binary adders, leading to potential improvements in speed and efficiency. Exact Mirror Adders can be implemented using different logic families such as CMOS, TTL, or other digital logic technologies. They are particularly useful in applications where efficiency and speed are critical, such as in high-performance computing and digital signal processing. The block diagram of existing method is shown in figure 1.

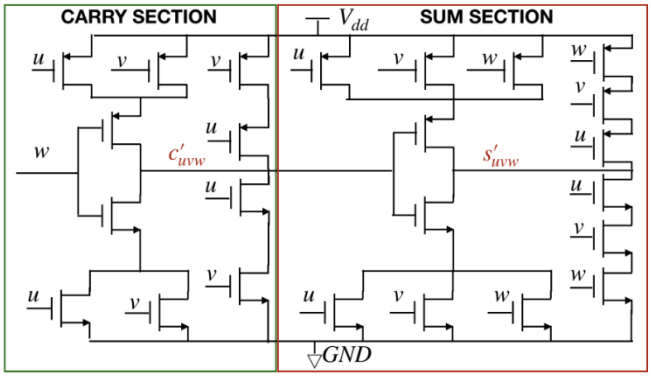

Figure 1. Block diagram of Existing Method

IV. PROPOSED METHOD

In the SEDA addition, we refrain from approximating the carry value to preserve a limited error range. The inaccuracy can spread to the highest important bit when the carrying value of the bit with the lowest importance is determined using an n-bit addition. Regarding the SEDA method, we merely make an approximation for the total, suvw, equal to c ′ uvw. Therefore, in the case of an n-bit approximation, the highest possible error is expected to be equal to 2n -1. By examining the truth table associated with a full-adder, it becomes obvious that the total output only contains errors when the given values of {u,v,w} are '000' and '111', while the carry bit remains error-free.By employing the approximation above, we can split the 1-bit precise mirror adder circuitry into two parts, enabling us to carry out two 1-bit approximation additions. The SEDA addition provides accurate carry outcomes for consecutive 1-bit additions, ensuring the error remains within a defined limit. In addition, the design has been rendered adjustable by incorporating multiplexers that are carried out employing transmission gates regulated by an input source/drain, as illustrated in Figure 2. By using n-SEDA adders, we can execute the exact addition of a 1-bit n-bit number or approximation addition of two n-bit numbers. Despite the addition of 5 muxes, power consumption is still used during switching a transistor's gates due to a substantial gate capacitance. Due to the typical occurrence of switching the gate input of the Transmission Gate whenever transitioning from an approximation method to an accurate mode of operation, the resulting power consumption is minimal.

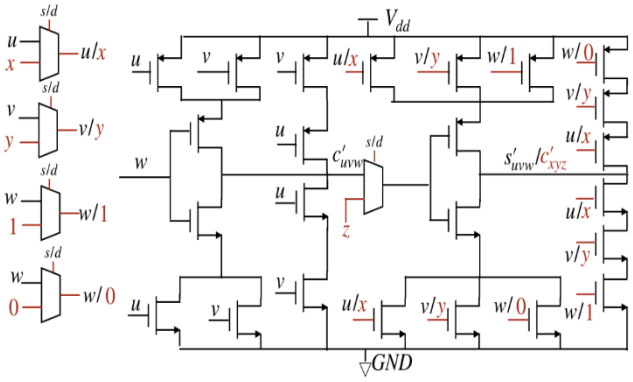

Figure 2. CMOS implementation of SEDA Adder

V. METHODOLOGY

1. Problem Statement

Clearly define the requirements and constraints for the adder. This includes the desired accuracy of the approximate adder, the power budget, speed requirements, and any other relevant specifications.

2. Selection of Adder Architectures:

Choose a suitable architecture for the exact adder. Common options include ripple carry adders, carry-

look ahead adders, or carry-select adders. Consider the trade-offs between speed, area, and power consumption for each architecture. Select an appropriate architecture for the approximate adder. This could involve techniques like using redundant number systems, approximate carry propagation, or approximate logic gates to reduce power consumption at the cost of accuracy.

3. Design of Exact Adder:

Implement the exact adder using the chosen architecture. Optimize the design for low power consumption while meeting the desired performance requirements. Utilize low-power design techniques such as voltage scaling, clock gating, or transistor sizing optimization to minimize power consumption.

4. Design of Exact Adder:

Design the approximate adder to provide a trade-off between accuracy and power consumption. This could involve techniques like approximate carry propagation, simplified logic gates, or error-tolerant arithmetic.Analyze the impact of approximation on the accuracy of the adder and ensure that it meets the required specifications.

FLOW DIAGRAM

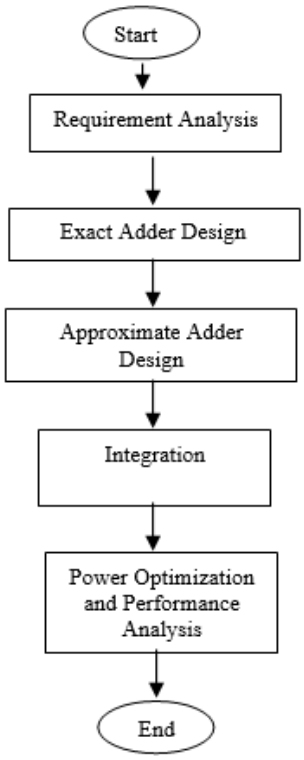

Figure 3. Flow Diagram

1. **Start:**
- The process begins with the start symbol, indicating the initiation of adders.

2. **Requirement Analysis:**
- Understand the requirements for the adder in terms of precision, speed, power consumption, and area.

3. **Exact Adder Design:**
- Design a low-power exact adder using techniques such as reduced transistor count, low-voltage operation, or other optimization methods.
- Simulate and verify the exact adder's performance in terms of power consumption, speed, and area.

4. **Approximate Adder Design**
- Design a dual approximate adder that can provide fast but slightly less accurate results compared to the exact adder.
- Select approximation techniques like operand truncation, bit skipping, or approximate logic.
- Simulate and verify the approximate adder's performance, including its error rate, speed, and power consumption.

5. **Integration**
- Integrate the exact adder and approximate adder modules into a single design.
- Implement necessary control logic for selecting between exact and approximate modes

6. **Power Optimization and Performance Analysis:**
- Analyse power consumption at various stages of the adder operation.
- Apply power optimization techniques such as clock gating, voltage scaling, or power gating.
- Evaluate the performance of the integrated adder in terms of accuracy, speed, and power consumption under different input conditions.

PERFOMANCE METRICS

The proposed method is evaluated through comprehensive simulations, considering various performance metrics:

a. **Power Consumption:** The amount of electrical power used by a device or system. It is a

fundamental parameter for assessing a device's energy efficiency.

b. **Delay:** measuring the amount of time it takes to transfer data from one destination to another

c. **PDPD:** the power–delay product (PDP) is a figure of merit correlated with the energy efficiency of a logic gate or logic family. Also known as switching energy, it is the product of power consumption P (averaged over a switching event) times the input–output delay or duration of the switching event D.

VI. RESULTS AND DISCUSSIONS

The simulation results for the Design and Analysis of Low Power Single Exact Adder Dual Approximate Adder for existing method of mirror adder and proposed method using SEDA are shown in figures 4 to figure 9 respectively.

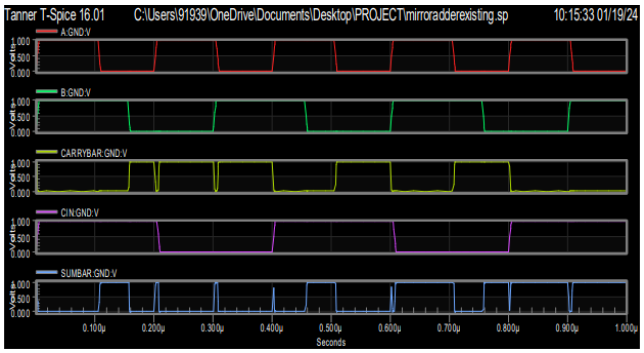

Figure 4. Waveform of mirror adder(existing method)

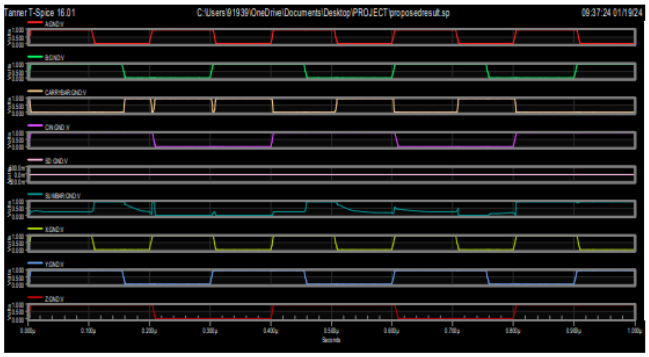

Figure 5. Transient Analysis of proposed SEDA adder in exact adder mode in 32nm

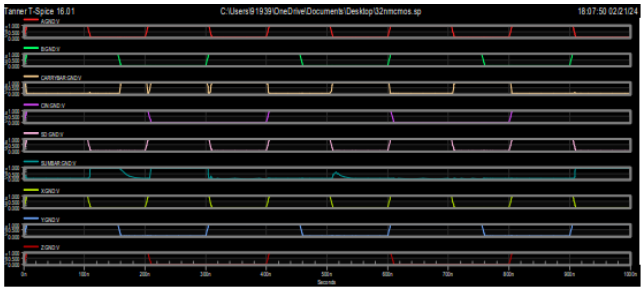

Figure 6. Transient Analysis of proposed SEDA adder in dual approximate mode in 32nm

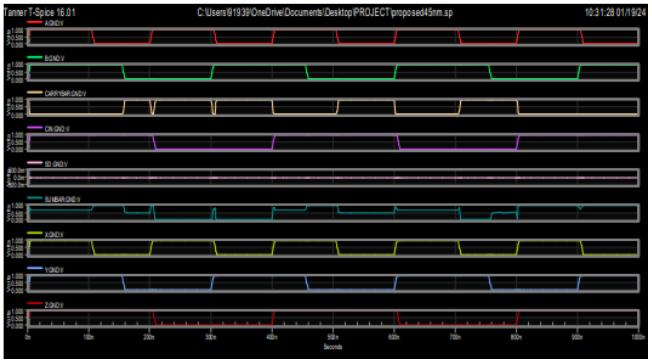

Figure 7. Transient Analysis of proposed SEDA adder in exact adder mode in 45nm

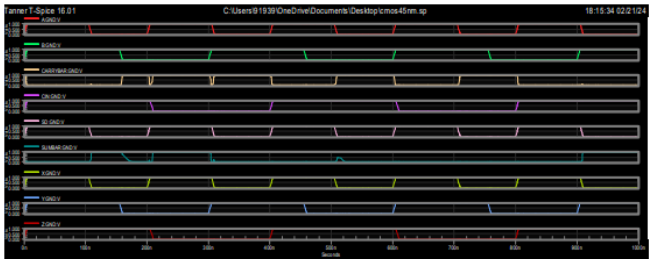

Figure 8. Transient Analysis of proposed SEDA adder in dual approximate mode in 45nm

Prameter	Proposed Adder in 45nm	Proposed Adder in 32nm	Existing Mirror Adder
Power Consumption (W)	**1.748622**	1.59986	3.333393
Delay (Ps)	87.203	45.359	275.05
PDPD(x 10^{-18} WS)	152.48	72.56	915.94

Table 1. Comparison table of Existing and proposed method

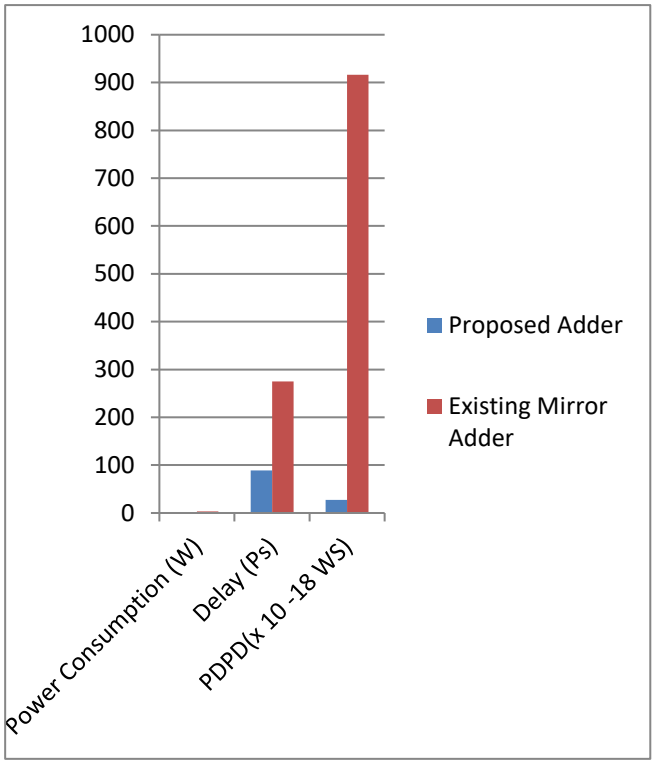

Figure 9. Comparison graph of Existing and proposed method

Overall, the comparison highlights the superior performance of the proposed adder in terms of power efficiency, speed, and energy-delay product. These improvements can lead to more energy-efficient and high-performance digital systems, making the proposed adder a promising choice for various applications requiring low-power arithmetic units.

VII. CONCLUSION AND FUTURE SCOPE

A conceptual framework for double n-bit approximation addition (SEDA) or single n-bit exact addition (SEADA) is presented in this paper. With a limited range of mistakes, SEDA's runtime parameter setting allows for the execution of either exact or approximate addition. All of the work has been completed using Mentor Graphics EDA tools in CMOS 45nm and 32nm technologies. Our results show that we can obtain a 90% reduction in power consumption and a 90% decrease in time when an application comprises more than 40% of approximation computations.

VIII. FUTURE SCOPE

Develop adaptive approximation schemes that dynamically adjust the level of approximation based on application requirements and workload characteristics. This could involve machine learning-based approaches or runtime adaptation mechanisms. Conduct in-depth error analysis to understand the impact of approximation on overall system accuracy. Develop error mitigation techniques to minimize the effects of approximation errors on application-level performance.

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Cite this article as :

Allabaksh Shaik, Dasari Keerthi Reddy, Bisabathini Kireeti, Gayam Yuva Tejasree, C Pavan Kumar, "Design And Analysis of Low Power Single Exact Adder Dual Approximate Adder", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 11 Issue 2, pp. 313-320, March-April 2024.
Journal URL : https://ijsrst.com/IJSRST2411225