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Design of Bio Potential Amplifier for Biomedical Applications

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ABSTRACT

The design of bio-medical signal acquisition system has become possible because of advancements in CMOS technology at rapid rate with tradeoffs in area, speed and power. These advancements have made it easy to continuously monitor and process the various bio-physiological signals whose amplitude and frequency characteristics are in the voltage range of few μV to mV and a frequency range of dc-10 kHz respectively. In bio-medical signal acquisition system, the first and the foremost important block is front-end amplifier (FEA), also sometimes referred as low noise amplifier (LNA) or preamplifier, or in some applications also called as instrumentation amplifier (IA). The important characteristics of such an analog front end are, it should exhibit low-power, low-noise, high gain, high CMRR, high PSRR, high input impedance, high dynamic range and smaller area. Tradeoffs among these characteristics can be optimized in a FEA design by suitable selection of its topology. Design of such analog front end amplifier has a vital role in defining the performance characteristics of the overall biomedical system. In this research work a novel amplifier designs are proposed to improve the noise efficiency especially for biomedical applications.

Keywords : Amplifiers, Operational transconductance amplifier, Bio-potential amplifier, Low noise amplifier, Source degeneration, Transconductance, Unity gain bandwidth.

I. INTRODUCTION

There has been an incredible ascent in enthusiasm for advancements in neuroscience and neuroprosthetic applications over the most recent couple of decades. The principle point of neuroscience is a superior comprehension of the brain, human neurophysiology, and source of disorders like Alzheimer, Parkinsons, deep coma etc. Recent, bio signal recording systems are massive and are not versatile that makes it difficult for ongoing diagnostics and causes discomfort to the patient. The role of implantable medical devices is becoming more important to save and improves the quality of human's lives [1]. The requirement for these systems to make flexible, compact and portability to extend their applications in various fields.

Advancements in CMOS technology paves the way for realizing integrated circuits with dense packing of transistors. This led to the procreation of bio-medical systems in the form of wearable and implantable systems which can help in diagnosis of physiological signals like neuroprosthesis, brain stimulation therapies, fetal ECG monitoring and many more. However, the need for bio-potential signal acquisition systems which are accurate made the researchers to focus on the development of integrated circuits with high packing density, lower cost, and power-efficient. So these advancements in microelectronic circuits have made possible to design portable and implantable electronic devices for biomedical applications by continuous integration of analog and digital building blocks on a single chip. These bio-medical systems need to be designed for low power consumption. More in particular implanted devices should exhibit low power dissipation to avoid heat flux tissue damages. Hence minimizing the total power consumption for such recording systems is a vital task.

Bio-medical signals and their characteristics The continuous growth in microelectronics, communication, and low power circuit design techniques have considerably brought changes in the instrumentation required for monitoring the physiological state of the human body, brain, and heart. The main challenge in the design of such analog front-end instrumentation is to deal with the nature of physiological signals. The bio-potential signals are the responses of physiological activities of organisms ranging from protein sequences to neural and cardiac rhythms to tissue and organ images. Several bio-medical signals includes Electroencephalogram (EEG), Electrocardiogram (ECG), Electromyogram (EMG), Electrocorticogram (ECoG), Local field potentials (LFPs), Action potentials (APs) and many more. Electrocardiogram (ECG) signals are the electrical potentials generated during the alternating contractions of atria and ventricles of the heart with an amplitude range of 0.5 mV to 4 mV at a frequency range of 0.01 Hz-250 Hz. Neural signals represent the electrical activity of the brain.

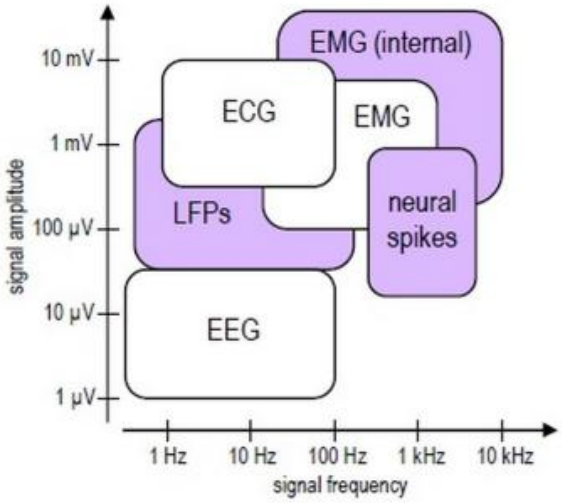

Figure.1. Frequency and amplitude of bio-Potential signals.

This electrical activity can be recorded from within the brain in the form of local field potentials (LFPs) or spikes with an amplitude range of 10 µV to 1 mV at a frequency bandwidth of 1 Hz-10 kHz or over the surface of the brain in the form of Electrocorticogram (ECoG) signals with an amplitude of 5 µV to 10 mV at a frequency band of 1 Hz-250 Hz or over the scalp in the form of Electroencephalogram (EEG) signals with an amplitude of 5 µV to 500 µV at a frequency range of 0 Hz-150 Hz. While Electromyogram (EMG) signals are the electrical activity of the muscles with an amplitude of 0.1 mV to 5 mV with a frequency band of 0 Hz-10 kHz. Hence the amplitude of bio-potential signals irrespective of the source is in the order of a few µV to tens of mV with a frequency range spanning from 0 Hz to a maximum of 10 kHz. Different bio-potential signals with their amplitude and frequency characteristics are illustrated in Figure.1.Figure.2 shows the conventional architecture of a bio-potential signal acquisition system. To record the various bio-potential signals having smaller amplitudes and smaller frequencies with high quality under the presence of various noise sources like

electronics, electrodes, power line interface, etc, the architecture consists of a front end amplifier (FEA) with low input-referred noise, reconfigurable bandwidth and higher gain followed by a programmable gain amplifier to accommodate weak signals and high dynamic range that limits the signal bandwidth and can supply current to external loads such as the input of an oscilloscope or a digital signal processor unit, etc used to visualize or process the waveforms respectively. Recent advances in technologies made neurobiology researchers make a connection between the electrical activity of the human body and the real world through integrated electronics. However, this type of system requires simultaneous recording of electrical signals from various nodes or points of the body for accurate signal processing resulting in the design of a multichannel recording system with optimized power dissipation and high accuracy of recording.

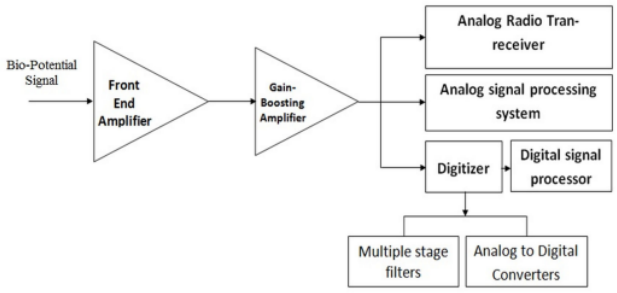

Figure.2. Conventional architecture of a bio-potential signal acquisition system.

Over the past four decades, Scaling in CMOS technology has been the primary concern of electronics industry and is responsible for producing highly denser and faster integrated circuits. The demand of miniaturization of integrated circuits (IC) in terms of number of devices on chip has been resulted in the reduction of channel length of MOS devices. The reduction in channel length has reported the performance improvement in terms of decrease in power and increase in device density on chip. But this trend has increased the power density i.e, total circuits per chip, and the total power consumption of chip. However, the need of improvement in performance has escalate the scaling process in every device parameter that includes effective channel length, power supply voltage, gate dielectric thickness, threshold voltage, transit frequency (fT), device leakage, etc. Table.1. shows the scaling trends in various MOS device parameters. The Table.1. is reprinted from[2]. Since most of these device parameters have reached the fundamental limits, substitutes to the present existing material and structures are need to be replaced in order to utilize the advantages of scaling.

Table.1. Scaling trends in various MOS device parameters

Node	nm	250	180	130	90	65	⇊
LGate	nm	180	130	92	63	43	⇊
t_{ox}	nm	6.2	4.45	3.12	2.2	1.8	⇊
Peak g_m	μS/μm	335	500	720	1060	1400	↑
g_{ds} @ Peak g_m	μS/μm	22	40	65	100	230	↑
g_m/g_{ds}	-	15.2	12.5	11.1	10.6	6.1	⇊
V_{DD}	V	2.5	1.8	1.5	1.2	1	⇊
V_{TH}	V	0.44	0.43	0.34	0.36	0.24	⇊
f_T	GHz	35	53	94	140	210	↑

Regularly, the monitoring or recording of bio potentials which are collected by electrodes from various parts of the human body and these signals are used to diagnose the diseases. The recording system setups are like EEG, ECG, EMG and ECoG. Figure.3. depicts the amplitude (1μV-10mV) . The acquisition of original signals is difficult in the practical recording system due to EEG signals are dominated by background noise as shown in Figure.4. The performance of bio-signals are restricted due to background noise is around 10μV i.e. offset voltages at electrode-tissue interface, noise interference from supply line and noise from MOSFETS [3]. EEG signal defines the function of neuron activity in the brain which is records in the form of electrical signals. The faithful extraction of EEG signal relates to the performance of EEG recording system. By recording the EEG signal from the brain diagnose the diseases like Epilepsy, Seizure detection, Alzheimer, confusion,

memory loss, head injuries, tumors, sleep disorders, deep coma and monitor the brain activity during brain surgery.

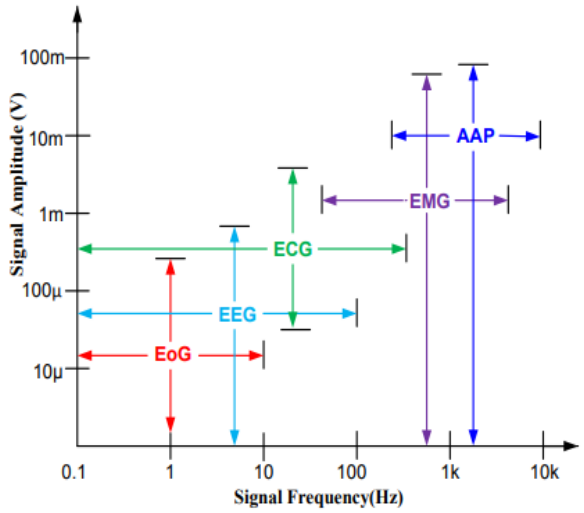

Figure.3. Various Physiological Signals from the Human Body and with Corresponding Amplitude and Frequency Ranges

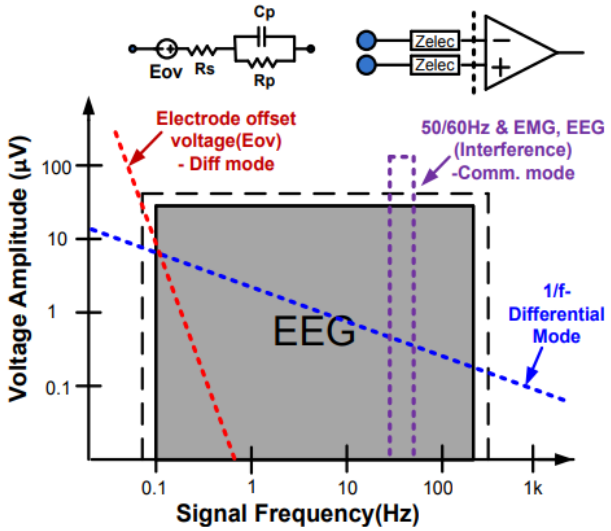

Figure.4. Effect of Various Noise Sources in Bandwidth of Biosignals Range

Other noise sources are the common mode interference noise from the 50Hz/60Hz AC supply and differential mode interference due to mismatch in input devices. Therefore, the designing of EEG recording system with low noise and low power is crucial for these applications. For the proper diagnosis, the faithful signal extraction should require an analog front end with low noise, low power, high Common Mode Rejection Ratio (CMRR) and configurable gain. From the past, the study about BMI (Fig.5.) has been developed rapidly. BMI systems are capable of creating a communication line to the human brain. These interfaces monitor brain-derived neurophysiological signals. When using an EEG-BMI system, the user wants to perform things on purpose so that their brain will produce signals that can be translated into orders. These instructions are sent to the machine so that it may do tasks or move objects that are external, such prosthetic limbs. The new experiences that enable connection between people and digital technologies like home appliances and prosthetic devices have been quite successful because to BMI technology. Researchers and developers have launched health care monitoring in biomedical sectors along with a number of applications using the brain-machine interface idea. The following criteria are the main focus of the researchers: • Cutting-edge, non-invasive electrodes that accurately detect EEG signals • Compact and wearable BMI systems; Low power and Low noise EEG recording devices.

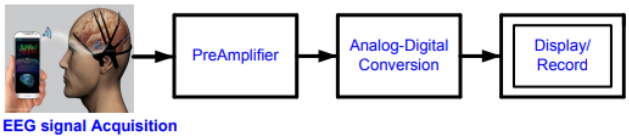

Figure.5. Block Diagram of EEG Signal Recording System

II. PRINCIPLES OF EEG ELECTRODES

Apart from above discussion, the challenging issue is measurement of the brain signals accurately with low noise by the development of advanced electrodes. To provide original EEG signal acquisition at the electrode-tissue interface, development of highperformance electrode is crucial. Many researchers have been interested recently in the development of simple, durable and low noise electrodes. The voltage-current characteristics of bio signal electrode are usually nonlinear. It is the

consequence of charge potential at an electrode surface. Electrodes are to be entitled by linear models need to be operated at low currents and voltages. Considering these ideal conditions, electrodes can be an embodiment of equivalent circuit shown in Fig.6. [4] published an explicit model give a detailed about electrode-skin interface as second order filter. This electrical equivalent circuit is the mixture of six linear components (resistors and capacitors). Wet and dry electrode terminals are relied upon to have the same electrical model however the parameter esteems will be fundamentally differs.

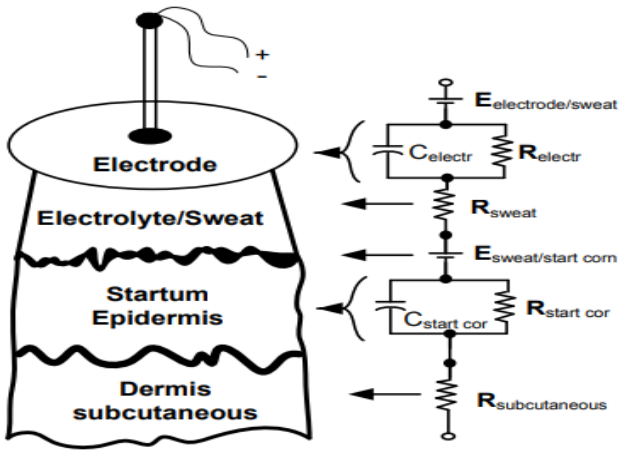

Figure.6. Electrode-Skin Interface and Electrical Equivalent Circuit

Passive electrodes are popularly used in basic wired BMI systems to measure the EEG signals. Passive electrodes are in the ring or disc shape and simple structure. The record of determined EEG signals some extra care must be needed because the potentials from the scalp are only in micro volts range and these are very sensitive to noise. Preparations are needed like hair removal, usage of conductive gels or for the better stick and good conductivity may discomfort or requires more time for an arrangement. These issues for contact impedance at the electrode-tissue interface are not reliable and comes out with a reduction in SNR. Sometimes the quality of the signals to be recorded has an ill effect with the wire vibrations [5].

Previously, to overcome the issues of passive electrodes new research diversion is carried and they come up with advanced electrodes called dry electrodes. For these dry electrodes, the conductive installation process is not required. Dry electrode design looks like a finger and easy to operate into the scalp through the human hair without any extra arrangement. Dry electrode can reduce the installation time between scalp and electrode. Recording signal quality for both passive electrode and the dry electrode is same. To improve the signal quality the researchers are introduced. The active electrodes consist amplifier or unity gain circuits embed to the electrode itself [6,7]. The target of the active electrode is for impedance conversion. This electrode provides high input impedance at inputs of amplifier along with reduced distortion in recorded signals. Therefore, the record of brain signals quality will be remaining same by using active electrodes. Fig.7. depicts the variation of electrode impedance with respect to frequency with which it can be inferred that as the frequency increase the electrode potential degrades gradually.

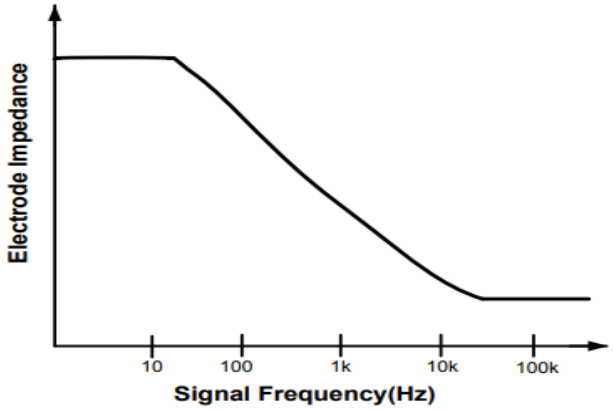

Figure.7. Variation in Electrode Impedance with Frequency

For the design of signal recording system, it is more important to know about electrically equivalent circuit which occurs between electrodes. This equivalent circuit shown in Fig.6. is used to specify the input impedance of bio signal amplifiers [8]. A modeled parallel RC circuit with the series resistor is

equivalent to one electrode. These modeled resistors in the electrode are contributed of thermal noise, so it is desired to have electrode impedance as small as possible. Bio signal amplifiers should have higher input impedance than electrode impedance, otherwise lose in the bio signal amplitudes, produces signal distortion and distorted bio potentials results misguide the clinicians in the diagnosis process.

III. EEG SIGNALS

General classification of bio signals are made as endogenous (EEG, ECG, EMG) and exogenous (X-rays, Monochromatic light, Optical Coherence Tomography (OCT)) types. Endogenous signals originate and collected from natural biology within or on living organisms, membrane cells, nerve cells and muscle cells through electrodes. Exogenous signals are externally applied to scan the body for observe the internal structure. Endogenous bio potentials have the bandwidth of 0.1Hz-10kHz. These signals are collected bio signals along with noise, which exists due to various noise sources in the system and displays the faithful signals from the brain by eliminating the noise. The typical EEG signals are recorded from the scalp in the range of hundreds of micro volts. These signals are used to diagnose epilepsy, sleep disorders, coma, brain death and brain tumor etc. Conventionally, EEGs are classified into 4 frequency bands [9]. • Delta Waves(δ): arises in adults deep sleep with large amplitudes and low frequency (lessthan 4kHz). Theta Waves (θ): mostly occur in young children and adults, teenage people with drowsiness. The frequency band of 4-7 Hz. Alpha waves (α): Origin for these waves at the rear side of the head, two sides and larger amplitude in more influence side. The bandwidth of alpha waves is 8-15 Hz. Beta Waves (β): These waves are appearing on both sides of the scalp with uniform distribution and with low amplitudes (13-50 Hz). Gamma Waves (γ): Gamma waves having the frequency greater than 32 Hz. The signals originated from somatosensory cortex and shown in short term memory. The above all signals are close to DC potential range. it is hard to differentiate the biosignals from the noise at DC level. For the better diagnosis need to have larger number of signals collection from the unit site meanwhile it also consumes more power and area. The recording system should have properties like low noise and low power to collect the original signals. Advanced devices such as nano scale devices are having less noise contribution, low voltage operation suites to meet the requirement of recording systems. IC technologies prove high noise immunity and ultra power dissipation suitable for the bio-chip designs.

IV. NANO INTEGRATION TECHNOLOGY

Moores law defines the advancements in continuous CMOS scaling or minimum feature size of transistors growing in exponential manner. It is most important that in spite of many challenges and difficulties, the theme of decreasing dimensions of the transistor and the resultant magnification of the VLSI IC industry have decided for standing for more than ten years. As the minimum feature of transistor size is going below 10nm, the sevier problem of switching activity will arise. Technology scaling in CMOS transistors, the many changes has been undergone to realize the architectures from past years. The basic operation of MOSFET will remain the same even though the numerous changes are happen. The phenomena of current carrying in a MOS device with some limitations will restrict the scale down of supply voltage at certain limit. As keeping the supply voltage constant with reducing the size of the transistors is the present trend. This results no improvement in power efficiency, which may possible with decreasing the supply voltage. Recent improvements in architectures, principle of operation and new material structure combinations will overcome the challenges of the conventional MOSFETs. In this regard, Tunnel Field Effect Transistor (TFET) is the nano structured device operating on the basis of quantum mechanical tunneling. TFET have been proven superior switching characteristics than conventional transistor. The

TFET device will become the solution for power efficient circuits with low operating supply voltages. Early in 1990s, limitations on integration circuits and reliability problems are forcibly driven towards low power supply voltages.

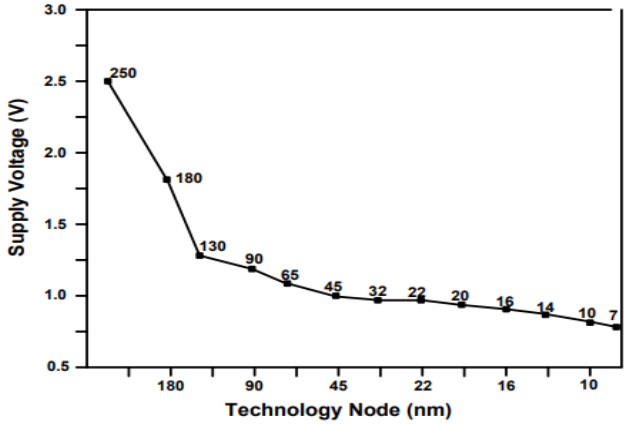

Figure.8. The ITRS Roadmap shows the Technological Requirement of Supply Voltages Related to Technology Nodes

Technically, there are issues about continuous CMOS scaling: Reducing VDD and Vth of the transistors without changing the electrical characteristics of the device. Control of leakage current and short channel effects in the devices. Minimizing the interconnect delays and compactness. Should care about thermal problems by increased transistor density and also reliability of the chip. Withstanding capability of large variations in the process corners at smaller dimension devices. Making the device with smaller technology node for maintain sufficient outcome. The International Technology Roadmap for Semiconductors (ITRS) helps in guiding the technological requirement of supply voltages for a corresponding technology node in nano level circuit designs is shown in Fig.8.

V. EXISTING MODULE

Figure.5. shows the block diagram of a measurement system. There is a demand for medicines and clinicians of multi-channel integrated implantable recording system. These systems help to record bio signals from multiple sites of the brain and human body for genuine diagnosis [10]. Non-invasive electrodes are placed on the scalp or the top of the cortical surface which will pick the EEG signals and fed to signal conditioning stage. The signal which is collected at electrode-tissue interface is the mixture of offset voltages along with EEG signal. The offset voltage is appeared due to variations in electrode interface, impedance mismatch, large electrode impedance, noisy components like MOS, resistance at the amplifier input. The signal conditioning block is responsible for the separation of EEG signal from the mixture. The main function of signal conditioning stage is that elimination of noise and amplifies the biosignals up to acceptable level by considering the high gain. The filtered and amplified signal is given to the A/D converter to process in digital form for further stages. This can be extended up to the application like remote, mobile and IoT health monitoring systems.

The performance of recording system for faithful signal display or recording depends on the signal conditioning block i.e.amplification and filtering of noise with low power consumption. The constraint on design parameters of signal conditioning circuitry is low power, low noise and with sufficient gain. Large no. of amplifiers (order of 100 -1000) is integrated into the on-chip multi-recording system, which reports the constraint about power and noise. First, the amplifier is the important block in signal conditioning stage which replicates the performance of recording system as a function of power consumption and noise. The power consumption of each and every amplifier should be reduced to overcome the problem of excessive heat dissipation which in turn may cause tissue damage or death in the surrounding tissues [11,12]. It is not easy to establish the precise limit on power dissipation. Conventionally, the maximum temperature at recording sites due to the power consumption of tissue should keep less than 1 ◦C (IEEE Standards Coordinating Committee 28 1992). Power limitation

determined by size and shape of the implantable system. Recent multielectrode arrays having roughly 100 electrodes with power consumption of 10mW and this calculation shows each channel consumable power less than 100μW in the uninjured state [13,14]. Taking into consideration, the power budget for all on-chip devices such as signal condition circuit, analog to digital converter and digital processing units along with supply regulation units, the power limit of each amplifier should be less. The battery operated implantable neural recording systems with low power consumption could be helpful for reducing the no. of charging cycles and more durability for avoiding the battery replacements. If the recording systems are allowable for ultra low power, it may be possible for replace the battery fully or partially by wireless power system [17] or by other alternatives like energy harvesting, self power generation techniques [15,16] such as piezo, thermoelectric, electromagnetic, infrared radiant principles. The energy harvesting devices are to generate energy from surrounding places through direct energy transformation. The idea of gathering energy from natural sources, human body movement and body heat for implantable gadgets has picked up another importance. By further research and improvements are going to help to make battery-less implantable recording systems. Since the physiological signals are weak in amplitude, the input referred noise of the amplifiers should be minimized to improve the dynamic range. The recording site of the electrode-tissue interface, impedance mismatch at the interface of the electrode input terminal of amplifier and circuit components like MOS devices, resistors forms the noise voltage is called total input referred noise. Typically, the background noise exists in the range of 5-10 μVrms which is dominates the bio-signals range. For the acquisition of faithful signal, the input referred noise level should be maintained below the signal amplitude levels [18,9]. In this case, always there exists a tradeoff between power consumption and input referred noise of the amplifier. Consider the recorded bio electrical signals with micro volts range (5 μV-500 μV) are not sufficient for analog to digital converter. The amplifiers should have a capacity of rejecting the large DC potentials to avoid the transistors enter into saturation. The ADCs minimum resolution range in milli volts, therefore to strengthen the bio signals range from micro volts to mill volts range an amplifier should have a gain of above 40 dB. Besides, another key prerequisite for the amplifiers configuration is to maintain a strategic distance from consumption of the electrode that may bring about cytotoxicity, which causes a leakage of current at the input of the amplifier. Other two important design parameters of amplifiers are CMRR and PSRR. The signals collected at high impedance node, often it will pick up a significant amount of 50/60 Hz AC supply interference which exists in the bio signal frequency range. The minimization of signal path distance between electrode and amplifier helps to reduce a supply, capacitive and inductively coupled interferences. Other on-chip interferences like digital circuitry interference and interference from on-chip regulated power supply. Fully differential topologies are more preferable for canceling the common mode interferences by providing the high CMRR, PSRR over the single end topologies. However, an additional Common Mode Feedback circuitry (CMFB) is required for fully differential configuration which increase power, area consumption and also leads to circuit complexity.

Typically, the input impedance of amplifier should be in the order of Mega ohms. The impedance of sensing electrode is interfaced with the input terminal of amplifier forms a potential divider circuit or parasitic frequency corners, which may restrict or suppress the interest of signals. Furthermore, the impedance imbalance at an interface of electrode and amplifier input may cause degradation of CMRR and PSRR.

Having an amplifier with high input impedance is the solution for above-mentioned issues. The other constraint along with power and noise about amplifier design is area consumption. Larger size designs are not

suitable for implantable recording systems. Designers and researchers are working actively towards minimizing the area, optimization techniques and nano scale devices i.e. multi-gate technology. High-density integration saves the fabrication cost and can also avoid tissue damage while placing in the brain.

VI. MULTI CHANNEL NEURAL RECORDING SYSTEM

With the advent of tiny in chip design for multi electrode array recording or activating the activity of brain neurons, brain-machine interfaces (BMI) are rapidly advancing in popularity. As demonstrated in Fig. 5, the neuronal activity are captured as biosignals with a range of amplitude and frequency [20]. These bio-signals are captured using a neural signal recording device, which is also used to monitor brain activity during brain surgery and diagnose conditions including epilepsy, seizure detection, Alzheimer's disease, disorientation, memory loss, head traumas, tumours, and profound coma. In order to cover a high number of stimulation and recording locations, the number of implants is increased [21]. In order to accomplish both high efficiency power transmission and high quality brain signal detection, the implant might be constructed to incorporate many Integrated Circuits (ICs). The maximum temperature should not exceed 1C, as per safety requirements [22]. The new difficulty is that power dissipation cannot be prevented since an extremely low power design would be required to operate an implantable microprocessor and reduce body heat. Future biological recording systems will be more useful and complicated. IoT (Internet of Things) recording systems with external devices and cutting-edge features like these excite the human body via hundreds of channels. The maximum temperature increase is estimated to be 0.1763 C for each chip's 1mW power dissipation. Alternately, a bigger implant chip area may be purchased to reduce temperature [23]. To offer enough gain, phase margin, and stability with a minimal amount of current, the telescopic cascode amplifier is a single stage amplifier that is preferred over multi stage amplifiers. To decrease noise and power consumption, [24] suggested an inversion coefficient approach to optimise the size of each transistor for various operating zones.

Recent methods for high density recording systems (Fig. 9.) of epileptic activity include embedding hybrid systems arrays of micro electrodes alongside micro wire exhibits with groups of wires connected to the main electrodes [25] or spreading over the cortical layers using linear arrays of multiple electrodes inserted into the brain tissue. [27] claimed that at the tradeoff of increased power consumption, an extremely low noise amplifier utilising an auto-zeroing approach obtained 90 nVrms. A low power, low noise telescopic OTA for EEG applications was disclosed in [28]. These methods cannot be used for long-term monitoring before surgery. Similar work was published as the Utah Integrated Circuit, which has 320 on-chip channels, 64 of which are for neurological stimulation and 256 of which are for neural recording. A practical distributed recording system uses thin, very flexible chip wafers to create a cortex's active region, which is then covered with many electrodes and integrated circuits (IC). The cortex of the human brain's potential epileptic regions may be covered by this recording technique. Next-generation brain recording systems are shown in Fig. 9 together with multi-neural amplifiers (numbering in the hundreds, with one neural amplifier (shown in Fig. 5) per electrode) and many electrodes to aid in patient care. To lessen the impact of heat on the brain, prolong battery life, and shorten recharging periods, such multi-channel recording devices need very low power and quiet operation. The input referred noise of the amplifier should be smaller than the background noise (5–10 Vrms) for improved signal identification. Low noise and low power amplifier designs do, however, come at a cost.

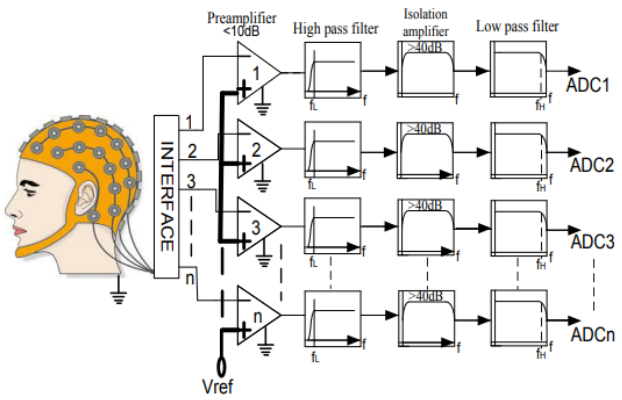

Figure.9. Shared Structure Multi Channel Neural Recording System

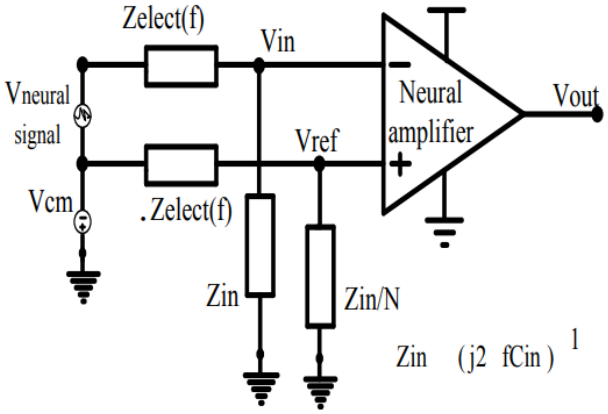

Figure.10. In a multichannel recording system, a single channel neural amplifier's electrical equivalent

Fig. 9 demonstrates that a significant amount of signals from several electrodes positioned all over the scalp must be captured. Through the appropriate channel, each electrode signal may be interfaced to the ADC [29]. One neural "amplifier" comprises of channels of a low pass filter, a gain stage (isolation amplifier), a differential stage, and a high pass filter. There are 'n' channels in a multi channel design, each containing duplicated circuitry. These complicated systems need a lot of power, a lot of consumable space, and a lot of noise. A partial sharing mechanism in the OTA structure was suggested as a solution to this issue [30], which reduces space and power consumption. For this construction, an improvement is necessary to reduce noise brought on by the many channels and more intricate circuitry. We suggest a self-cascode composite current mirror with source degeneration as an active load in OTA to combat this noise issue on multichannel recording systems. The entire recording system's power hungry block, OTA, exposes increased power usage. The degree of comprehension of illnesses like intractable epilepsy is raised by the use of parallel and massively full-duplex integrated interfaces. Real-time research may be done on implantable on-chip systems that can monitor and stimulate neurons [31]. Similar studies on the multi-channel recording system have been described.

Impedance mismatch between the reference and 'n' number of signal inputs is the main difficulty in integrating the many channels on a single neural recording device. In the multi-channel array shown in Figure 10's shared structure Vref (positive terminal), "n" inputs linked to each neural amplifier's negative terminal have the same structure. The effective capacitance at the Vref input terminal is n times greater than the rest of the inputs. The substantial common mode rejection is the cause of this huge impedance mismatch. Improved CMRR was reported, and impedance mismatch is predicted [32]. The typical intrinsic CMRR, which is dependent on the on-chip device mismatch, should be >70dB. The typical approach, in which MOS transistors operate in the saturation region, has limitations for the design of low power and low noise circuits based on contemporary VLSI circuit methods. This study adapts a recent proposal for a low power and low voltage analogue front end system architecture where all transistors are operated in the subthreshold region [33]. Recently, a charge pump level converter with an extreme low power energy harvesting architecture based on subthreshold operation with compromised performance was developed [34]. In this work, we offer a method for designing an analogue front end preamplifier with low power consumption and low noise that involves operating transistors in the

subthreshold range. Inversion Coefficient(IC) [35], a technique we offer that analyses MOS transistor behaviour depending on level of inversion, is shown in Fig. 11. The degree of inversion and operating area of MOS transistors may be determined by the inversion coefficient. Once the inversion level is known, a distinctive indicator of MOS transistor behaviour may be created. Gain, bandwidth, and aspect ratio trade-offs are optimal for designs with proper modelling and understanding of the inversion level. The designer of a circuit should be aware of how to choose the drain current, channel width (W), and channel length for each MOS transistor (L).

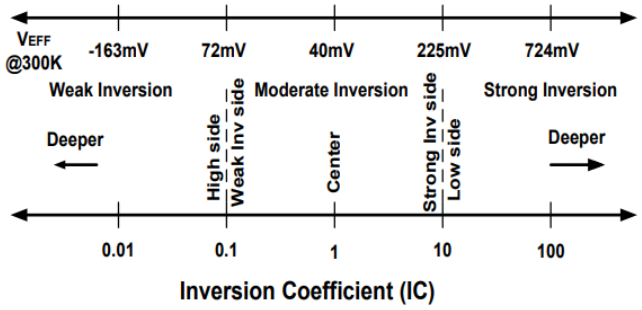

Figure.11. IC value-based operating region and bias voltages

A transistor is considered to be operating in mild inversion if the inversion coefficient (IC) value is less than 0.1, moderate inversion if the IC value is between 0.1 and 10, and severe inversion if the IC value is more than 10. With significant channel inversion, the drain drift current predominates. The ratio of the drain current to the square of the effective gate-source voltage is one in strong inversion (VEF F). The input transistors are tuned to wider widths and shorter lengths in order to produce transistors in sub-threshold region to get greater gm. Channel creation is poor and current and diffusion take precedence in weak inversion. The drain current and transconductance of a MOS transistor are inversely correlated with the gate-source voltage when the transistor is operated in weak inversion.

The proposed low noise opamp design has a source degraded current mirror and a topology similar to that of a traditional telescopic opamp [36]. Telescopic cascode is a single stage architecture that is often used because it has the advantages of two current pathways and fewer devices. By biassing the transistors at sub-threshold and mild inversion regions instead of the strong inversion region, this design helps to optimise factors including area, power, noise, and relaxation in headroom that gives high swing. In the architecture that is being suggested, M0 is a tail transistor that copies the current Ib from the bias circuitry and sources it (n+1) times. The n+1 stage shares this copied current (Ms, M1-Mn).

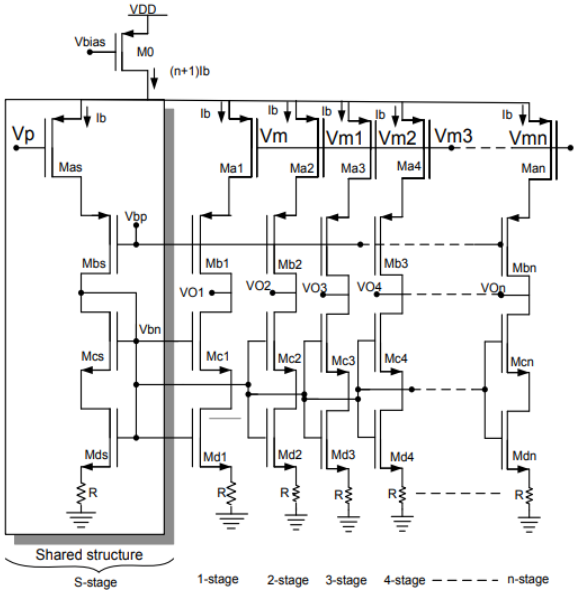

Figure. 12. Multi Channel Shared Structure with Active Load for Source Degeneration in OTA

These transistors Mas, Mbs, Mcs, Mds, and R create a shared structure that may serve as 'n' number of amplifier stages. This common method decreases the complexity of the circuitry while increasing on-chip space efficiency. The suggested method, which is shown in Figure 12, has been demonstrated to be low power and to use less current (n+1)Ib than the (2n)Ibin typical multi electrode construction. At the first stage, node V serves as the common source point for all half circuits of the n stage. The four elements of the n-stage half circuit are Man, Mbn, Mcn, Mdn, and R. Standard biassing circuitry is taken into

consideration for generating the bias voltage for the PMOS cascode devices and tail current source [37]. This study discussed low noise and low power recording channels with high density. In this study, a brand-new active load current mirror arrangement is suggested, as shown in Fig. 12. The self-cascode composite structure with source degeneration replaces the fundamental current mirror.

VII. RESULTS AND DISCUSSION

Figures 13 and 14 demonstrate how a change in R causes Rout sd and gm sd to increase. Gain enhancement and noise reduction are seen by the slope of the gm vs. R graph for the Mdn transistor. Figure 15 illustrates how R affects input referred noise, with greater R resulting in less noise. Gain enhancement and input referred noise reduction are both provided by gm dn reduction. In a self-cascode composite structure, the change in gm of local transistors caused by R is minimal, and transconductance is inversely correlated with output impedance of an active load. The value of R is inversely proportional to the input referred noise as shown in Fig. 15, and this has a restriction on the manufacture of vast values of resistance. By adding a source degenerative resistor (R) in an active load, a significant quantity of input referred noise is decreased. The trade-off between input referred noise and area is taken into account while choosing the ideal value for R. Amplifiers still produce a finite output voltage even when the input voltage is zero, which causes systematic or arbitrary deformities known as "offset." Systematic offset occurs as a consequence of erroneous quiescent operating point selection for active devices or poor amplifier design selection. The random offset is a consequence of different processing methods or mismatched machines. The offset voltage is the bare minimum input voltage required to create the output zero.

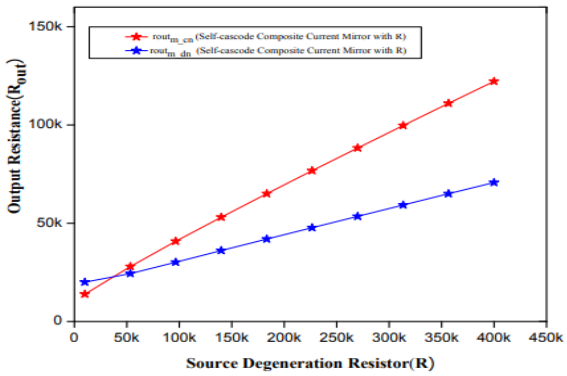

Figure.13. Impact of R Value in rout of Local Transistors (Mcn, Mdn) of Proposed Current Mirror and Cascode Current Mirror

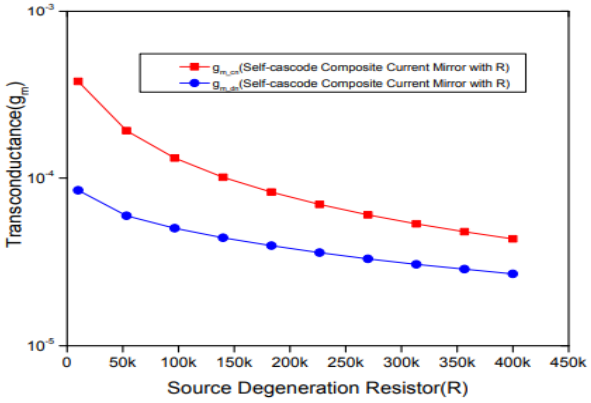

Figure. 14. Effect of R Value on gm of Cascode and Proposed Current Mirror

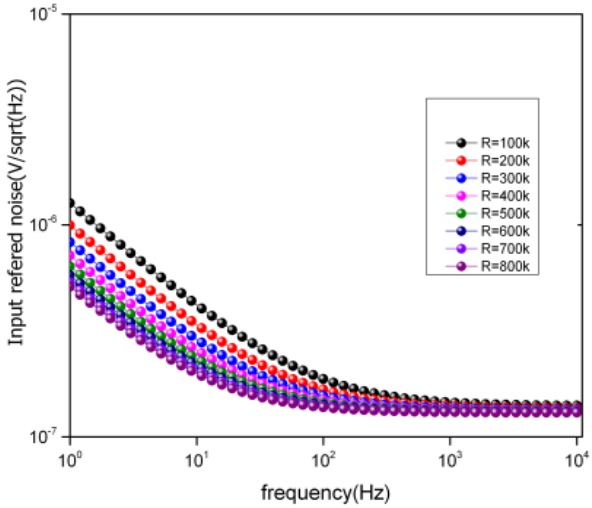

Figure. 15. Effect of R Value on Input Referred Noise Voltage.

By driving the gate terminal of the M7 and M8 output transistors from the folded node, positive feedback inside the amplifier design is achieved to raise the output impedance of RFC OTA [39]. An comparable method is used in this report for IRFC

OTA [16]. Fig. 16 depicts the half-circuit analysis used to get the formula for the MRFC OTA output impedance. A parallel combination of RN and RP, where RN and RP are the corresponding impedances of the M5 and M7 drains, respectively, is used to indicate the impedance at the output.

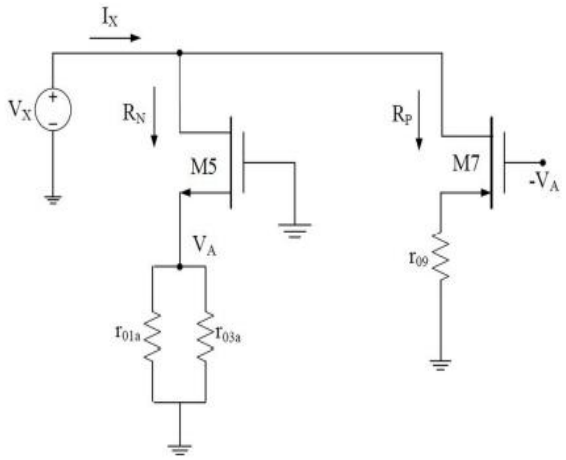

Figure.16. The small-signal counterpart of the positive feedback component for calculating output impedance.

The open-loop AC responses for each of the three designs are shown in Fig. 17. For FC, RFC, and MRFC, the simulated unity-gain bandwidth is discovered to be 24.6 MHz, 34.4 MHz, and 74.71 MHz, respectively. When compared to FC, the UGB of MRFC is raised three times; when compared to RFC, the increase is just around 2.2 times. The phase margins for the FC, RFC, and MRFC are 88.418°, 79.78°, and 74.40°, respectively.

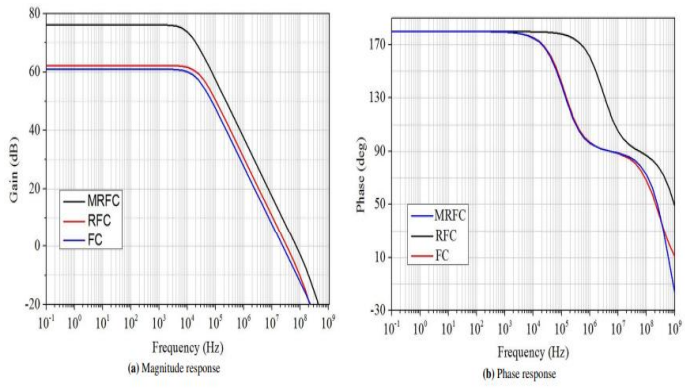

Figure.17. Response of the FC, RFC, and MRFC amplifiers to AC Frequency

VIII. CONCLUSION

In comparison to FC, RFC, and IRFC OTAs, the designed circuit performs better in terms of transconductance, DC gain, slew rate, noise, and UGB, resulting in improved FoMs at a given level of power consumption. It is possible to increase DC gain by using positive feedback at the cascode node. The suggested amplifier may be utilised to create a sample and hold amplifier for biomedical applications since it has lower input-referred noise than FC and RFC OTAs. The enhancement is made possible by including a source degeneration resistor into the self-cascode composite current mirror in this work's effort to propose a multi-channel neural amplifier that is energy efficient, low noise, and NEF enhanced. The suggested system focuses on the >40dB gain and 7.2kHz bandwidth need of bio-signals, which are used to diagnose conditions like epilepsy seizures, Alzheimer's disease, head traumas, profound coma, etc. employing neural recording systems. By regulating the trade-off between power and noise, the optimal value of R is created, and transistor design parameters like gm/ID, W/L, and ID are optimised for low power and high gain. The suggested circuit has a 66 dB gain, a phase margin of 94 o, a power consumption of 2.15 W, and input referred noise of 0.6 V/sqrt when developed and simulated in the UMC 180nm Cadence environment (Hz). It is investigated how the number of channels affects the average current of each channel, and the NEF of the suggested approach is determined for each channel. The suggested OTA is appropriate for portable and intelligent health monitoring applications because to its low power and low noise levels.

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