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Low Power Voltage Level Shifter Employing Power Gating for IOT Applications

Aakula Vinod Kumar[1], T. Sesha Giri[2]
Student[1], Professor[2]
Department of ECE, Shree Institute of Technical Education, Tirupati, Andhra Pradesh, India

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ABSTRACT

Power management is of increasing concern and challenge to SOC and product designer. Power Gating (PG) is now well understood as a technique for reducing static leakage power when circuits are idle In the IOT applications, Level shifters (LS) are used to transport digital signals from the near-threshold voltage level to the actual supply voltage level when interfacing the near-threshold domain and the nominal voltage domain. The LS should be quick enough to meet needs while keeping transition energy and static power as low as possible in order to reduce overhead. For this, we are proposing the double current limiter level shifter with Power Gating Technique which reduces the power consumption by preventing the supply directly connected to the circuit. At the power supply, two transistors were connected in parallel to obtain the design. Level Shifter that meets the requirements of contemporary IOT applications for power, delay, and voltage level shifting. The proposed Level Shifter was implemented in 45nm technology using Tanner EDA tool.

Keywords: Double Current Limiter, Level Shifter, Power Gating, IOT Applications, Power Consumption.

I. INTRODUCTION

In portable gadgets, power dissipation is quite significant. Until recently, energy consumption was not a serious concern because heat was dissipated by huge cooling fins, packaging, and fans are all examples of components. Systems with sub-threshold as well as near-threshold voltages consume minimal energy as well as power. Signal transmissions among sub-VTH as well as near-VTH systems are often difficult whenever standard LSs are used, since every circuit's voltage level is approximately to or less than the MOS device's vth, whereas the supply sources of the outer networks keep rising. When working with multi-voltage domains, level shifters are critical. Sub threshold leakage currents will become an increasingly major component of total power dissipation as future technologies scale and reduce power consumption. One of the really efficient leakage power mitigation solutions currently available is power gating. From the study of this work, we offer a power gating technique for Level shifters that allows for power gating during active mode.

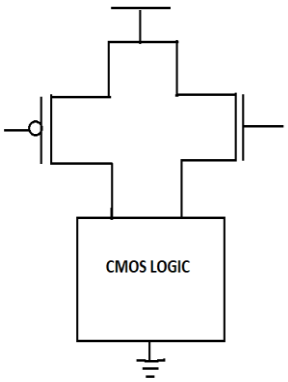

Figure 1: Block diagram of Power Gating

A level shifter cell is often used to adjust the voltage level from high to low or low to high. When numerous voltage domains are active on the chip, level shifters are used. A signal with a voltage spectrum that differentiates from the signal in another voltage domain. Because of the voltage range variation, the destination domain will operate in an unreliable manner. Buffers can be used to get LSs ranging from low to high. In general, MOS transistors' gate voltages have been pushed to the point of breaking down. Even though the breakdown point is often much higher than that of the main supply source, the MOS device's input can be worked at a voltage greater than the supply voltage. Level shifters are used to make sure that When different voltage blocks are combined in a SoC, they function appropriately. As signals migrate from one voltage level to another, level shifters must maintain the right driving strength and exact timing. At any stage of the synthesis or implementation process, level shifters can be incorporated.

Although level shifters are employed to resolve voltage mismatches between different parts of a system, they have a broad array of applications. Level shifters are commonly employed in legacy device interfacing, as well as in SD cards, SIM cards, and UARTs.

II. REARLIER WORK

The digital circuit used to change the voltage from one level to another is a Differential Cascade Voltage Switch Logic.

While installing the LSs across the different voltage domains, some particular placement requirements must be met.

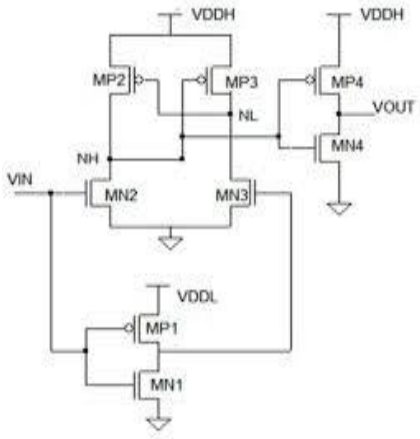

Fig2: Basic DCVS Level Shifter

The problem of adding LS is that it occupies up space while causing severe power loss. LS in its most basic version fosters rivalry between pull-up and pull-down networks.

Double Current limiter Level Shifter

Two current limiters are utilized in this Level Shifter to prevent the circuit from generating or transmitting excessive current as a result of a short circuit in the load.

Whenever supply voltages require the installation of internal current-limiters, In most cases, they are built with current sensors, control circuits, and pass transistors. Current sensors are frequently built with typical low resistance and MOS semiconductors. Furthermore, the voltage across is proportional to the current. This voltage could be used to regulate current flow in pass transistors.

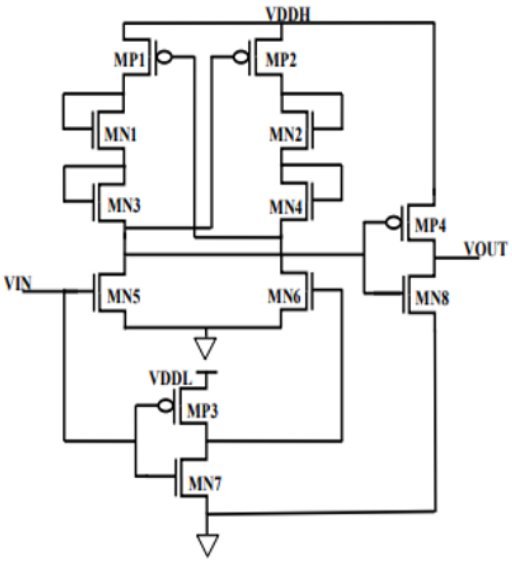

Fig3: Double Current Limiter Level Shifter

The transistor is worked as current limiter when the connection of the transistor is in such a way that the drain terminal is fed to the gate terminal. In the pull up network, current limiters are connected to lessen the current. When Vin is given Logic 0, device MN5 switches off and the device MN6 switches on. As the gate terminal of MN6 transistor is connected through the inverter, by this MN6 transistor gets the voltage of VDDL and gets turned on. From this the MP1 transistor turns on which simultaneously turns on the current limiter transistors of MN1 and MN3. This gives the Logic 1 as input to the MP4 and MN8, by this the transistor MN8 turns on and gives the output voltage of Logic 0.

When Vin is given Logic 1, transistor MN5 turns on and transistor MN6 turns off. As the terminal of MN6 transistor is connected through the inverter, by this MN6 transistor gets the voltage of zero and gets turned off. Due to the on condition of transistor MN5, the MP0 transistor turns on which simultaneously turns on the current limiter transistors of MN2 and MN4 while the transistors MN1 and MN3 are in off state. This gives the Logic 0 as input to the MP4 and MN8, by this the transistor MP4 turns on and gives the output voltage of Logic 1 which refers to VDDH.

The current limiters MN1-MN2 and MN3-MN4 moderate the voltage swing in the primary conversion stage by limiting the current, the better the power consumption and delay can be achieved. In this case, the existing complementary level shifter design aids in the formation of positive feedback while also ensuring the Level Shifter's stipulated functionality.
From the operation of Double Current Limiter Level Shifter, we observe that the output voltage gets the swing between VDDH and ground. Thus we obtain the full swing output voltage.

III. PROPOSED WORK

In the proposed work, power gating technique is applied since leakage power is the major concern in today's world. Power gating is an approach used in integrated circuit design to minimize power consumption by switching off current to non-utilized blocks.

In power gating technique, the additional transistors are to be placed in various ways such as one transistor as a header switch and other as a footer switch or both transistors are placed either as a header switches or as a footer switches. These additional transistors may be connected in series or parallel which depends on the application or need.

Introducing the sleep transistors isolates the chip's power network into two segments: a permanent power network that is connected to the power source and a virtual power network that runs the cells and may be switched off.

A significant fraction of the ICs in a realistic device/application are not used for a longer length of time. This can save a great deal of electricity whereas if energy to that section of the IC is turned down. This preserves not only static (leakage) but also dynamic (non-gated) power.

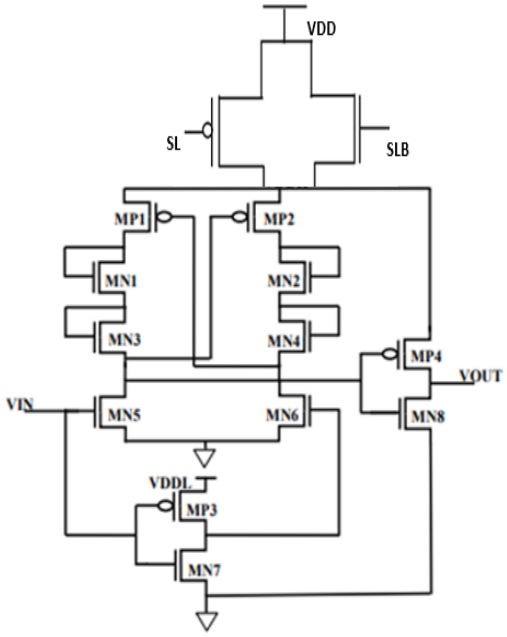

Fig4: Schematic of proposed Level Shifter

In this proposed method two additional transistors are added to level shifter to gate the supply from the circuit when both sl and slb are on, then only supply is passed to the circuit which is termed as active mode. In sleep mode both transistors MP0 and MP0 are turned off. In this scenario supply is not passed to circuit. Hence power is saved when the sleep transistors are off.

In this case, the transistors employed are Pmos (MP0) and Nmos (MN0). Figure 4 depicts the circuit diagram for the proposed level shifter.

These two modes are altered at the proper moment and in the appropriate manner to maximize power performance while trying to minimize performance degradation. Thus, the objective of power gating is to lessen leakage power by briefly shutting off power to circuits that are not essential in that mode.

In active mode of operation, When Vin is given Logic 0, transistor MN5 is turned off, and transistor MN6 is turned on. Because the gate terminal of the MN6 transistor is linked to the inverter, the MN6 transistor receives the voltage VDDL and turns on. The MP1 transistor is activated as a result, and the current limiter transistors MN1 and MN3 are activated as well. This provides Logic 1 as an input to the MP4 and MN8, which causes the transistor MN8 to turn on and provide Logic 0 as an output voltage.

When Vin is given Logic 1, transistor MN5 is activated and transistor MN6 is deactivated. Because the MN6 transistor's terminal is linked through the inverter, it receives a voltage of zero and is switched off. Because transistor MN5 is turned on, the MP0 transistor is activated, which activates the current limiter transistors MN2 and MN4, while transistors MN1 and MN3 are turned off. This provides Logic 0 as input to the MP4 and MN8, causing the transistor MP4 to flip on and provide the Logic 1 output voltage, which is VDDH.

IV. EXPERIMENTAL RESULTS

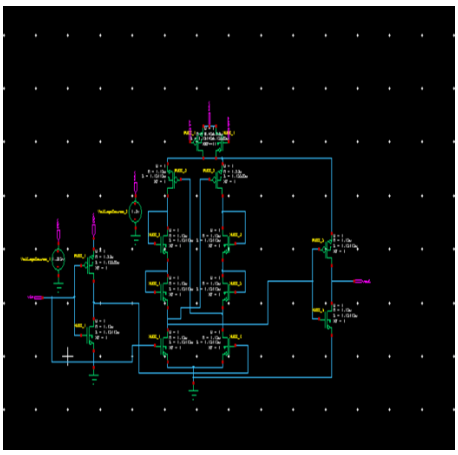

Fig5: Schematic of proposed LS

Figure 5 shows the schematic of proposed level shifter with power gating technique by adding two transistors in parallel as header switches in Tanner tool.

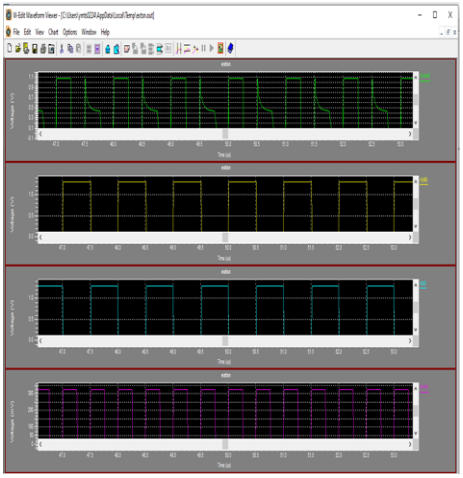

Fig 6: Simulation results for proposed LS

Figure 6 shows the simulation results for proposed level shifter. In this, we observe that when the sl and slb are in active state, we get the output voltages accurately with full swing. And also when the sl and slb are in sleep mode, we get the output voltages which seems to be the discharge of the voltage.

Evaluation table for Area, delay and power:

Parameter	Existing level shifter	Proposed Level shifter
Power (mw	6.1	1.95
Delay(ns)	3.6	3.2
Area	12	14

Table1: comparison between Existing and Proposed methods.

Table1 describes the comparison of performance parameters such as Area, Delay and Power between Level shifter (Existing) and Level shifter with power gating technique (Proposed). From these results, we conclude that the power dissipation is reduced in proposed method by using power gating technique.

The delay is also better in case of proposed level shifter. But, the area (which is nothing but the number of transistors) is less in existing level shifter compared to proposed level shifter because of additional transistors used in power gating technique.

The power results of level shifter with power gating technique. In the result, we are calculating the power from two voltage sources independently. To calculate average power, we have to evaluate the average of average power obtained by the two voltage sources. One is from voltage source_1 and the other is from voltage source_2.

The delay result of level shifter with power gating technique. Because the delay is estimated between the triggering value, which is only input, and the targeted value, which is only output. The computed delay value is 3.242ns in this case.

V. CONCLUSION

This article recommends a double current limiter level shifter with power gating approach. The recommended level shifter with power gating technique was created to shift voltage levels by utilizing 45nm technology. In the power gating approach, additional transistors are placed close to the supply or ground. When compared to the conventional double current limiter level shifter, the proposed circuit requires less energy and even has a lower delay, according to the measurements. The power source doesn't really interact with the power gating network whenever the extra devices seem to be in sleep state. This reduces the amount of energy consumed when sleeping. Ultimately, the postulated level shifter with power gating technique is applied to the IOT applications at interfacing devices.

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