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A Novel Three Stage Comparator Using Lector Approach

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ABSTRACT

This brief presents a three-stage comparator and its modified version to reduce power consumption by using Lector approach. Compared to the traditional three-stage comparator, this novel design of comparator in this work reduces the power consumption. In Lector approach, we are inserting additional transistors in such a way that gate terminals of these extra transistors should have connected with complementary side of output node as per the logic. By this connection, some extra resistance will be added between the paths from supply to ground, which leads to reduction in leakage current. This greatly reduces the leakage power consumption. This proposed design is simulated using Tanner EDA employing 45nm CMOS Technology.

Keywords : Three stage comparator, Lector Approach.

I. INTRODUCTION

In Signal filtering and processing applications, the power consumption and processing time is very critical. Most ADCs use a comparator as part of their building blocks. Hence the comparator must have a high speed and consume less power. Comparator is used to compare two analog signals and will give the output in binary signal based on the comparison [2]-[3].

The comparators measure the smallest voltage differences in ADC's inputs, resolving the performance and the precision of any ADCs. An application that requires digital information recovery from analog signals, such as I/O receivers and radio frequency identification (RFID) memory circuits, widely uses high performance comparators to intensify a little input voltage to a big voltage level [3, 4]. Moreover, digital logic circuits can detect these signals within a short period. Therefore, a faster and precision-making comparator requires high gain and high bandwidth [5, 6].

Several structures of high-speed comparators exist, such as the multistage open loop comparator, the preamplifier latch comparator, and the regenerative latch comparator. Among the different structures, high resolution and high speed can be obtained easily by using the multistage open loop comparator. On the other hand, the latch-type comparatoris the most usable one in the abovementioned applications due to its high-speed and low power consumption features. Latch-type comparators are able to accomplish

decisions more rapidly with no static power indulgence and strong positive feedback [13]. Moreover, latch-type comparators are able to generate high gain in regeneration mode due to their positive feedback features. However, to design circuits for low voltage operations capable of decreasing the dynamic range of the inputs and the corresponding differential process [2, 14], the power dissipations in rail-to-rail operations are often increased. Consequently, the most vital limitations of the dynamic latch comparator are the kickback noises generated by high transmission currents [15]. In addition, employing a transmission gate can also induce spikes at the differential input voltage signals, which affects the performance of the dynamic latch comparator due to random noise, input offset voltages, and component mismatch.

LECTOR (LEakage Control TransistOR technique):
The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation made that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In our method, we introduce two leakage control transistors (LCTs) in each CMOS gate such that one of the LCTs is near its cutoff region of operation.

Two leakage control transistors (PMOS) and (NMOS) are introduced between the nodes and of the pull-up and pull-down logic of the NAND gate. The drain nodes of the transistors and are connected together to form the output node of the NAND gate. The source nodes of the transistors are connected to nodes and of pull-up and pull-down logic, respectively. The switching of transistors and are controlled by the voltage potentials at nodes and respectively.

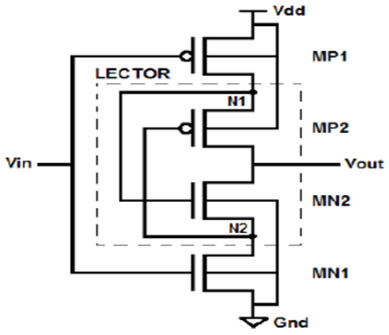


Figure 1: Block diagram of Lector approach

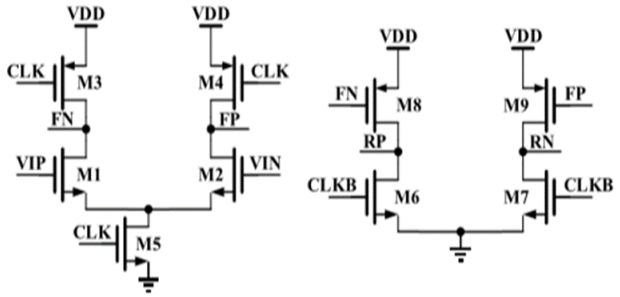
II. EARLIER WORK

In three stage comparator, three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added. This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise.

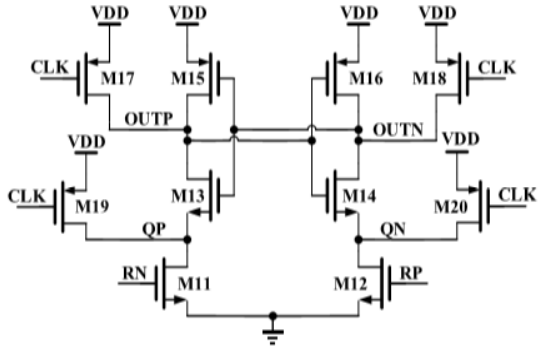
Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two stages, rather than one stage, before arriving at the latch stage. Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about.

As can be seen in Fig. 2, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to VDD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20 ps in post-layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation). This makes sense because the second stage is actually a dynamic inverter which does not incur much delay.

Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Fig. 3), the first-stage output load in the three-stage comparator is only M8–9 in Fig. 3. The output load is reduced by several times, improving the amplification speed.



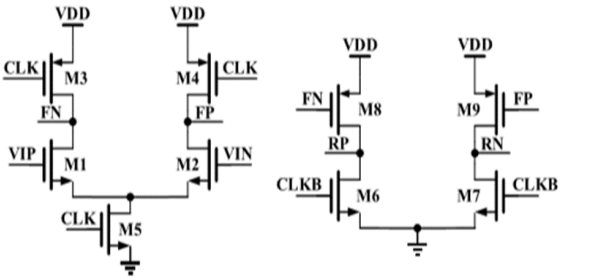
(a)



(b)

Fig. 2. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator, as shown in Fig. 3. Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages of Fig. 3(b) and extra paths M29–32 in the latch stage of Fig. 3(c). The extra first two stages use pMOS input pair.



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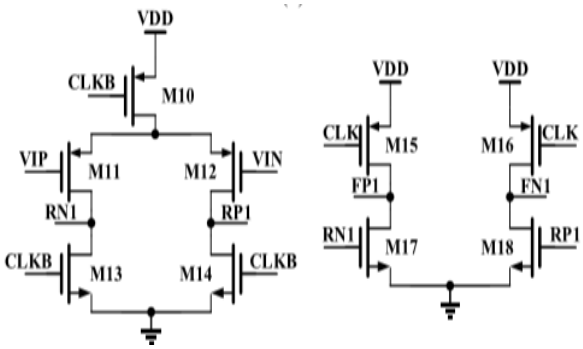
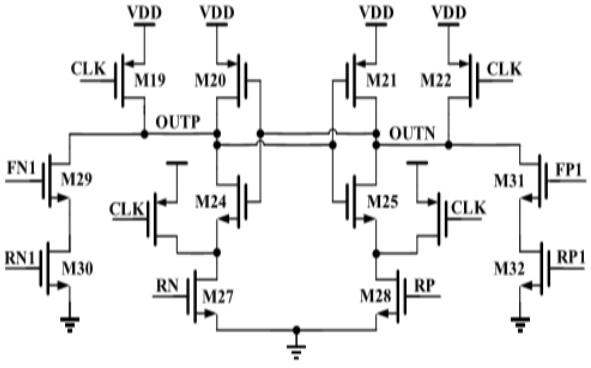


(b)



(c)

Fig. 3.Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further. The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 3(b) are reset to GND, while

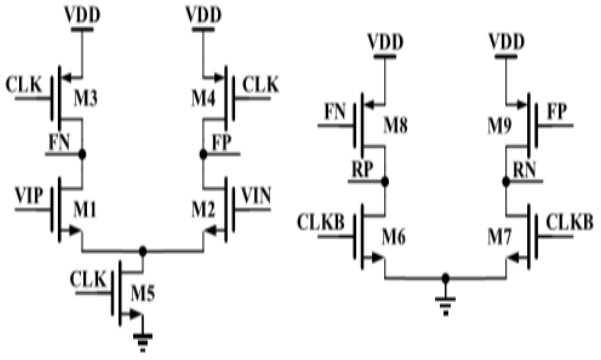
FP1 and FN1 are reset to VDD. This turns off M30 and M32 in Fig. 3(c), ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 3(b) rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 3(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 3(c) are turned off again to prevent the static current.

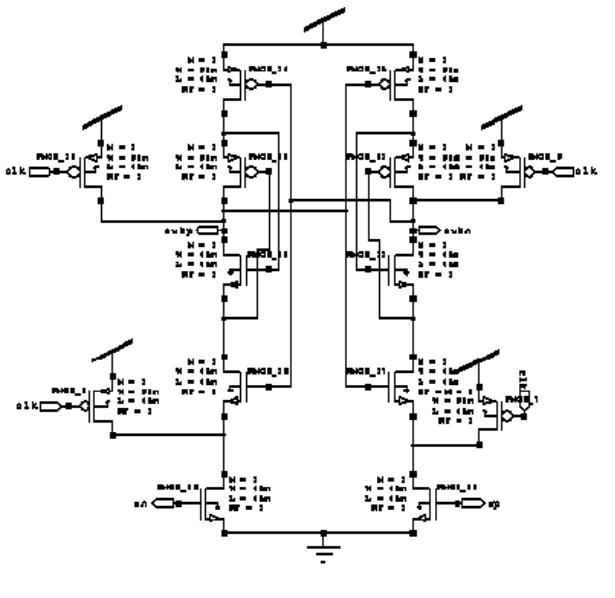
III. PROPOSED WORK

This chapter discusses about the three stage comparator and its modified version on using lector approach. We describe a new leakage power reduction technique called LECTOR (LEakage Control TransistOR) for designing CMOS circuits. Here, we are using Lector technique is applied latch based comparator which used for third stage of working in three stage comparator. In Latch based comparator, two inverters are designed based on lector approach which helps in reducing power consumption.

Three stage comparator:



(a)



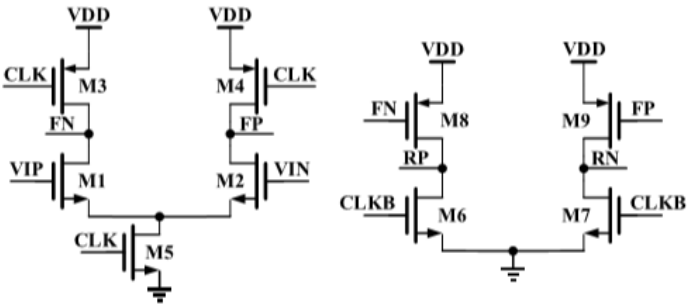
(b)

Fig: 4(a) First two stages (preamplifiers). (b) Third stage (latch stage).

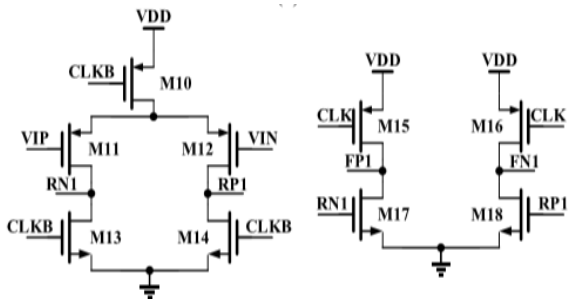
The first two stages in a three stage comparator acts as a Preamplifier and the third stage is the latch stage. The design in the third stage is drawn on the basis of lector technique. The latch formed by the two inverters designed using lector approach. By using lector approach, we are able to reduce power consumption in the circuit.

Modified Three stage Comparator:

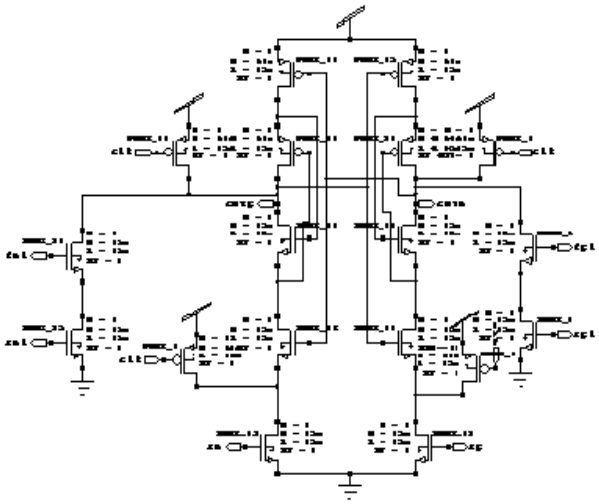
Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages and extra paths in the latch stage.



(a)



(b)



(c)

Fig.5 :(a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, lower kickback noise and less power consumption. It is suitable for high-speed high-resolution SAR ADCs. As an example, the proposed modified version is suitable for the time-interleaved noise-shaping SAR ADC.

IV. EXPERIMENTAL RESULTS

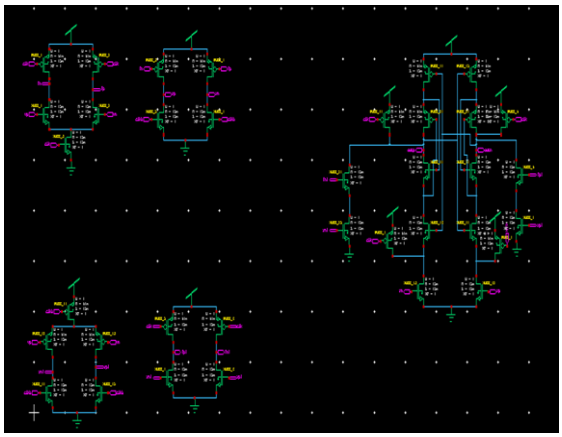


Figure 6 : Schematic of proposed three stage comparator

Figure 6 shows Tanner tool diagram of suggested modified three stage comparator using Lector Approach

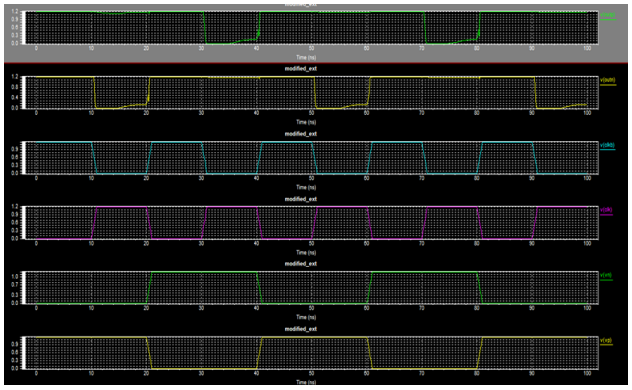


Fig 7: Simulation results for proposed three stage comparator

Figure 7 shows the results of waveforms for recommended three stage comparator using Lector Approach

	AREA	DELAY (ns)	POWER (μW)
EXISTING	19	0.6	3.1
MOD EXISTING	32	0.4	5.4
PROPOSED	23	0.37	2.65
MOD PROPOSED	36	0.42	5.27

Table1: comparison of performance parameters between existing and proposed method.

Table1 describes the comparison of performance parameters such as Area, Delay and Power between three stage comparator existing design and proposed design using Lector Approach.

From these results, we conclude that the power dissipation is reduced in the design using Lector Approach. But, the area is more by inserting additional transistor using lector.

V. CONCLUSION

We used Lector logic in this paper to three stage comparator. The Tanner tool, which uses 45nm technology model files, is used to design and simulate these proposed designs. The performance parameters of these designs are determined and compared. Under proposed work, we are reducing the power consumption by using lector approach at latch based comparator. These comparators are well suited for high-speed high-resolution SAR ADCs.

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