International Journal of Scientific Research in Science and Technology
Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)
doi : https://doi.org/10.32628/IJSRST229666

A High-Performance Full Adder Design with Low Area, Power and Delay

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Article Info
Volume 9, Issue 6
Page Number : 476-483

Publication Issue
November-December-2022

Article History
Accepted : 01 Dec 2022
Published : 15 Dec 2022

ABSTRACT

A new one-bit adder architecture is described that may be used with a variety of logics, including Static CMOS, transmission gates, the Transmission Full Adder (TFA), and the New-14T Gate Diffusion Input Method (GDI). The Modified Gate Diffusion Input Method (MGDI) is used to suggest a novel structure design for a full adder. The full adder circuit is used in the Modified Gate Diffusion Input Method (MGDI), and experimental results demonstrate its superior performance compared to traditional methods. Full adders with multistage arrangements are also considered, as their performance may differ from that of a 1-bit full adder. As a result, two applications of multistage full adder structures, the ripple carry adder (RCA) and 6:2 compressor are used to analyze the findings. The power, area and delay are reduced by around 40% when compared to the existing methods. All the designs are simulated using Tanner EDA. The proposed full adder has a lower transistor count (6 or 7 transistors), lower power dissipation, and less delay than previous designs, according to simulation data.

Keywords : CMOS, Transmission Full Adder (TFA), New-14t, Multistage structures, Gate Diffusion Input Method (GDI), Modified Gate Diffusion Input Method (MGDI).

I. Objectives of the Paper

Recent advancements have increased the importance of portable systems, and digital circuits must consume less power and generate less heat. Recent innovations have increased the importance of portable systems, and digital circuits must consume less power and produce less heat. For increased performance, the majority of applications, such as those found in computers and portable communication devices, require minimal power dissipation [1]. These properties have resulted in significant progress in the development of low-power CMOS devices. Full adders are a common core component in digital circuits that perform arithmetic operations [2]. The proposed full adder has fewer transistors (6 or 7 transistors),

lower power dissipation, and shorter latency than previous designs, according to simulation results. Three inputs are provided, and two outputs are generated. C-OUT stands for carry output, whereas SUM stands for sum output. By using adder logic and cascading the carry bit, eight inputs can be used to create a complete byte-wide adder [3].

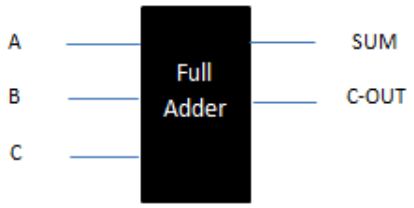

Fig. 1: Full Adder- Block Diagram

The basic full adder structure shown above is built using a truth table. Any combination of NOR gates, NAND gates, two half adders, and an OR gate can be used to build an adder circuit. Below is a full adder logic circuit employing two Half adders and an OR gate.

Sum Logical Expression:

Sum =A'B'C+A'BC + AB'C' + ABC

= C (A'B' + AB) + C' (A'B + AB')

= C XOR (A XOR B)

Carry Logical Expression:

C-Out = A' BC + AB' C + ABC' + ABC

= AB + BC + AC

Full adders are essential components in digital circuits and will continue to play a vital role in VLSI design in the future. Full adders will need to be designed with these factors in mind as the demand for higher performance and lower power consumption grows. Furthermore, new challenges such as 3D integration and nm-scale device fabrication must be addressed. With continued advancements in VLSI technology, the full adder will continue to play an important role in digital circuit design for many years to come. Because of numerous applications such as IoT and portable devices, arithmetic blocks have been paying close attention to the entire adder for some time now [4-5]. We've seen that there are a variety of ways to improve its performance, including the use of new materials and the redesign of its structure. Full adders have numerous applications in VLSI. It can, for example, be used to build arithmetic circuits, perform logic operations, and generate control signals. Full adders are frequently used in conjunction with other components such as multiplexers, flip-flops, and so on. When combined, these components can provide the functionality required for a wide range of VLSI applications.

II. EXISTING SYSTEM

Because complementary metal-oxide semiconductor (CMOS) logic in microprocessors, microcontrollers, and other digital logic circuits can reduce power consumption and noise, the full adder circuit is typically built using CMOS logic. The CMOS logic is implemented by combining the benefits of PMOS and NMOS. As a result, CMOS logic can reduce power consumption and noise.

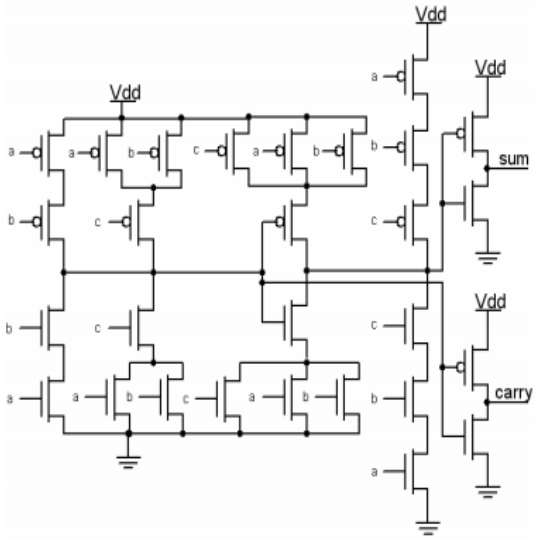

Fig. 2: CMOS full adder

In VLSI systems, addition is a fundamental arithmetic operation that is widely employed. Examples of related operations include the operations addition, subtraction, multiplication, division, and address computing. A 1-bit full adder is essential in VLSI design, and increasing its speed is a major objective. In this technique, circuits for 1-bit full adders are built using a variety of logics, including New-14t, TFA, and TGA.

The circuit schematics for these entire adder circuits are listed below.

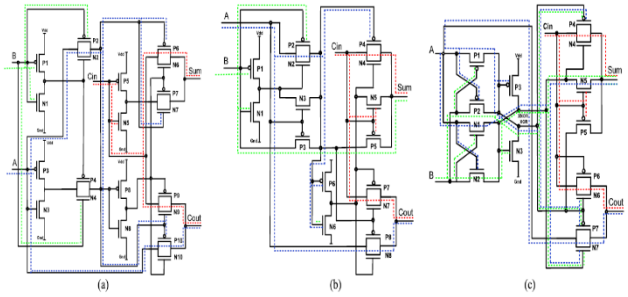

Fig. 3: TGA. (b) TFA. (c) New-14T.

The proposed approach is applied to construct a hybrid full adder. Compared to current full adder circuits, our suggested full adder uses less power and contains fewer transistors. The mux in this adder is constructed using GDI logic, whereas the XOR gate is created using pass transistor logic.

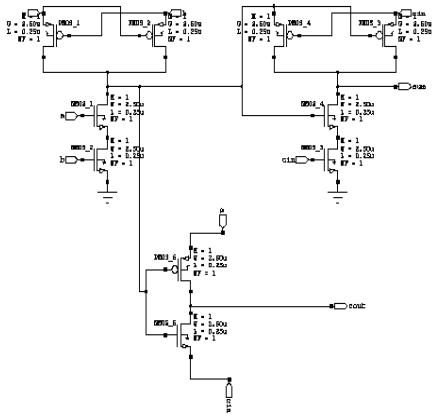

Fig. 4: Circuit diagram of GDI Full Adder

One NMOS and one PMOS make up GDI cells. 3 input terminals are available: G (NMOS and PMOS shorted gate input). N (the PMOS's input source), and N (the input source of NMOS). The output comes from D (a drain terminal that NMOS and PMOS have shorted) [6],[7].

N and P are connected to the Bulk of both NMOS and PMOS respectively.

GDI has (n+2) inputs when compared to CMOS.

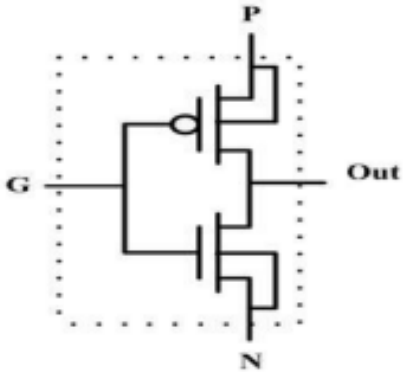

Fig. 5: The Basic cell of GDI

A. Draw Backs of GDI

Output voltage degradation.

Use of power in excess.

For GDI, the usual CMOS manufacturing process poses difficulties.

III. PROPOSED SYSTEM

A. MGDI (Modified Gate Diffusion Input) method:

MGDI is a revolutionary low-power design idea that can help with a several number of problems. This approach is appropriate for quick low-power circuits with a few transistors and enhances logic level swing and static power characteristics. It also enables a straightforward top-down design utilizing a tiny cell library.

When compared to conventional CMOS, GDI lowers gate leakage current and sub-threshold leakage. The GDI cell layout is distinct from traditional PTL methods in a several number of areas, enabling

advancements in design including nature level, transistor count, static power distribution, and logic level swing [5].

Fig. 6: MGDI basic cell

The input terminals of the MGDI cell, such as the GDI cell (input both PMOS and NMOS), P (input to PMOS drain/source), and N (input to NMOS drain/source), are linked to the supply voltage or Vdd aside from the PMOS transistor bulk node.
The PMOS transistor's bulk node is connected to a high constant voltage, whereas the NMOS transistor's bulk node in the MGDI cell is connected to GND.

B. EX-OR gate using MGDI method:

The first input (A) is linked to the PMOS source and gate, and the second input (B) is connected to the MOS source terminal, the PMOS and NMOS common gate input terminals, and both. The three transistors' common drain terminal receives the desired output since the source terminal must be grounded to execute the XOR.

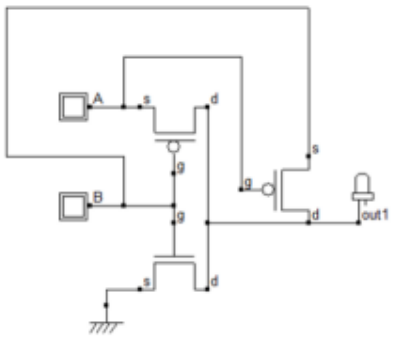

Fig. 7: EX-OR Gate using MGDI Method

C. Advantages of MGDI:

1. MGDI is a good choice for designing high-speed circuits since it uses less power and few transistors.
2. Enhances swing deterioration and static power attributes.
3. Used as a modest cell library to allow for a simple top-down design.
4. MGDI gates reduce the number of transistors, needing less silicon space, compared to conventional static CMOS and domino CMOS-based techniques.
5. MGDI gates have less leakage and switching power than regular logic gates.

D. Proposed Adder

A full adder is a logic circuit that combines the carry from the previous step with the corresponding binary bits of two binary integers to generate a sum with a new carry. It is also known as a three-input adder as a result. The carry-out is formed by Module 3, which is made up of multiple topologies, while the sum is produced by two XOR circuits (Modules I and II). Mathematically,

$$\text{sum} = A \oplus B \oplus C \quad \text{Eq. (1)}$$

$$\text{carry\_out} = AB + C(A \oplus B) \quad \text{Eq. (2)}$$

Let's assume $H = A \oplus B$, we get,

$$\text{sum} = H \oplus C \quad \text{Eq. (3)}$$

$$\text{carry\_out} = A.H' + C.H \quad \text{Eq. (4)}$$

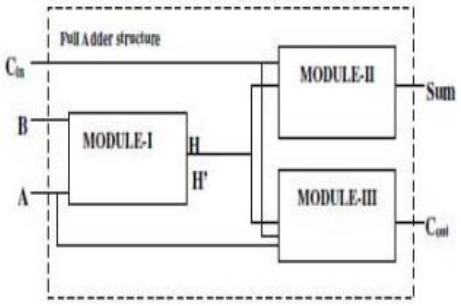

Fig. 8: Block diagram of proposed Full Adder

IV. SIMULATION RESULTS

There are 6 and 7 transistors in the proposed complete adder. The modified gate diffusion input (MGDI) approach is used. The input is directed to the Gate as well as the Source/Drain in this MGDI and GDI technique. So, it is also possible to decrease the Area, Power, and Delay. Tanner EDA Tool is used to simulate each and every design.

A. Proposed Full Adders :

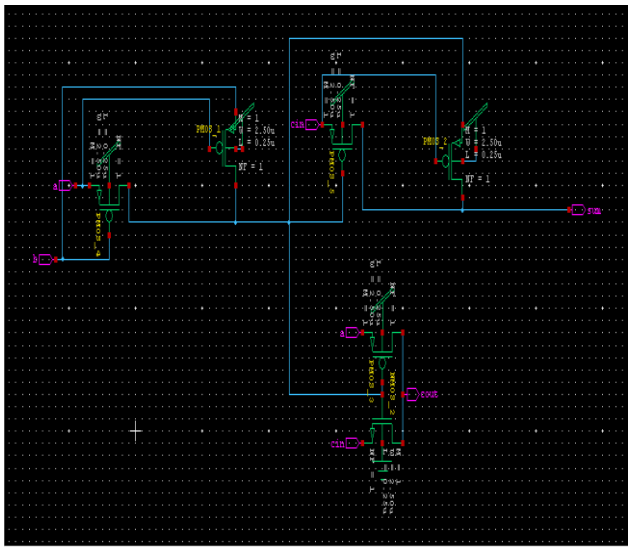

Fig. 9: Schematic diagram of Proposed full adder1 (6-T)

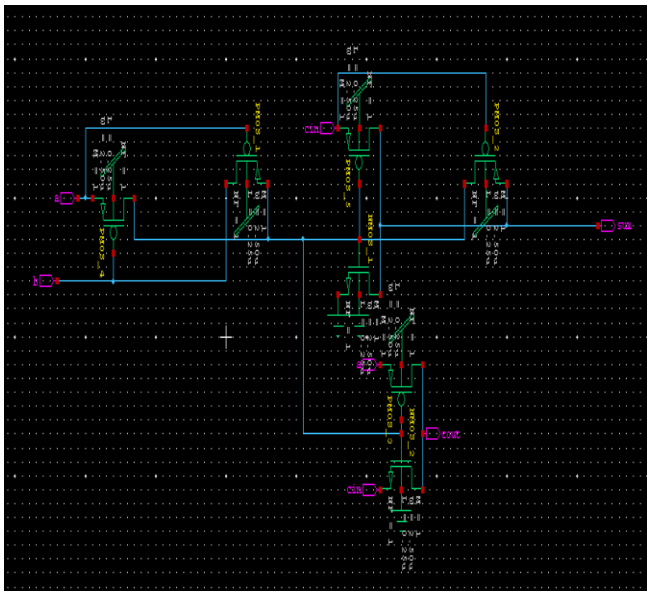

Fig. 10: Schematic diagram of Proposed full adder2 (7-T)

B. RCA with the Proposed Full Adders:

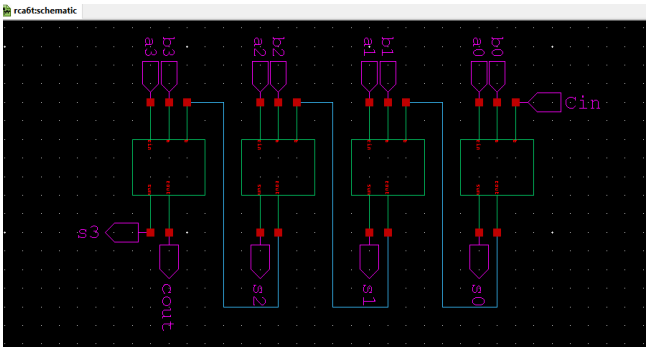

Fig. 11: Schematic diagram of RCA for Proposed Full adder 1,2(6-T,7-T)

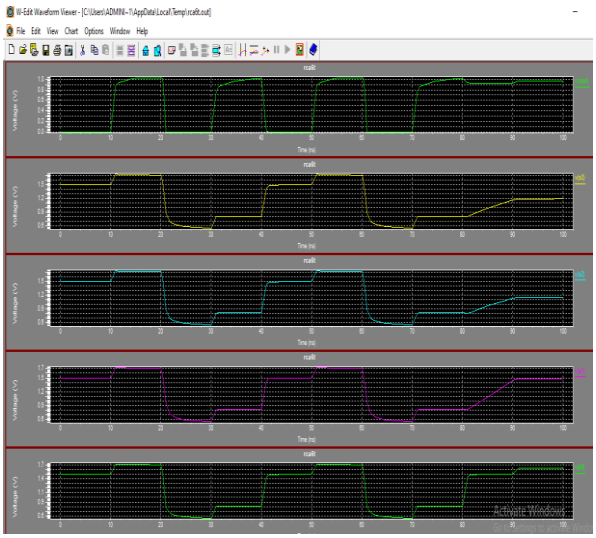

Fig. 12: Waveform of proposed RCA 6-T output (Proposed full adder1)

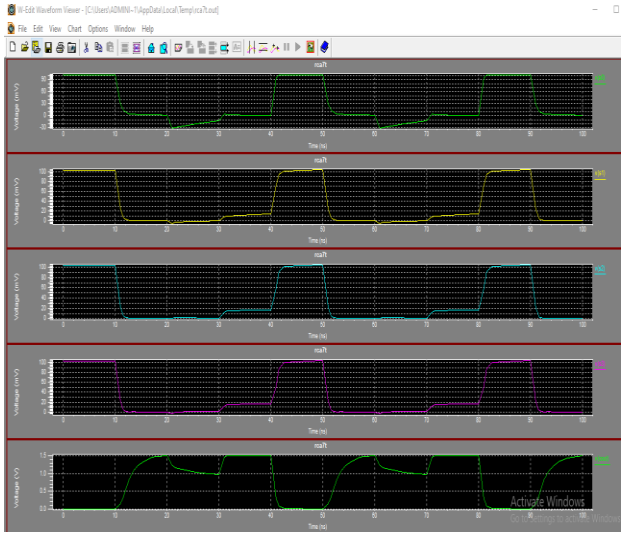

Fig. 13: Waveform of proposed RCA 7-T output (Proposed full adder2)

C. 6:2 Compressor with the Proposed Full Adders:

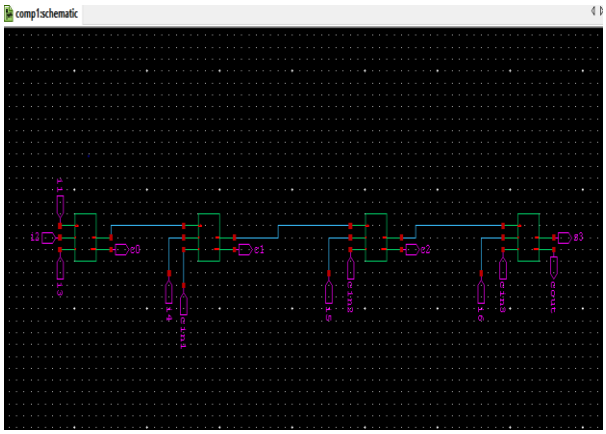

Fig. 14: Schematic diagram of 6:2 Compressor for Proposed Full adder 1, 2(6-T,7-T).

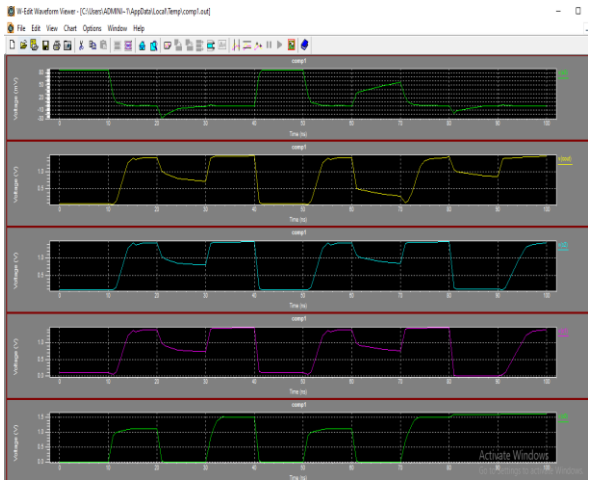

Fig. 15: Waveform of proposed 6:2 Compressor for Proposed Full adder 1 output (6-T)

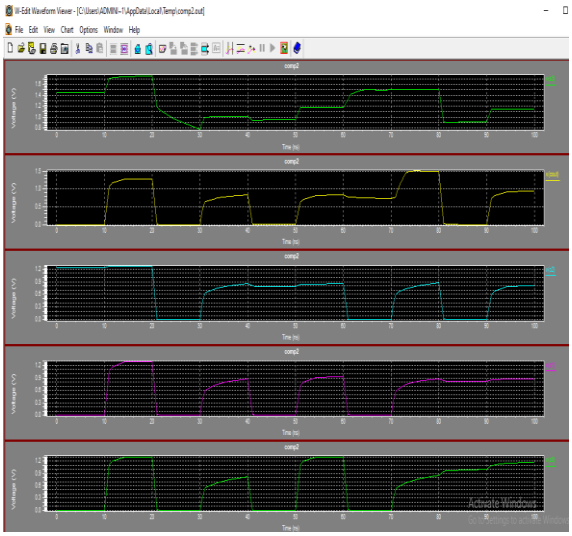

Fig. 16: Waveform of proposed 6:2 Compressor for Proposed Full adder 2 output(7-T)

D. Layout Diagrams Of Proposed 6-T & 7-T Full Adders:

The Modified Gate Diffusion Input Method's Full Adder configuration, which uses 6- and 7-transistors, is shown below. The full adders schematic diagram is subsequently transformed into a Verilog code file during the layout process in Software Dsch 2.6c. Software Microwind 2.6a compiles the modified Verilog code file and creates the layouts.

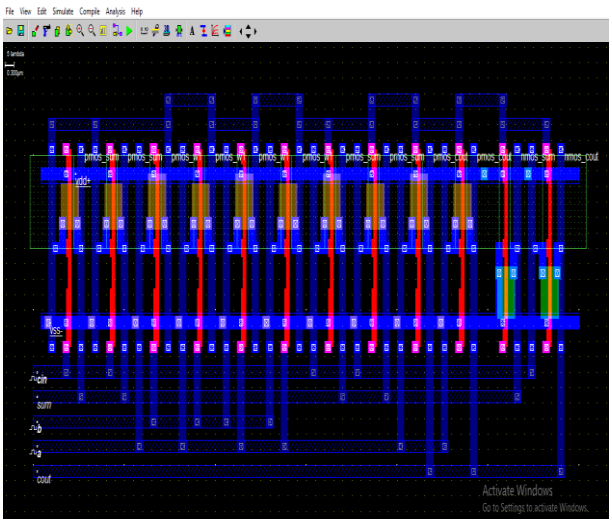

Fig. 17: Layout of Proposed 6-T Full Adder

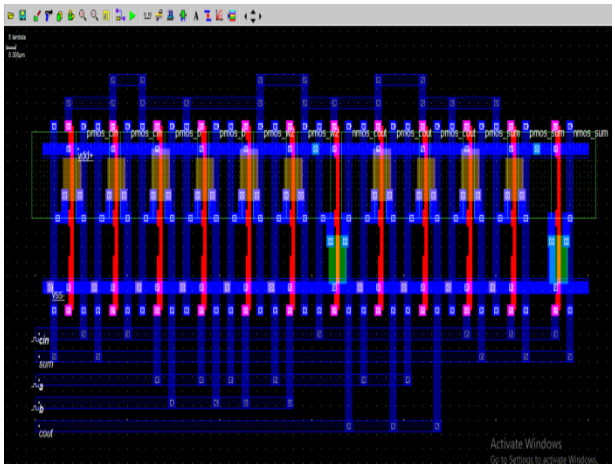

Fig. 18: Layout of Proposed 7-T Full Adder

E. Comparison of Results:

Evaluation of power, delay and area of proposed full adder.

TABLE I

Name	Transistor count	Power(µw)	Delay (ns)
PROPOSED FULL ADDER 1	**6**	**0.46 µw**	**0.75 ns**
PROPOSED FULL ADDER 2	**7**	**0.42 µw**	**0.78 ns**
GDI Method	10	0.2 µw	2.3 ns
New14 T	14	1.0 µw	20 ns
Transmission Gate Adder (TGA)	20	5.7 µw	20 ns
Transistor Full Adder (TFA)	16	1.09 µw	20 ns
Conventional CMOS	28	12 µw	20 ns

Table. 1: Evaluation of power, delay and area of full adder

TABLE II

Name	Transistor-count	Power	Delay
RCA_PROPOSED1 (with 6-T)	24	0.37µw	18.8ps
RCA_PROPOSED2 (with 7-T)	28	1.44µw	20ns
compressor_PROPOSED1 (with 6-T)	24	1.95µw	20.7ps
compressor_PROPOSED2 (with 7-T)	28	1.14µw	1.7ns

Table. 2: Evaluation of power, delay and area for RCA and 6:2 Compressor

V. ACKNOWLEDGMENT

A novel bit adder is compared to several 1-bit adder circuits, including CMOS, New-14t, TGA, Transmission Full Adder (TFA), GDI Method, and MGDI Method. A unique bit adder is developed. These adders are used into multistage circuits like RCA and 6:2 compressor circuits in order to assess how well they work. Tanner EDA Tool is used to simulate all of the designs.

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Cite this article as :

Dondapati. Bindu Sree, K. Rajasekhar, "A High-Performance Full Adder Design with Low Area, Power and Delay", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 9 Issue 6, pp. 476-483, November-December 2022. Available at doi : https://doi.org/10.32628/IJSRST229666
Journal URL : https://ijsrst.com/IJSRST229666