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# Study of Low Power OP-AMP Boosting Techniques

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## ABSTRACT

This paper presents, study of low power operational amplifier using boosting techniques. Operational Amplifiers (Op-amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high-speed amplifiers and filters. General purpose op-amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly.

**Keywords:** Op-amps, CAD, Compensation Techniques, CMOS.

## I. INTRODUCTION

With the growing demand for low power mixed signal integrated circuits for portable or nonportable high-performance systems, analog circuit designers are challenged with making analog circuit blocks with lower power consumption with little or no performance degradation. Op amps are widely used for control and instrumentation applications where high accuracy is required. There has been a trend toward lower voltage and lower current operation to meet the needs of battery-operated products and CMOS op amps are ideally suited for low power application. The classic Widlar op amp architecture, originally developed for bipolar junction transistors (BJT), has required modification for use with CMOS devices. In particular, it has proved difficult to match the open loop gain of bipolar op amps with CMOS technology [3, 4]. This is due to the inherently lower transconductance of CMOS devices as well as the gain reduction due to short channel effects that come into play for submicron CMOS processes. As a result, gain boosting schemes have been reported [5,6] to improve the gain. Multiple stage amplifiers with gain stages of more than three may be used for higher gain analog circuit designs. Nevertheless, multistage amplifiers generally are difficult to compensate. One way to reduce the power consumption of op amp circuits is by scaling down the power supply voltage. Resulting in a reduced input common mode range and output swing. Since the threshold voltage of MOSFET does not scale down at the same rate as the reduction of the minimum transistor length with the advance of technologies as shown in Fig. 1. $V_{GS}$ is the gate-to-source voltage and $V_T$ is the nominal threshold voltage.

Reduced power supply voltage makes many existing gain boosting techniques no longer suitable for standard CMOS processes. Moreover, static power dissipation increases with the decreased threshold voltage. Scaling does not benefit analog circuits as great as it does digital circuits since the minimum size transistors are not

usually selected in analog circuits because of noise and offset voltage constraints. There are two classes of low voltage op amps in general. The first class operates with 2-3 Volt power supplies while the second class works with power supplies below some existing structures with minor changes while op amps used under 1.5 V power supply low voltage range have to adapt some innovative designs to fit the extremely low voltage. 1.5 Volt. Op amps in the range of 2-3 V power supply low voltage range can still use. One important design aspect is the operation region of transistors. Power consumption is the highest when the MOSFET works in strong inversion while power consumption is much lower if the MOSFET works in weak inversion or subthreshold region due to the low quiescent drain current.

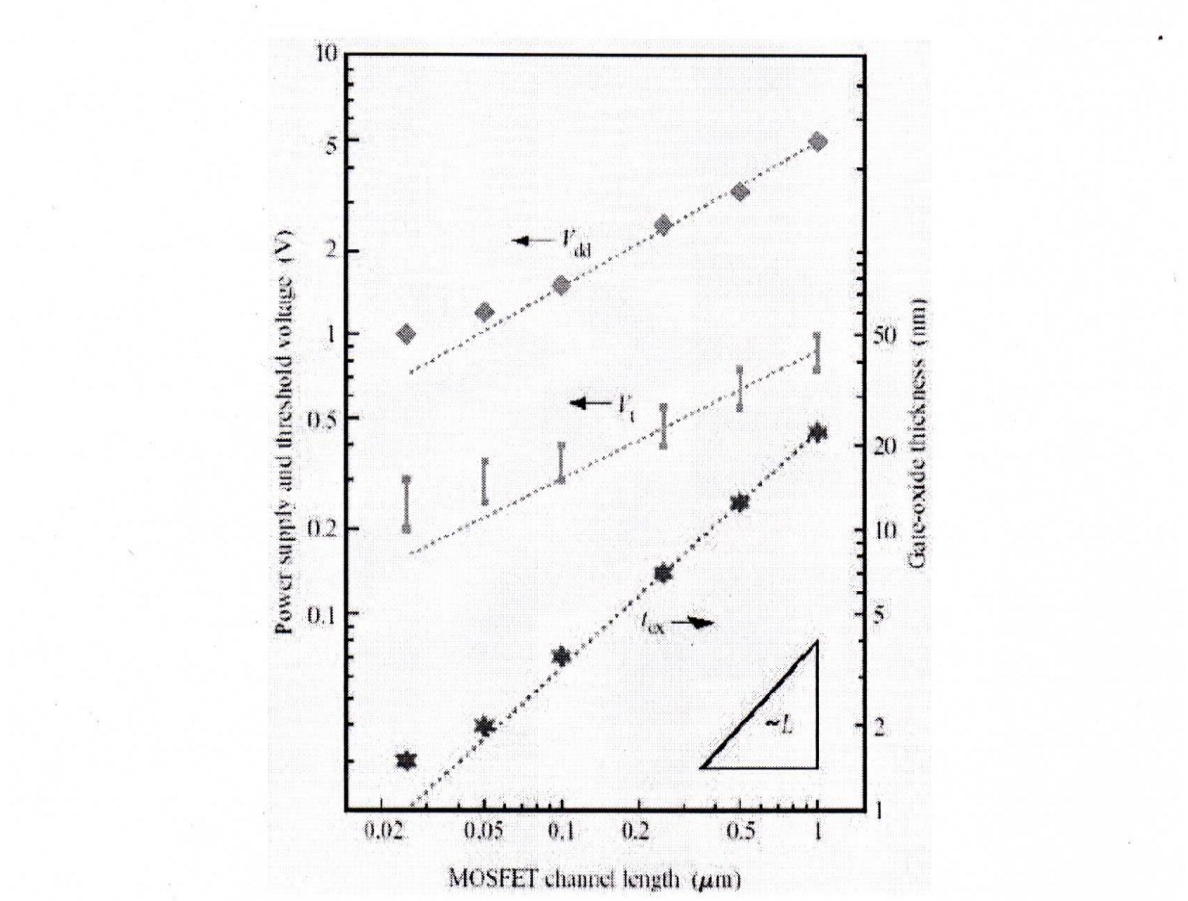


**Figure 1: Power supply and threshold voltage versus the MOSFET channel length [1]**

## II. MOSFET OPERATION

MOSFETs in amplifier stages usually work in their active (saturation) regions. There are basically three operation regions of an MOS transistor within the active region; the strong inversion region, the moderate inversion region, and the weak inversion region.

When an n-type MOSFET is biased with voltages, three different situations may happen at the semiconductor surface. Assuming the source is tied to the p substrate at the zero voltage ground level, a negative voltage VG applied to the gate will bring excess positive carriers (holes) to the interface and give rise to an accumulation of holes. This case is called the accumulation. When a small positive voltage VG is applied to the gate, the majority carriers (holes) near the semiconductor surface are repulsed and leave negative ions behind. This is

called the depletion case since there are no free carriers available to cause the current flow. As VG gets larger, the positive gate voltage starts to attract minority carriers (electrons) in the p substrate to the gate surface area. The gate voltage required for the electron concentration under the gate to be equal to the majority carrier (hole) concentration in the p substrate is usually called the threshold voltage $V_T$ . With $V_G$ gradually increasing, when the electron concentration at the surface is larger than the intrinsic carrier concentration while the hole concentration is less than the intrinsic carrier concentration, the minority carrier (electrons) becomes majority at the surface and the channel beneath the gate is inverted to n region. This is called the inversion case. At first, the surface is in a state of weak inversion region due to the small electron concentration. As gate voltage $V_G$ is increased, the moderate inversion region and strong inversion region are reached. The operation region of a MOS device as a function of $V_{eff} = V_{GS} – V_T$ is shown in Fig. 2. $V_{GS}$ is the gate-to-source voltage and $V_T$ is the nominal threshold voltage.

## III. FREQUENCY COMPENSATION TECHNIQUES

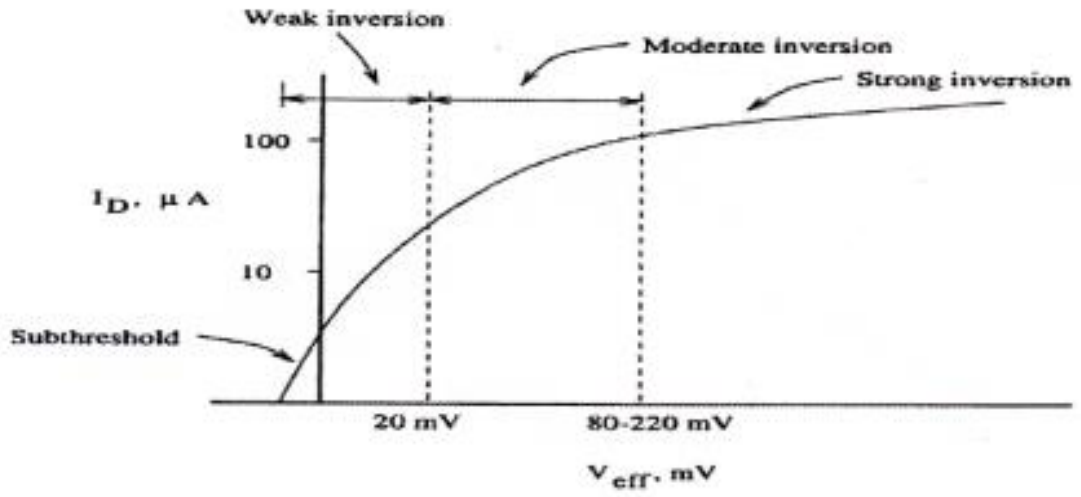


**Figure 2: Operation regions of an MOS transistor [2].**

In general, operational amplifiers are amplifiers with an open loop gain high enough to ensure the closed loop transfer characteristic with negative feedback is approximately independent of the op-amp gain. An adequately high gain is the key requirement of an op-amp to utilize the negative feedback configuration.

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90° assuming the gain bandwidth is ten times higher than the single pole. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op-amps require at least two gain stages. As a result, op-amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause ∟FA to reach –180° before the unity gain frequency. The circuit will then oscillate due to the negative phase margin. It leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called “compensation.” By intuition, two different approaches may be taken to stabilize the circuit. The most straightforward way is to make the gain drop faster in order for the phase shift to be less than –180° at the unity gain frequency. This method achieves stability by reducing the bandwidth of the amplifier. The most popular pole splitting method uses this

procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In my case, the number of the poles of the op-amp needs to be minimized while still providing enough gain.

## IV. LOW SUPPLY VOLTAGE TECHNIQUES

As mentioned, one common way to reduce the power consumption of analog circuits is by reducing the power supply voltage. However, the circuit performance degrades at low voltages. It raises the challenge of modifying circuit structures for low voltage application since low voltage analog circuit design techniques are quite different from high voltage analog circuit design. The alteration or even redesign of the current circuit structure is necessary for low voltage operation. Low voltage design is required for conditions when current levels are very small and supply voltages are low. Applications can be found but not limited to the biomedical area. The main restrictions of low voltage circuit design are the transistor threshold voltage and the device noise level. The down scaling of threshold voltage relies on specific device technology advancement. Higher threshold voltage has better noise margin and is less sensitive to noise while the lower threshold voltage decreases the noise margin and become more noise sensitive.

## V. CONCLUSIONS

MOSFET operation is introduced and three different inversion levels are presented with the suggestion of applying weak inversion operation to low power design. A few popular cascode gain boosting techniques for op amp designs are presented with their merits and demerits. Some possible design techniques for a very low voltage environment are introduced and discussed. The choice of an appropriate technique or a combination of a few techniques can be employed for the corresponding low power high gain op amp design.

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