

Study of Design of High Gain OP-AMP

Vikas Kumar Roy

M. Phil. Students, Department of Physics, B. R. A. Bihar University, Muzaffarpur-842001, Bihar, India

ABSTRACT

In this paper, we report on study of design of high gain operational amplifier using compensation techniques. Operational Amplifiers (Op-amps) are one of the most widely used building blocks for analog and mixed-signal systems.

Keywords: Op-amps, CAD, Compensation Techniques, CMOS.

I. INTRODUCTION

Many compensation schemes for multistage amplifiers have been investigated and reported [3–5, 7]. Techniques similar to those used in general feedback control systems have been adapted to use with electronic amplifiers. These methods include lead-lag networks, pole splitting, nested Miller compensation as well as signal level variable components. However, most compensation methods require more circuit area and more complex design than the dominant pole approach used in the classic op-amp architecture. Special problems of integrated circuit amplifiers which include lack of large sized capacitors, parasitic coupling, and package parasitic and on/off chip load problems make the compensation more difficult than discrete component amplifiers.

The most widely used method of compensating integrated circuit op-amps is undoubtedly pole splitting in which the amplifier stage with the smallest bandwidth is further narrow-banded by a compensating capacitor that creates a well-defined dominant pole that sets both open and closed loop bandwidth of the overall amplifier.

This work is concerned with the compensation techniques for operational amplifiers and will explore new and novel methods of achieving compensation in feedback amplifiers that do not limit the bandwidth of closed loop performance to the same degree that commonly used methods do. Specific tools and methodologies will be developed to allow comparison of the new methods with standard methods of compensation.

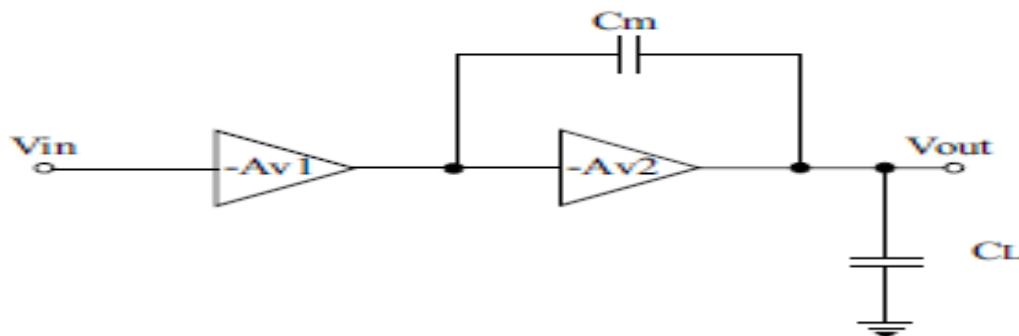
II. MATERIALS AND METHODS

The design guide here is to apply the feed forward intuition on the system model and do the mathematical analysis to check if the idea works theoretically. After the feasibility is verified with theory, the feed forward scheme is then going to be evaluated by a system level simulation. Many different versions of SPICE simulators and MATLAB simulators already have built-in system level models of the circuit blocks. System level

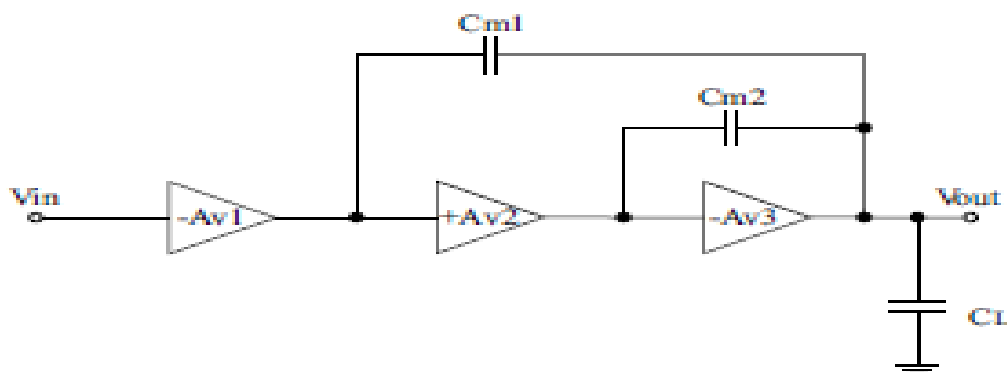
simulation can be done within a short time compared to the device level simulation. For accuracy and other practical issues, a mixed simulation method combining the system level simulation with the device level simulation is a very efficient and viable way to assess the creative design method.

The single stage amplifier typically has good frequency response and could achieve a phase margin of 90° assuming the gain bandwidth is ten times higher than the single pole. However, the dc gain of the single amplifier is generally not high enough and is even less for submicron CMOS transistors. In general, op-amps require at least two gain stages. As a result, op-amp circuits have multiple poles. The poles contribute to the negative phase shift and may cause $\angle A$ to reach -180° before the unity gain frequency. The circuit will then oscillate due to the negative phase margin. It leads to the necessity of altering the amplifier circuit to increase the phase margin and stabilize the closed loop circuit. This process is called “compensation.” By intuition, two different approaches may be taken to stabilize the circuit. The most straightforward way is to make the gain drop faster in order for the phase shift to be less than -180° at the unity gain frequency. This method achieves stability by reducing the bandwidth of the amplifier. The most popular pole splitting method uses this procedure. Another compensation method pushes the phase crossover frequency out by decreasing the total phase shift. In my case, the number of the poles of the op-amp needs to be minimized while still providing enough gain. Pushing the phase crossover frequency out is the basic idea of approaches like introducing zeros to cancel the poles or using feedforward paths to improve the phase margin without narrow-banding the bandwidth as much as the pole splitting method does.

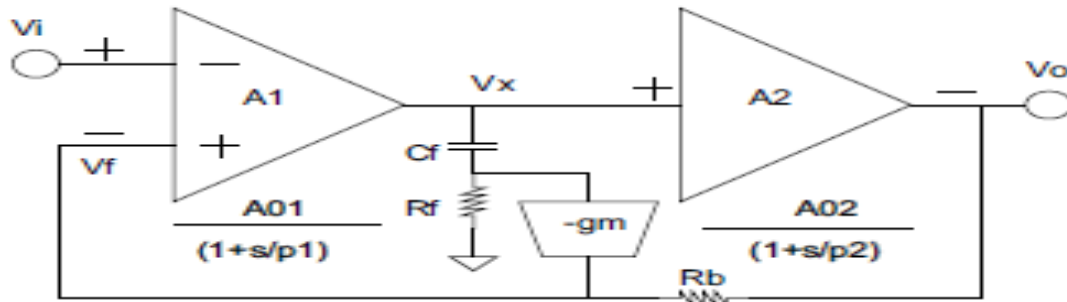
Single Miller Compensation (SMC)



Nested Miller Compensation (NMC)

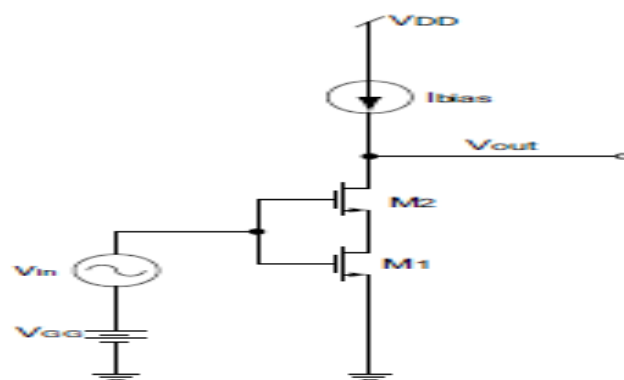


Simplified model of the feedforward compensated operational amplifier



III. DESIGN OF HIGH GAIN OP AMP USING COMPOSITE CASCODE CONNECTIONS

Many gain boosting schemes have been present to improve the gain of an op-amp. These gain enhancing methods often require complicated circuit structures and high supply voltage, and may produce a limited output voltage swing. Multiple stage amplifiers may be used for higher gain analog circuit designs. Many compensation schemes for multistage amplifiers have been investigated. However, most compensation methods require more circuit area and more complex design than the dominant pole approach used in the classic op-amp architecture. Other high-gain CMOS op-amps have been investigated in previous work [8–14], but most did not achieve gains higher than 100 dB. A few achieved a gain ranging from 120 dB to 130 dB. These CMOS op-amp designs use up to five cascaded gain stages to achieve the high gain. The highest reported was the simulated 140 dB [10] unbuffered op amp with three cascaded gain stages. In general, high gain architectures need complex compensation to stabilize the op-amp and generally require more than one compensation capacitor.



Composite Cascode Amplifier

IV. CONCLUSIONS

This paper proposes a creative feedforward compensation method which overcomes the serious drawback of bandwidth narrowing by the widely used pole-splitting method. It can improve the phase margin as well as optimize the bandwidth of the op amp. The feedforward method can be easily applied to the existing popular two gain stage op amp architectures with very little alteration. The mathematical derivation and circuit

simulation demonstrate the advanced properties and improved performance of this feedforward compensation technique.

V. REFERENCES

- [1]. Y. Taur, "Cmos design near the limit of scaling," IBM Journal of Research and Development, vol. 46, no. 2/3, pp. 213–222, March/May 2002.
- [2]. D. J. Comer and D. T. Comer, "Using the weak inversion region to optimize input stage design of CMOS op amps," Circuits and Systems II: Express Briefs, vol. 51, no. 1, pp. 8–14, Jan. 2004.
- [3]. P. Gray and R. Meyer, "Recent advances in monolithic operational amplifier design," IEEE Transactions on Circuits and Systems, vol. CAS-21, no. 3, pp. 317–327, May 1974.
- [4]. D. Johns and K. Martin, Analog Integrated Circuit Design. New York: John Wiley & Sons, Inc., 1996.
- [5]. J. Huijsing, R. Hogervorst, and K.-J. de Langen, "Low-power low-voltage vlsi operational amplifier cells," IEEE Transactions on Circuits and Systems, vol. 42, no. 11, pp. 841–852, Nov. 1995.
- [6]. P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd Ed. New York: Oxford University Press, 2002.
- [7]. W. Black, D. Allstot, and R. Reed, "A high performance low power CMOS channel filter," IEEE J. Solid-State Circuits, vol. SC-15, no. 6, pp. 929–938, Dec. 1980.
- [8]. A. L. Coban and P. E. Allen, "A 1.75 v rail-to-rail CMOS op amp," Proc. Of IEEE International Symposium on Circuits and Systems, vol. 5, pp. 497–500, Jun. 1994.
- [9]. R. G. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 v CMOS class-ab operational amplifier with hybrid nested miller compensation for 120 db gain and 6 mhz ugf," IEEE J. Solid-State Circuits, vol. 29, no. 12, pp. 1497–1504, Dec. 1994.
- [10]. J. Purcell and H. S. Abdel-Aty-Zohdy, "Compact high gain CMOS op amp design using comparators," Proceedings of the 40th IEEE Midwest Symposium on Circuits and Systems, vol. 2, pp. 1050–1052, Aug. 1997.