© 2020 IJSRST | Volume 7 | Issue 7 | Print ISSN: 2395-6011 | Online ISSN: 2395-602X
Themed Section: Science and Technology
DOI : 10.32628/IJSRST

Study of Fully Differential Low-Noise Amplifier

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ABSTRACT

In this present paper we report on study of fully differential low noise amplifier. Amplifiers are the most critical component of the FIRS integrated circuitry, for several reasons. From a noise standpoint, the signals being amplified have magnitudes on the order of tens to hundreds of microvolts.
Keywords: IC, Fully Differential Low Noise Amplifiers, CMFB

I. INTRODUCTION

Amplifiers are the most critical component of the FIRS integrated circuitry, for several reasons. From a noise standpoint, the signals being amplified have magnitudes on the order of tens to hundreds of microvolts [1]. After the initial amplification, the signals will be at least two orders of magnitude higher, so any noise injected by the remaining signal processing circuitry will have much less significance. From a power and size perspective, a 100 channel recording system would require 100 amplifiers (one for each channel), but only one MUX, transmitter, and set of reference circuitry, so the bulk of the area and power consumption on the chip will be due to the amplifiers. This makes the optimization of power consumption and layout size particularly critical for the amplifier circuit.

II. REQUIREMENTS FOR LOW-NOISE BIOSIGNAL AMPLIFIERS

The first requirement for the amplifier is that it must have a very low intrinsic noise level. The amplifiers add noise to the signal through thermal noise and $1/f$ noise sources in the transistors. Since the signals being amplified are on the order of microvolts, the noise added by the amplifier must be minimized to avoid overwhelming the signals to be amplified. In addition to the noise sources intrinsic to the transistors, we must also consider interference noise from the digital circuitry on the chip (i.e., the multiplexer). Switching transients can be coupled into the analog circuitry through parasitic capacitances in the substrate or between interconnects. This type of noise can be minimized through a fully differential architecture. The standard requirement for noise is that the input referred noise level of the amplifier be less than the typical extracellular neural “background” noise of 5-10 μVrms [2-5].
Another important requirement for bio-signal amplifiers is that they must be able to reject large DC offsets. The open-circuit dc potential between a buffered saline electrolyte and a gold electrode can be as high as +/- 50

mV [6], which would saturate the amplifier outputs if DC signals were passed. Several methods have been used to accomplish this which will be discussed in the next section.

The final requirement for the amplifier circuit relates to the cutoff frequency. Typical neural action potentials have energy in the range from 100 Hz to 7 kHz [1], while local field potentials can contain signal energy below 1 Hz [7]. For these reasons, the amplifier should have a low frequency cutoff below 1 Hz, and a high frequency cutoff around 7 kHz. The low frequency cutoff rejects the DC offsets at the electrode interface, and the high frequency cutoff prevents unnecessary noise from being included in the output signal.

III. IMPLEMENTATIONS OF LOW NOISE AMPLIFIERS

Many implementations of single-ended low noise amplifiers (LNAs) for biomedical applications have been reported in literature ([1], [2], [3], [4]-[7]). All of the designs attempt to meet the requirements listed above, with varying degrees of success. A useful way of comparing amplifier designs is with a noise efficiency factor (NEF) introduced in [8]. The NEF of a system is defined as

$$NEF = V_{rms,\,in}\sqrt{\frac{2.I_{tot}}{\pi.U_T.4kT.BW}} \quad (1)$$

where $V_{rms,in}$ is the total equivalent input-referred noise, BW is the bandwidth of the system in Hz, I_{tot} is the total current consumed, and U_T is the thermal voltage. The ideal case is a single bipolar transistor, which has a NEF of 1. All practical designs will have a higher NEF than one. The NEF quantifies the noise-power tradeoff for amplifiers (the lower the NEF, the lower the noise level for a given power consumption). Figure 1 compares the NEF values for a number of published amplifiers. From Figure 1 it can be seen that [5] has the lowest NEF of all of the reported designs, this is the design we have chosen as a starting point for our fully differential design.

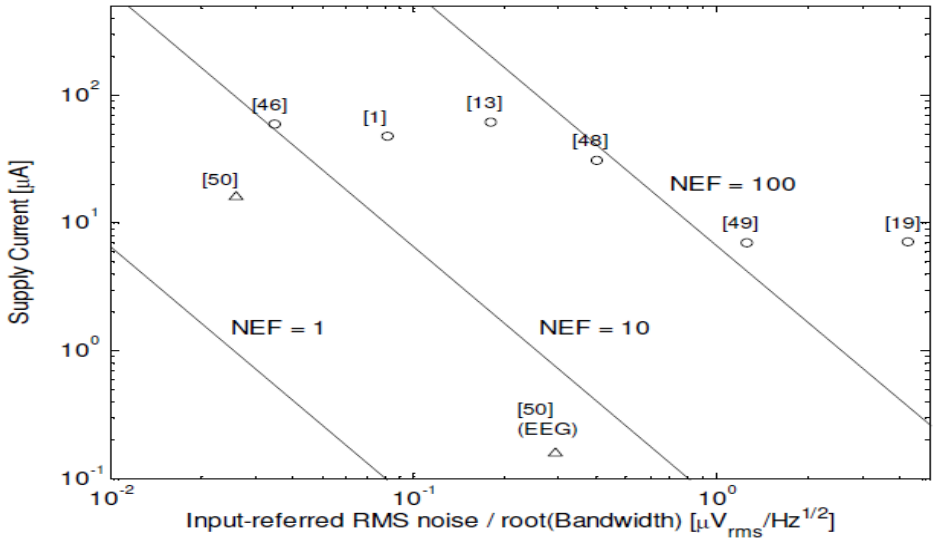

Figure 1: Supply currents vs. normalized noise for reported biomedical amplifiers. The lines indicate constant NEF contours.

Another area in which the reported designs vary is in the method used to cancel DC voltage offsets caused by the electrode-tissue interface. Several of the older designs made use of large off-chip capacitors to achieve low frequency cutoffs. This is not feasible for a FIRS with a large number of amplifiers, as the size of the implanted

unit would be prohibitively large. Another method is to use auto-zeroing techniques such as correlated double sampling or chopper modulation ([1], [2], [4]). The advantage of these techniques is that they save chip area by avoiding the need for large capacitors and resistors. The disadvantage is that these designs require more complex circuitry for the amplifier itself. The most common technique in recent designs is to use capacitively coupled inputs made with on-chip integrated capacitors and highly resistive active elements to achieve a low-frequency cutoff. Several papers have reported creating the resistive elements with the junction resistance of a p-n diode biased near 0 V ([1], [3]), while more recent papers have made use of nMOS transistors biased in the subthreshold region ([6], [7]) and diode connected nMOS or pMOS transistors ([2], [8]). The amplifier design which has been adapted for this work makes use of diode connected pMOS transistors.

IV. AMPLIFIER DESIGN

The LNA design developed for this work is a fully differential implementation which has minimal intrinsic noise, as well as the capability to reject digital interference from other circuit components. The amplifier is based on a single-ended implementation, reported in [2], [5]. The main difference between the previously reported single-ended design and this fully differential design is the need for a CMFB circuit in the OTA of the LNA for the fully-differential design. The schematic of the fully differential bio-amplifier is shown in Figure 2. The mid-band gain A_M is set by C_1/C_2, and for the case where C_1, $C_L >> C_2$, the bandwidth is $gm/(A_M C_L)$, where gm is the trans-conductance of the operational transconductance amplifier (OTA). Transistors M_a-M_d are MOS-bipolar devices acting as "pseudo-resistors" [5]. With positive VGS (as in this case), the parasitic source-well-drain pnp bipolar junction transistor is activated, and the device acts as a diode connected BJT.

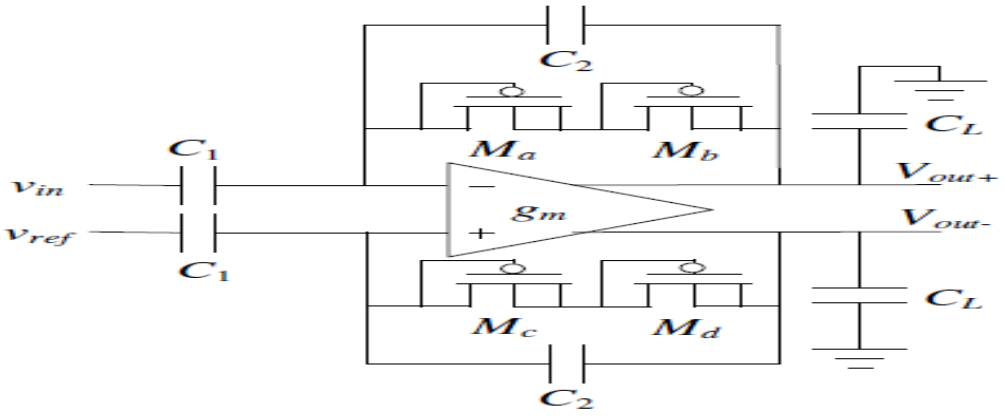

Figure 2: Schematic of fully differential low noise amplifier

For small voltages across these devices, their incremental resistance is very high (see Figure 3). The schematic of the OTA is shown in Figure 4. The topology is a standard current mirror design which is suitable for driving capacitive loads, but the transistor sizing is critical for achieving low noise at low current levels. The CMFB circuit has been omitted from this schematic, but it would take the signals at v_{out+} and v_{out-} as inputs, and its output would be to control the voltage at the node labeled v_{cntrl}. CMFB circuits will be discussed in the next chapter which describes the CMFB circuits used in each of the LNA implementations. Analysis of this circuit reveals the input-referred thermal noise power to be

$$\overline{V_{ni,thermal}} = \left[\frac{16\,kT}{3g_{m1}}\left(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right)\right]\Delta f \qquad (2)$$

Here g_{m1} represents the transconductance of transistors M_1 and M_2, g_{m3} represents the transconductance of transistors M_3-M_6, and g_{m7} represents the transconductance of transistors M_7 and M_8. From this expression it is clear that thermal noise will be minimized if g_{m3}, $g_{m7} << g_{m1}$. We can accomplish this by making $(W/L)_3$, $(W/L)_7 << (W/L)_1$. Sizing devices M_3-M_8 with small W/L ratios forces them to operate in the strong inversion region, where their relative transconductance decreases as $1/(ID)^{1/2}$.

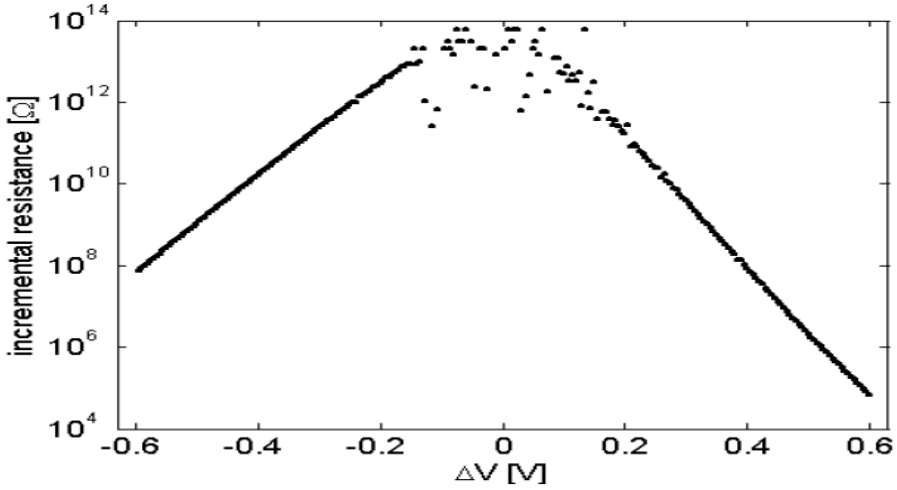

Figure 3: Incremental resistance of single MOS-bipolar element. For low voltages the incremental resistance exceeds 10^{12} Ω.

Sizing devices M_1 and M_2 with large W/L ratios forces them to operate in the weak inversion region, where their relative transconductances are maximized.

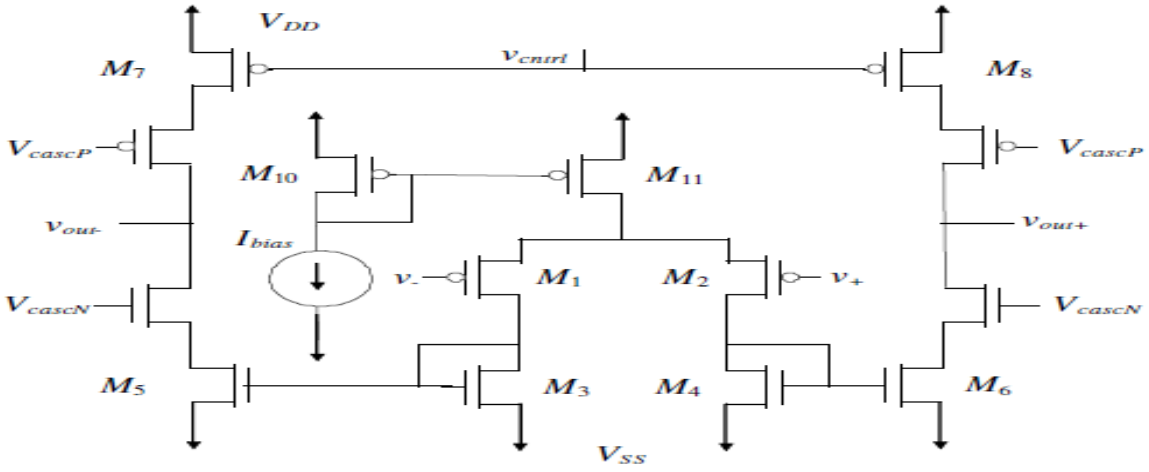

Figure 4: Schematic of operational transconductance amplifier used in low noise amplifier

Flicker noise ($1/f$ noise) is a major concern for low-noise, low-frequency circuits. This design minimizes the effects of flicker noise by using pMOS transistors for the input differential pair and making the gate areas of all devices as large as possible. Flicker noise in pMOS transistors is 1-2 orders of magnitude lower than in nMOS transistors (provided $|VGS|$ does not greatly exceed the threshold voltage) ([5], [3]), and flicker noise in a transistor is inversely proportional to the gate area. There is a limit to the size of the gate areas, imposed both by area consumption and stability concerns. As the gate areas increase, the capacitances seen at the gates of transistors $M_{3,5}$, $M_{4,6}$, and $M_{7,8}$ increase, which moves the non-dominant poles closer to the dominant pole, reducing stability. For more analysis and design details on this circuit, the interested reader is referred to the

most recent paper on the single-ended design [5]. The same design principles described for the single-ended design apply to the fully differential design.

V. CONCLUSIONS

A fully-differential low noise amplifier has been developed and tested with several common-mode feedback circuits. The fully differential design will reject any digital noise generated from the digital circuitry in the FIRS. One of the CMFB circuits tested with the LNA is a novel design developed for this application.

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