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Analytical Study of Integrated CMOS Transmit-Receive Switch Using Inductive Substrate Bias

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ABSTRACT

In this paper, we report on analytical study of transmit receive switch using inductive substrate bias. This research work focuses on the transmit-receive (T/R) switch, which is one transceiver block which has defied integration so far. Modern RF transceiver architectures commonly use a T/R switch to share the use of resources such an antenna. The spiral inductor is a critical component of this technique and a new compact model is proposed and verified by simulation and experiment. The spiral inductor model is incorporated in a tool which allows quick synthesis and analysis of spiral inductors across a variety of geometries and substrate doping.

Keywords : RF Switch, MOSFET, Spiral Inductor.

I. INTRODUCTION

The interest in low-cost, low-power, silicon-based transceiver designs for radio-frequency (RF) applications, such as cell phones and wireless networking, has prompted research in wireless circuit design techniques using complementary-metal-oxide-semiconductor (CMOS) technology. A critical limitation in obtaining fully integrated CMOS wireless systems is the lack of high-quality switches. Consequently, new techniques are required to overcome this problem. Cellular telephones and wireless-local-area-networks (WLAN) are the two major markets for wireless devices. In the last decade, optical fiber transmission capacity has increased. Close on the heels of an enormous increase in wired data bandwidth; a similar increase in the wireless data bandwidth is expected. The WLAN market has picked up in the last couple of years with greater consumer demand for wireless connectivity. This is justification of the work [1]. The interest in low-cost, low-power, silicon-based transceiver designs for radio-frequency (RF) applications, such as cell phones and wireless networking, has prompted research in wireless circuit design techniques using complementary-metal-oxide-semiconductor (CMOS) technology. A critical limitation in obtaining fully integrated CMOS wireless systems is the lack of high-quality switches [2]. This work introduces an inductive substrate bias technique that enables the design of T/R switches in a standard silicon complementary metal-oxide-semiconductor (CMOS) process. This work first describes and analyzes the inductive substrate bias technique which is critical to the performance of the T/R switch. The power handling capability of the switch is 40X higher than other designs reported to date in a CMOS technology. Comparison with simulations suggests that the spiral inductor model developed is indeed accurate. The performance achieved by the switch can be further improved by using better technologies.

II. METHODS AND MATERIAL

Integrated T/R Switch Requirements: Based on previous work [3] and datasheets of existing parts [4], a set of specifications are developed for an integrated T/R switch for 802.11 type wireless-local-area-network (WLAN) systems. The asymmetry in the received and transmitted power levels can be effectively used to arrive at a set of specifications which can be met by designs in a CMOS technology.

Performance Metrics for T/R Switches: The performance of a T/R switch is characterized by several parameters in the transmit and receive modes. A brief description of each of these is presented below:

Insertion Loss (IL): For an ideal switch, no power is lost in the switch. Insertion loss is the power lost in the T/R switch, and is given by 'P_{out}(dB) − P_{in}(dB)', under matched conditions. For a WLAN system, a T/R switch with an IL < 1.5 dB is desirable.

Isolation (Iso.): Isolation is a measure of the signal attenuation from the signal port to the unused port, e.g., in the Tx mode, isolation is measured from the Tx port to the unused Rx port. Although, isolation is usually in the negative dB range, it is common practice to use its absolute value. Isolation greater than 30 dB is desirable to protect the unused port from high power and minimize loss.

Return Loss: This parameter is a measure of the input and output matching conditions. Similar to the isolation parameter, the return loss is usually expressed in absolute value terms even though the actual value is usually in the negative dB range. A return loss greater than 10 dB, at the input and the output, usually indicates acceptable power transfer conditions.

Linearity: Linearity or power handling capability is a measure of the ability of the T/R switch to maintain a low loss without distorting the signal at high input power levels. The desired value of this parameter depends on the maximum input and output power of the application. The 1 dB compression point, P1dB, is a common measure of linearity in T/R switches.

Power: Static power dissipation must be kept as low as practical. Power consumption of less than 1 mW is desirable.

ESD reliability: The ESD performance of the switch is usually measured using the human-body-model (HBM) method. This method essentially measures the robustness of the part when subjected to a static discharge arising from human contact. In applying this model, a 200 pF capacitor is charged to a certain voltage and then discharged through the device-under-test (DUT). The DUT breaks down and ceases to function as the voltage on the capacitor exceeds a certain threshold. This breakdown voltage is used as a measure of the ESD reliability of the DUT. Most GaAs RF components are rated at 500 V HBM. Other practical requirements of the T/R switch include robustness with respect to antenna mismatch. Also, control voltage levels used to toggle the state of the switch must be available in the system. The turn-on and turn-off times typically must be less than about 10 ns to enable rapid transition between Tx and Rx modes, although specific values depend on the application.

III. RESULTS AND DISCUSSION

T/R Switch Specifications: The specifications for an integrated T/R switch used in a WLAN system at 5.2 GHz are summarized below in Table 1. The switch also must meet other criteria which include: Protection of active devices against voltages greater than Vdd, Minimize high temperature effects, Low switch-on/switch-off times, and Robustness with respect to mismatch and large reflections at the antenna.

Table 1 : Target specifications for the T/R switch.

Specification Parameter	Target value
Operating frequency (GHz)	5.2
Insertion Loss (dB)	< 1.5
Return Loss (dB)	> 10
Isolation (dB)	> 25 (Tx mode); > 15 (Rx mode)
Input Linearity: P_{1dB} (dBm)	> 25 (Tx mode); > 10 (Rx mode)
ESD (HBM kV)	> 2
Control Voltages (V)	$0 < V_{ctrl} <$ Vdd
DC power (mW)	< 1

T/R switch Performance: The performance of the protoype has been measured at the I/O pads, viz. Tx, Rx, and Antenna, using Cascade Microtech's ACP-40W GSG probes with 150-μm pitch, while the dc control voltages were supplied using an SGS probe. The unused port in any given measurement is terminated by a 50-Ω load.

Small-signal Measurements: S-parameter measurements to obtain small-signal IL, isolation, and return loss were carried out using the HP8510 Network Analyzer. The measurement setup is shown in Figure 1. Full two-port calibration using Impedance Standard Substrates (ISS) from Cascade Microtech was performed to correct for the effects of the probes and cables. Further corrections, such as contact resistance elimination, were implemented by making use of short, open, and thru test-structures incorporated into the switch design. Pad capacitance subtraction was carried out for the antenna pad but not for Tx and Rx pads since these are absent in an integrated transceiver.

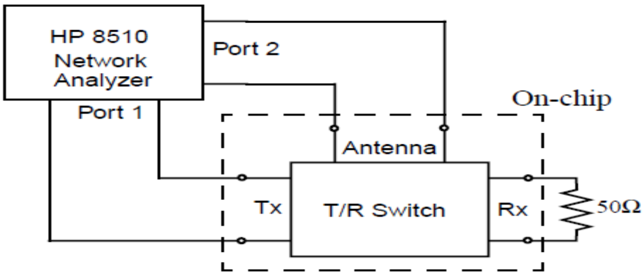

Figure 1: S-parameter measurement setup for IL, isolation and return loss in the Tx mode. In the Rx mode, Port 1 is connected to the antenna, Port 2 is connected to Rx while Tx is terminated with 50 Ω.

Measured results given in Figures 2 and 3, show that the IL at 5.2 GHz, as given by S_{21}, is 1.5 dB and 1.4 dB for the transmit and receive mode, respectively. In the transmit mode, the measured isolation is 30 dB, assuring adequate protection of the LNA from the high-power levels transmitted by the PA. Isolation measured in the receive mode is 15 dB, which is sufficient as the received power is quite low. The return losses, S_{11} and S_{22}, in both modes are greater than 10 dB indicating acceptable matching.

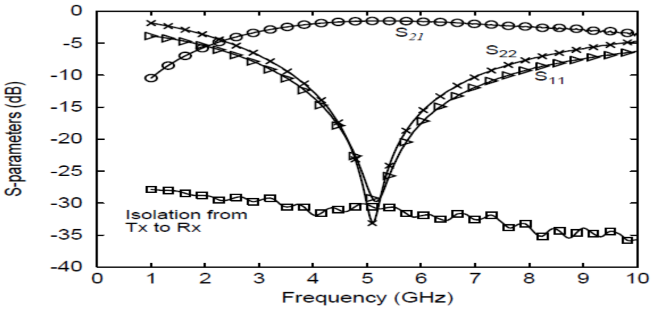

Figure 2: Measured S-parameters and isolation in the transmit mode

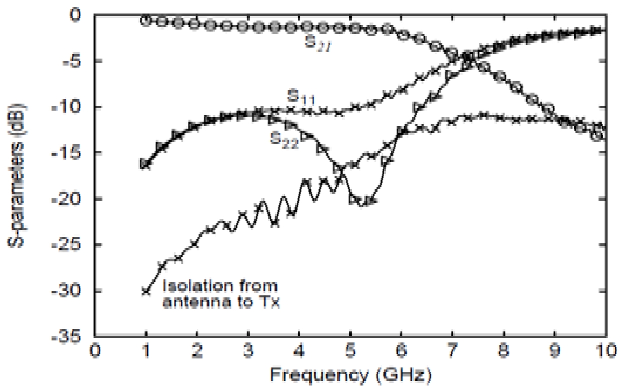

Figure 3: Measured S-parameters and isolation in the receive mode.

Power Handling Capability: Linearity of the switch is measured using the HP83711 signal generator along with an external power amplifier as shown in Figure 4. The output signal is measured by a HP8653 spectrum analyzer. As shown in

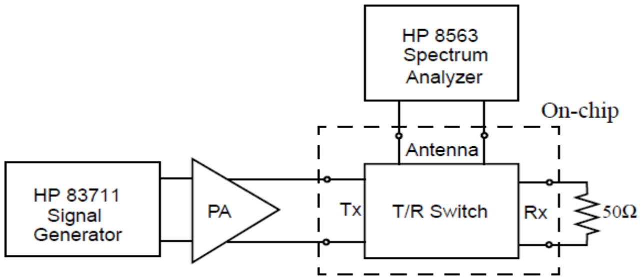

Figure 4 : Linearity measurement setup in the Tx mode. The unused Rx port is terminated by a 50-Ω load.

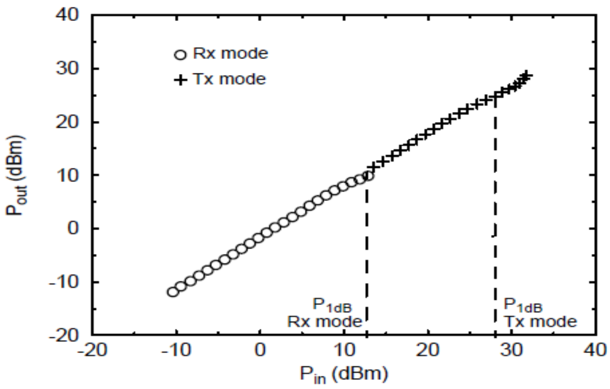

Figure 5 : Measured linearity of T/R switch in Tx and Rx modes.

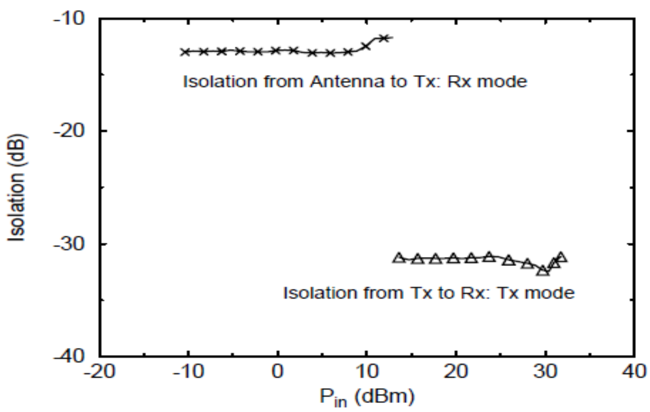

Figure 6 : Measured isolation under high input powers up to P_{1dB} in Tx and Rx modes. No degradation is observed up to P_{1dB} in the Tx mode.

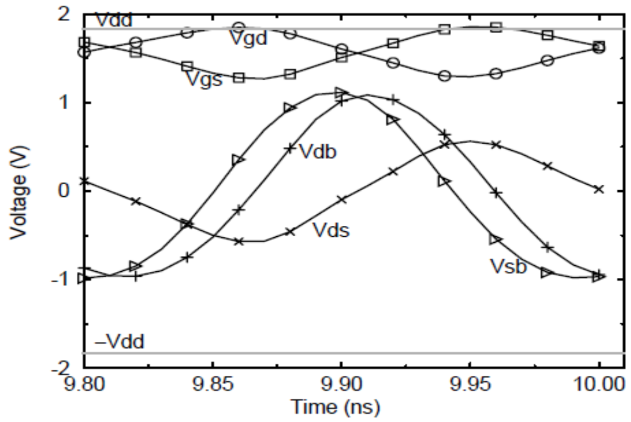

Figure 7: Simulated voltage waveforms for M_1 in Tx mode with Pin = 27.5 dBm and Pout = 25.8 dBm. Note that none of the voltages exceed +/– 1.8 V

Figure 6, the linearity, measured as P1dB, is 28.0 dBm and 11.5 dBm in the transmit mode and receive mode, respectively. Using the same setup, isolation performance is investigated for high input powers. Measurements results in Figure 7 confirm that isolation remains at its small-signal value up to input powers of 8 dBm and 30 dBm in the Rx and Tx mode, respectively.

IV. CONCLUSION

The inductive substrate bias technique using on-chip spiral inductors significantly enhances the power handling capability of the switch. The prototype achieved a power handling capability which is about 40x its CMOS counterparts, and an overall performance level comparable to its commercially available discrete counterparts. Simultaneously, it increases the level of RF transceiver integration by including a matching circuit which enables the LNA and PA to be matched independently. As the comparison between measurements and simulations show, the spiral inductor model developed previously allows prediction of circuit behaviour at high frequencies.

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