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An Area Efficient Full Adder Design Using Modified Mux In QCA

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ABSTRACT

QCA technology is considered to be a possible alternative for circuit implementation in terms of energy efficiency, integration density and switching frequency which can replace CMOS implementations as nm technology decreases. Multiplexer (MUX) can be considered to be a suitable candidate for designing QCA circuits. The proposed MUXes outperform the best existing design in terms of power consumption with approximate reductions. Moreover, similar or better performance factors such as area and latency are achieved compared to the available designs. These MUX structures can be used as fundamental energy-efficient building blocks for replacing the majority-based structures in QCA. In this project, the MUX design is modified and proposed in QCA. QCA technology is considered to be a possible alternative for circuit implementation in terms of energy efficiency, integration density and switching frequency which can replace CMOS implementations as nm technology decreases. Multiplexer (MUX) can be considered to be a suitable candidate for designing QCA circuits. The proposed full adder outperforms the best existing design in terms of area with approximate reductions. Moreover, similar or better performance factors such as power and latency are achieved compared to the available designs. The scalability property of the proposed design is excellent and can be used for energy-efficient complex QCA circuit designs. These implemented designed are simulated and waveforms are observed using QCA designer tool.

Keywords: QCA Technology, Full Adder, QCA Clocking

I. INTRODUCTION

The current Complementary Metal Oxide Semiconductor (CMOS) technology has almost reached its physical scaling limitation. The reduction of CMOS technology brings severe challenges in terms of physical dimensions, power consumption and leakage current. In the future development of integrated circuit technology, nano electronics technology has been widely studied for its novel

properties. Quantum-dot Cellular Automaton (QCA) technology is a potential alternative to CMOS technology [1]

Unlike traditional circuits, as for this technique, the logic states are encoded based on the position of the electrons. Therefore, it not only provides a nano level solution method, provides a new paradigm for information transmission, calculation and exchange, but also has the advantages of fast switching speed, low power consumption, and high density [2]

QCA cell is the smallest unit of QCA technology. It is a tinynano scale-building block for computing and signal processing. QCA cells communicate with each other through Columbus repulsion on a large array using electron permutation of quantum-dots in cells [3].

This feature would make this paradigm radically different from the existing current-switching transistors. QCA technology used a smart information encoding mechanism suitable for nanostructures, eliminating the problems of the current-switching transistors. The QCA cell array contains the information based on electrons charges polarization arrangement and does not include the transport of charges. In other word, the interaction between QCA cells and neighboring cells is directly generate the dynamic and stable to one of two ground states (i.e. logic '0' and logic '1'). In the QCA circuit, the timing, calibration, and recovery of signals are controlled by an external clock and operated according to the rules of Boolean logic [4]

QCA technology provides a revolutionary approach to computing and opens up a new pattern for circuit design. The most important operations in computer systems such as multiplication, subtraction, and division are based on simple modifications of the full adder circuit. Therefore, it can be seen that in computers, information processing and operations, the full adder is the basic and key element. So, an efficient adder structure is the key to designing a high-performance arithmetic circuit. The high performance full adder circuit design has also attracted much attention. Therefore, many researchers have designed full adder circuits to improve the efficiency of full adder circuits in QCA technology. In this paper, we propose an efficient QCA full adder structure. Compared with the adder design structure in other previous literatures, it has been greatly improved based on a comprehensive consideration of some QCA circuit's metrics.

In this paper, we propose an efficient full adder circuit in QCA. Compare to other QCA based full adder design, the number of the QCA cells is few, layout area of the circuit is small, the time delay from input cell to output cell of this circuit is short, and the value of cost is low.

The organizational framework of this study divides the research work in the different sections. The literature review is presented in section 2. Further, in section 3, QCA technology was discussed. Moreover, in next section IV, briefly explain about Proposed System and finally the Simulation results discussed in section V. Conclusion and future work are presented by last sections VI.

II. LITERATURE SURVEY

Oya, T.; Asai, T.; Fukui, T.; Amemiya, Y. A majority-logic nanodevice using a balanced pair of single-electron boxes. J. Nanosci. Nanotechnol. 2002, 2, 333–342 - In this paper describes a majority-logic gate device that will be useful in developing single-electron integrated circuits. The gate device consists of two identical single-electron boxes combined to form a balanced pair. It accepts three inputs and produces a majority-logic output by using imbalances

caused by the input signals; it produces a 1 output if two or three inputs are 1, and a 0 output if two or three inputs are 0. We combine these gate devices into two subsystems, a shift register and an adder, and demonstrate their operation by computer simulation. We also propose a method of fabricating the unit element of the gate device, a minute dot with four coupling arms. [14]

Fahmy, H.A.H.; Kiehl, R.A. Complete logic family using tunneling-phase-logic devices. In Proceedings of the Eleventh International Conference on Microelectronics, ICM '99, Safat, Kuwait, 22–24 November 1999; pp. 153–156 -This paper presents the work done to develop and characterize the behavior of binary Tunneling Phase Logic (TPL) devices. Three input NAND, NOR and MINORITY functions are demonstrated using a single TPL element. The fan-out of the gates is discussed as well as the loading effects of multiple gates in cascade. Stable regions of operation are reported and future research possibilities are explored. The majority of digital circuits use voltage levels to indicate the different logic values. Beside the voltage, current-mode, charge-mode (like Charge Coupled Devices or Single Electron Logic and phase-mode circuits also exist but are less popular [15].

Zahoor, F.; Hussin, F.A.; Khanday, F.A.; Ahmad, M.R.; MohdNawi, I.; Ooi, C.Y.; Rokhani, F.Z. Carbon nanotube field effect transistor (cntfet) and resistive random access memory (rram) based ternary combinational logic circuits. Electronics 2021, 10, 79- The capability of multiple valued logic (MVL) circuits to achieve higher storage density when compared to that of existing binary circuits is highly impressive. Recently, MVL circuits have attracted significant attention for the design of digital systems. Carbon nanotube field effect transistors (CNTFETs) have shown great promise for design of MVL based circuits, due to the fact that the scalable threshold voltage of CNTFETs can be utilized easily for the multiple voltage designs [16].

Tabrizchi, S.; Panahi, A.; Sharifi, F.; Mahmoodi, H.; Badawy, A.H.A. Energy-Efficient Ternary Multipliers Using CNT Transistors. Electronics 2020, 9, 643 In recent decades, power consumption has become an essential factor in attracting the attention of integrated circuit (IC) designers. Multiple-valued logic (MVL) and approximate computing are some techniques that could be applied to integrated circuits to make power-efficient systems. By utilizing MVL-based circuits instead of binary logic, the information conveyed by digital signals increases, and this reduces the required interconnections and power consumption.[17].

III. QCA TECHNOLOGY

Fundamental QCA components and logic gates The basic element in QCA technology is a QCA cell, which is a nanoscale square structure with two electrons and four quantum dots. According to coulomb repulsion, two electrons must be located on the antipodal site of the cell in ground states. If the potential barrier be tween quantum dots is reduced by a certain value, the electrons in the cell can arbitrarily tunnel between the quantum-dots. It's important to note that the tunneling effect occurs only within the cell. Therefore, there are two stable charge configurations in the QCA cell representing two polarization states. These two states can be used to encode binary information, the polarizations '-1' and '+1' represent the binary logic values '0' and '1', respectively. Figure 1(a) and 1(b) show two types of QCA cells, called normal cells and rotated cells, respectively. Rotated cells are usually used for coplanar crossings. A QCA Wire is created by placing a series of cells side by side. As shown in Figure 1(c), the QCA wire includes an input cell, an output cell and some free cells. Due to Coulomb interactions, the value of a logical '0' or '1' from the input cell will be transfer through the chain of free cells [5] In the

traditional digital circuit design, the basic logic gates includes AND gate, OR gate and NOT gate. Similarly, the base logic gates in QCA are inverter and 3- input majority gate.

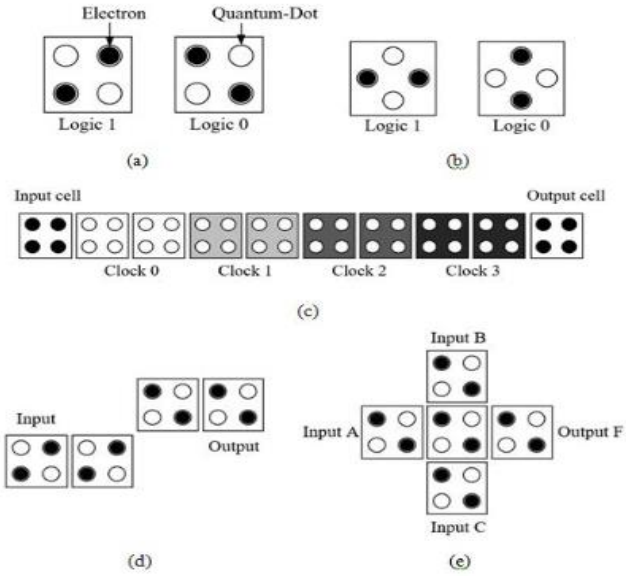

Figure 1 : QCA logic and fundamental QCA components: (a) normal cell; (b) rotated cell; (c) QCA wire; (d) Inverter gate; (e) 3-input majority gate

Inverter is usually constructed by positioning two cells diagonally from each other. In QCA technology, inverter can be included in the inter connected wire because it does not create any additional latency.

Figure 1(d) shows a schematic diagram of the inverter gate. A structure of 3-input majority gate is more complicated than the inverter's. The schematic of the 3-input majority gate is shown in Figure 1(e), which demonstrates it consists of five QCA cells, shaped like a cross. If any two or three input values of the 3-input majority gate are '1', the output value of the 3-input majority gate is '1', and in other cases the output value is '0'. Obviously, theoretically setting any one input of the 3-input majority gates to '0' will change the 3-input majority gate into a 2-input AND logic gate. Similarly, setting any one input of the 3-input majority gates to '1' will change the 3-input majority gate into a 2-input OR logic gate. Therefore, the Boolean logic expression of the 3-input majority gate can be expressed as

$$F=AB+BC+AC \ldots\ldots\ldots (1)$$

In QCA technology, all logic functions can be implemented by the combination of inverter and the 3-input majority logic gate [5].

With the development of QCA technology, a majority logic gate with five inputs was created. The design and implementation of the 5-input majority gate based on QCA technology has been explored in work such as Ref. [6]

Five-input majority gates work the same way as three-input majority gates, if any three or more of the 5-input values in the 5-input majority gate are '1', the output of the 5-input majority logic gate is '1', the output of 5-input majority logic gate is '1', otherwise it is '0'. Similarly, the output of a 5-input majority gate expression is

$$F=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE + CDE+AC \ldots\ldots\ldots (2)$$

A. QCA clocking scheme

QCA clocking scheme Four-phase clocking in each QCA clocking zone is typically used. There is a 90◦ phase shift from one clocking zone to the next, which is shown in Figure 2. The clock signals of QCA circuits are generated by an electric field applied to the QCA cells to modulate the tunneling barrier between dots. The transition and conversion of information takes place in the 'SWITCH' phase. A cell is latched during the 'HOLD' phase. A clocked QCA 'wire' can be considered as a chain of D-latches. The smallest unit of delay in QCA is a clocking zone delay (latency) which is the quarter of the clock cycle delay.

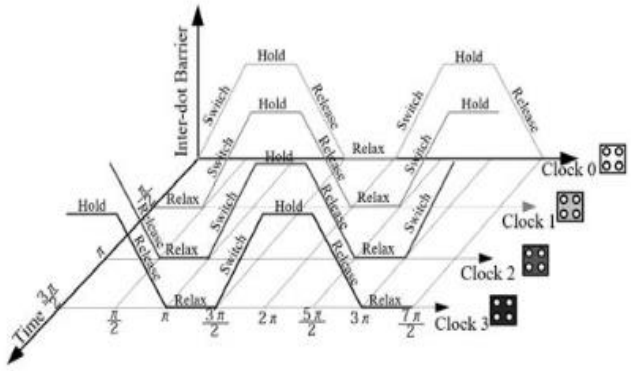

Figure 2:Clocking scheme

B. QCA Wire Crossings

Because of the interaction of adjacent cells, the input data is carried down arrays of the QCA cells. Binary data is transferred from one physical location to another by wire. In general, there are two types of wire crossing, which that is multilayer crossover and coplanar crossover. As shown in Figure 3(a), a coplanar crossing is proposed [7] as a unique property of a QCA layout that uses only one layer for the crossover. A coplanar crossover uses both normal cells and rotated cells, which they do not interact with each other when they are properly aligned. The other option is multilayer crossover [8], which uses a minimum of three layer and used more cells. It similar to the placement and routing of metal wires in CMOS technology as shown in Figure 3(b). According to coulomb repulsion, the polarization of stacked cells becomes inverse when the value is passing between layers. So, the multi-layer crossover needs at least three layers to achieve.

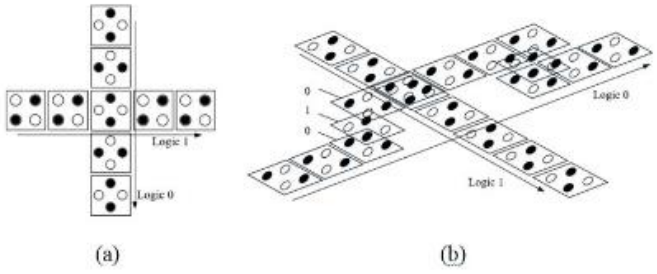

Figure 3: QCA crossover: (a) coplanar crossover; (b) multilayer crossover

IV. PROPOSED METHOD

In the proposed method, an improved way to implement full adder using mux is implemented in QCA technology. By comparing the previous suggested QCA architectures like 2:1MUX, 4:1MUX, from which full adder circuit is implemented. But the design is using more number of QCA cells which increases the total area consumption. On comparison the proposed design can be said to have improvement in parameter such as area making it as area efficient design.

QCA-cell plays an imperative part in QCA strategy, which permits us execute the couple of the computation and exchange of the information through the cover. An uncomplicated that which electrons could retain. Every cell is involved with a pair of electrons. The Coulombic interchange among electrons could make two unmistakable cells passes with distinctive charge courses of action. This field of an electron is implied by two dots in the cube cell.

Columbia's repugnance compels the electrons to include the furthermost dots in a QCA cubicle that takes over the near most energy states-governed of the circuits. Cell polarization implies the corresponding field of the electrons inside the QCA cell and that choose either assigning binary "1" or binary "0". Two states of QCA cells are available to begin with is 90° normal cells and the other is 45° rotated cells. A 90° cell with the polarization of p = +1 that knows binary 1. The proposed full adder design using modified XOR in QCA is shown in fig.

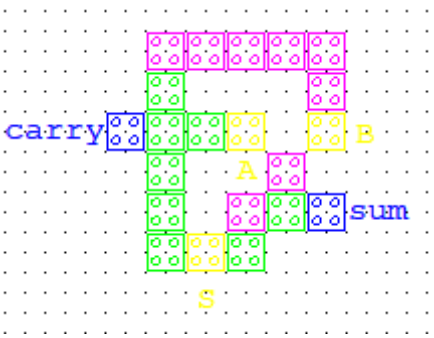

Figure 4: Proposed Full adder

Proposed system Analysis

Imagine a full adder with three inputs (A, B, and C). The C input will act as the carry bit which is transferred from the previous stage. The implementation function of a full adder is as follows:

$$\text{Sum} = A \oplus B \oplus C,$$

$$\text{Carry} = AB + AC + BC.$$

As can be seen from (1) and (2), each full adder has two outputs (Sum and Carry) and the Sum output is the result of XOR of circuit inputs. According to (2) it should also be noted that carry can be defined as an output of 3-input majority gate (with A, B and C as its inputs). Hence, we can design an optimal full adder in QCA technology with this simple reason. The implementation of this full adder is shown in Fig. 4. This figure shows that the occupied space and the used cells in the proposed circuit are fewer than the circuits using only three-input and five-input majority gates. Table 1 shows the results related to the comparison of a few optimal full adders and the proposed circuit. According to this table, we can conclude that the proposed structure is an optimal circuit in terms of occupied space and the number of cells (while it has a standard delay) in comparison to other circuits. In addition, it should be mentioned that the proposed full adder is designed in coplanar method and has an acceptable delay. As can be seen from Fig. 1, the proposed design can be generalized to more bit full adder design in the coplanar method. This is another advantage of the proposed full adder.

V. SIMULATION RESULTS

The possible output and input combinations are shown in fig.5 and fig.6 in both existing system and proposed system. The existing system implemented based on 2:1 and 4:1 multiplexers and for this design took 43 cells in design structure shown in table 1. Similarly the proposed system implemented based on Full adder using QCA and for this design took 21 cells in design structure shown in table 1.

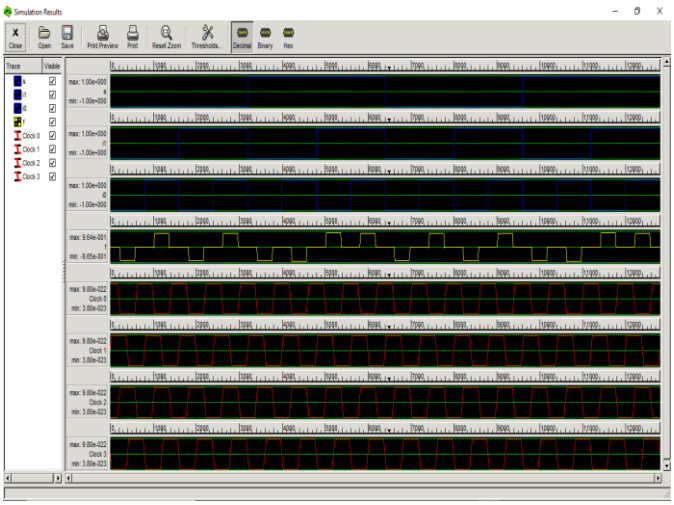

Figure 5: Simulation results for the Existing System

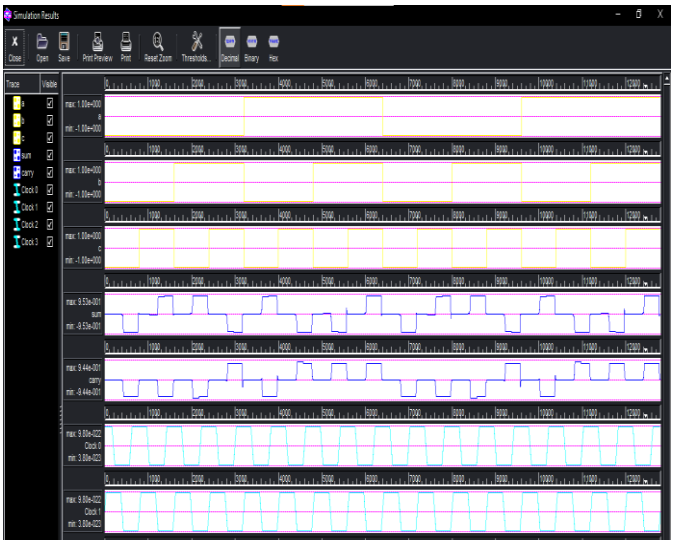

Figure 6: Simulation results for the full adder circuit

From the Figure 5 and 6, we can know, when the input value, and get the output. The results confirm that the proposed full adder work properly and exactly like the function of a full adder.

TABLE I

COMPARISON TABLE

Design	Cell count
Existing System	42
Proposed System	21

Table I shows the comparative analysis of full adder design using QCA. Existing System full adder has been constructed using 42 standard cell structure in which delay is more. The proposed design requires

the 21 standard QCA cell structure has better performance in terms of area and delay.

VI. CONCLUSION

In this paper, an optimal way to execute a full adder using MUX in QCA is designed in the QCA Designer simulation tool for nanotechnology applications has been proposed. The morphological characteristics of this efficient design ease highly dense circuitry execution. According to execution parameter comparison, it is observed that the proposed half adder architectures buildup of ultra-efficient full adder to attain efficient and optimum layouts and achieved less parameter count like area occupied.

Future works

The work can be extended to design 8-bit full adder with QCA technology.

VII. REFERENCES

[1]. Lent CS, Taugaw PD, Porod W, et al . Quantum cellular automata. Nanotechnology (IOPScience), 1993, 4 (1): 49-57. https://doi.org/10.1088/0957-4484/4/1/004

[2]. Lent CS and Tougaw PD. A device architecture for com- puting with quantum dots. Proceedings of the IEEE, 1997, 85 (4): 541-557. https://doi.org/10.1109/5.573740

[3]. Orlov AO, Amlani I, Bernstein GH, et al . Realization of a functional cell for quantum-dot cellular automata. Science, 1997, 277 (5328): 928-930. https://doi.org/10.1126/science.277.5328.928

[4]. Amlani I, Orlov AO, Kummamuru RK, et al . Experimental demonstration of a leadless quantum-dot cellular automata cell. Applied Physics Letters, 2000, 77 (5): 738-740. https://doi.org/10.1063/1.127103

[5]. Zhang R, Walus K, Wang W, et al . A method of majority logic reduction for quantum cellular automata. IEEE Trans actions on Nanotechnology, 2004, 3 (4): 443-450. https://doi.org/10.1109/TNANO.2004.834177

[6]. Navi K, Sayedsalehi S, Farazkish R, et al . Five-input majority gate, a new device for quantum-dot cellular automata. Journal of Computational & Theoretical Nanoscience, 2010, 7 (8): 1-8. https://doi.org/10.1166/jctn.2010.1517

[7]. Tougaw PD and Lent CS. Logical devices implemented using quantum cellular automata. Journal of Applied Physics, 1994, 75 (3): 1818-1825. https://doi.org/10.1063/1.356375

[8]. Mohammadi M, Mohammadi M and Gorgin S. An efficient design of full adder in quantum-dot cellular automata (qca) technology. Microelectronics Journal, 2016, 50 (16): 35-43. https://doi.org/10.1016/j.mejo.2016.02.004.

[9]. Azghadi MR, Kavehei O and Navi K. A novel design for quantum-dot cellular automata cells and full adders. Journal of Applied Sciences, 2007, 7 (22): 3460-3468. https://doi.org/10.3923/jas.2007.3460.3468

[10]. Labrado C and Thapliyal H. Design of adder and subtractor circuits in majority logic-based field-coupled qca nanocom puting. Electronics Letters, 2016, 52 (6): 464-466. https://doi.org/10.1049/el.2015.3834

[11]. Hashemi S, Tehrani MA and Navi K. An efficient quantum dot cellular automata full-adder. Scientific Research & Es says, 2012,7 (2): 177-189.

[12]. Navi K, Farazkish R, Sayedsalehi S, et al . A new quantum dot cellular automata full-adder. Microelectronics Journal, 2010, 41 (12): 820-826. https://doi.org/10.1016/j.mejo.2010.07.003

[13]. Cho H and Swartzlander EE. Adder and Multiplier Design in Quantum-Dot Cellular Automata. IEEE Transactions on Computers, 2009,58 (6): 721-727. https://doi.org/10.1109/TC.2009.21 Advances in Computers and Electronics c © 2020 by SyncSci Publishing . All rights reserved.

[14].Oya, T.; Asai, T.; Fukui, T.; Amemiya, Y. A majority-logic nanodevice using a balanced pair of single-electron boxes. J. Nanosci. Nanotechnol. 2002, 2, 333–342

[15].Fahmy, H.A.H.; Kiehl, R.A. Complete logic family using tunneling-phase-logic devices. In Proceedings of the Eleventh International Conference on Microelectronics, ICM '99, Safat, Kuwait, 22–24 November 1999; pp. 153–156

[16].Zahoor, F.; Hussin, F.A.; Khanday, F.A.; Ahmad, M.R.; MohdNawi, I.; Ooi, C.Y.; Rokhani, F.Z. Carbon nanotube field effect transistor (cntfet) and resistive random access memory (rram) based ternary combinational logic circuits. Electronics 2021, 10, 79

[17].Tabrizchi, S.; Panahi, A.; Sharifi, F.; Mahmoodi, H.; Badawy, A.H.A. Energy-Efficient Ternary Multipliers Using CNT Transistors. Electronics 2020, 9, 643

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