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Design of High Performance and Power Efficient Flash ADC

Kareti Sai Tejaswi[1], Dr. S. Leela Lakshmi[2]
[1]PG Scholar, Department of ECE, VEMU Institute of Technology, P.Kothakota, Andhra Pradesh, India
[2]Professor, Department of ECE, VEMU Institute of Technology, P.Kothakota, Andhra Pradesh, India

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ABSTRACT

In this paper, Flash Analog to digital converter is implemented. The designed Flash ADC consists of a resistive ladder network, comparators, the thermometer to a binary encoder and the entire design is carried out using Tanner tools employing 180nm technology. The reference voltage applied to the resistive ladder network is 1.8V. A two-stage operational amplifier is used as a comparator in the flash ADC. Here, we are modifying the structure of operational Amplifier using Power Gating Technique. Binary code is obtained from the thermometer code by utilizing a Mux based encoder by designing the MUX in domino Logic. The major problem that usually appears in flash ADC is as the number of resolution bits increases, the Area, as well as the power consumption of the circuit, also increases. In this paper, we principally concentrated to lessen the propagation delay of the ADC by optimizing encoder circuitry. With the purpose of reducing latency, Encoder is implemented using 2:1 mux based on Pseudo NMOS Logic. Performance parameters of Flash ADC such as delay as well as average power are calculated and compared.

Keywords : Domino Logic, Flash ADC, Pseudo Logic, Operational Amplifier

I. INTRODUCTION

Flash analog to digital converter has the highest speed of any type of ADC. It uses one comparator per quantization level (2N1) and 2N resistor string. The reference voltage is divided into 2 N values, each of which is fed into a comparator. The comparator compares the input voltage with the each reference voltage value and results the binary output in terms of '0's and '1's at the output of the comparator that is called as thermometer code which consists of string of '0's and '1's. A thermometer code exhibits all zeros for each resistor level if the value of input voltage is less than the reference voltage and one's if the input voltage is greater than or equal to the reference voltage. Block diagram of N-bit Flash ADC is shown in Fig. 1. Flash analog to digital converter has the highest speed of any type of ADC. It uses one comparator per quantization level (2N1) and 2N resistor string. The reference voltage is divided into 2 N values, each of which is fed into a comparator.

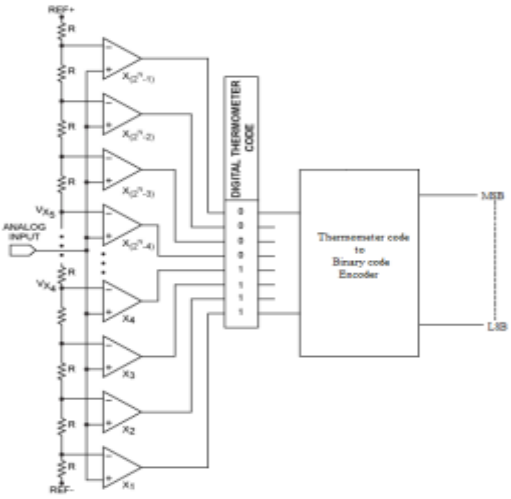

Figure 1: Block diagram of N-bit Flash ADC

The comparator compares the input voltage with the each reference voltage value and results the binary output in terms of '0's and '1's at the output of the comparator that is called as thermometer code which consists of string of '0's and '1's. A thermometer code exhibits all zeros for each resistor level if the value of input voltage is less than the reference voltage and one's if the input voltage is greater than or equal to the reference voltage. Block diagram of N-bit Flash ADC is shown in Fig. 1.

In wireless communication world entire signals are analogues. But we are surrounded by Digital devices. Everything in the universe measures all signals with analog only. But, how analog parameters are in digital devices?. Most of the applications are in digital signal processors only. Like microcontrollers, microprocessors. Analog to Digital converters are the mixed signals of both analog and digital for processing the information or data. Present days most of the electronic applications are in digital only. Because of digital have finite set of occurrences. And also important factor is low power consumption, low operating voltage with a high speed data transmission. So we focus on efficient analog to digital converter.

We have different types of analog to digital converters like Successive Approximation (SAR), Dual slope ADC, Sigma delta ADC and Flash ADC. Among those most cases we prefer only flash ADC. "Because of its better tradeoff between its all performance metrics".[1] Some of the basic factors which depend on the performance of ADC are input signal bandwidth, resolution, quantization error, SNR, differential non linearity and integration non linearity. But resolution always inversely proportional to conversion rate of the device.

The organizational framework of this study divides the research work in the different sections. The literature review is presented in section 2. Further, in section 3, QCA technology was discussed. Moreover, in next section IV, briefly explain about Proposed System and finally the Simulation results discussed in section V. Conclusion and future work are presented by last sections VI.

II. LITERATURE SURVEY

Kriti Thakur, Sandeep Kaur Kingra [1] was proposed Design and Implementation of Hybrid 4-bit Flash ADC in 90nm CMOS technology with 1.2V supply voltage and 1GHz frequency. In this design double tail comparator is used to improve speed. For digitizing comparator yields, A multiplexer based encoder design is used. .It consume power upto 1.4mW and delay of the circuit is 1.8ns.

Liyaqat Nazir, Burhan Khurshid, et al. [2] was proposed A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique in 90nm CMOS technology. The ADC consumes 1.9807 mW from a 1.2V supply. To improve the speed TIQ based comparator is used. A simple and fast analog to-digital converter architecture that uses pseudo-dynamic logic encoder to offer higher data conversion rates while maintaining a low power consumption level has been proposed .the effective number of bits is 4-bits.

Parag P. Kute, Pravin Dakhole, et al. [3] was praposed Cross Coupled Digital NAND Gate Comparator Based

Flash ADC in 180nm technology. This ADC is designed in TANNER SEDIT 13. The effective number of bits is 4-bits. In this paper a digital three input NAND based comparator is constructed for the 4 bit Flash ADC. It completely eliminates the use of reference ladder, instead comparator trip points are generated by varying the width W of the transistors. Thermometer to binary decoders are presented, which shows that a multiplexer based decoder is more attractive approach since the amount of hardware and area consumption is less compared to other presented decoders and critical path is shorter. This makes design possible for low power consumption. Hence multiplexer based decoder is fast and compact for ADC implementation.

Panchal S. D., Dr. S. S. Gajre, Prof. V. P. Ghanwat [4] was proposed Design and implementation of 4-bit flash ADC using folding technique in cadence tool. In this design to improve speed folding technique is used.

Bala Dastagiri N, Abdul Rahim B,et al.[5] was proposed Domino Logic Based High Speed Dynamic Comparator in 130nm CMOS technology with 0.8V supply voltage. In this design domino logic based double tail comparator is used to improve speed. Maintaining the offset voltage stability, to improve speed, power consumption and delay, which resulted in increase in speed and a nominal change in power consumption as compared to existing double tail, and preamplifier based comparators. Therefore we can say that small changes in design of conventional comparator circuits there is comparativelyslight increase in speed. This design consumes power 1.7640 nw with delay 37.782ns at slew rate 10.941G.

Rahul D. Marotkar, Dr. M. S. Nagmode [6] was proposed Design of Low Power Encoder through Domino Logic for 4 Bit Flash Analog to Digital Converter in 90nm Technology using Cadence Tool with 1.2V supply voltage. The simulation results are calculated and the average power consumption of the proposed encoder is 0.01728mW which is very useful for making high speed devices as compared to the current mode logic.

Mr. K. N. Hosur, Mr. Dariyappa, Mr. Shivanand, Mr. Vijay, Mr. Nagesha, et al, [7] was proposed Design of 4 Bit Flash ADC using TMCC & NOR ROM Encoder in 90nm CMOS Technology. In this design comparator and encoder circuits are implemented using TMCC and NOR ROM encoder respectively. The output of the comparators is in the encoded form. Therefore an encoder has to be designed in order to convert the encoded signal into n bits data (digital) which is binary code. This can be done by using the ROM encoder. The power consumption of proposed ADC is 4.43mW whereas operating input frequency of 2MHz and a operating voltage of 1.8 Volt.

Marcel Siadjine Njinowa,Hung Tien Bui, et al. [8] was praposed Design of Low Power 4-Bit Flash ADC Based on Standard Cells in 180nm CMOS technology with 1.8V supply voltsge at sampling speed of 400MHz. The converter utilizes comparators created using only logic gates for converting analog input signals to digital values. To help maximize operating speed, the proposed design uses the Fat-tree method. This design consumes power 6.9mw in 180nm technology.

III.EXISTING SYSTEM

A. Domino Logic

There are various methods to implement the design equations for the conversion of thermometer code to binary code. Static CMOS, pseudo NMOS, dynamic logic and Domino logic are the variety of logic styles utilized for the implementation. Static CMOS implementation is generally preferred in the noisy environment due to the property of less sensitivity towards the noise. As the circuit size increases, the number of transistor usage also increases largely which increases the power dissipation. The maximum frequency of operation of static CMOS

implementation of the conversion is 1 GHz. To improve the speed, dynamic logic implementation is used. With this implementation, maximum of 4 GHz operation is attained. To further improve the speed as well as to reduce the number of transistors, pseudo NMOS logic implementation is used. By using pseudo NMOS logic, maximum of 5 GHz operation is obtained with a very high value of power dissipation. To reduce the power dissipation by keeping the frequency of operation same, Domino CMOS logic implementation is used. Smaller critical path delay, low transistor count and medium values of power dissipation and power delay product makes

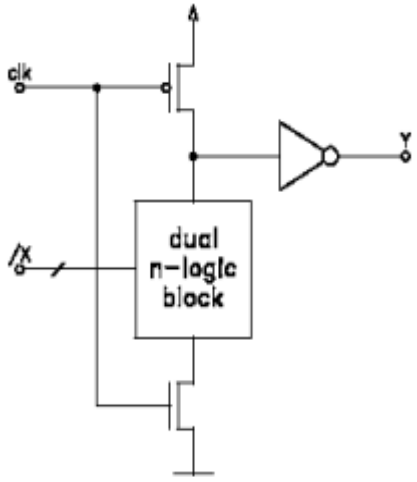

Figure 2: Basic structure of Domino logic

Domino CMOS logic implementation a preferable choice over other logic style implementation for high speed Flash ADC design. Basic diagram of Domino logic is shown in Fig. 2. Domino logic consisting of the two phase when CLK=0 it occurs the "Pre-charge" phase, when CLK=1 it occurs "Evaluation" phase. In Domino logic input values is changed only during Pre-charge phase, if the value is changed during the Evaluate phase it can interrupt the output voltage.

B. Two Stage op-Amp

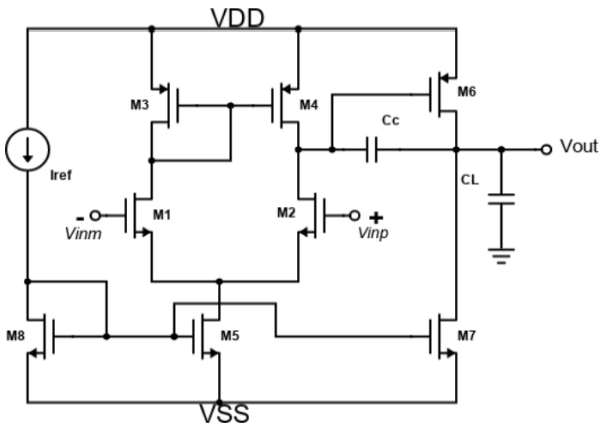

Figure 3: Block diagram of two stage op-amp

The above figure 3 shows a block diagram of the two-stage op-amp. It consists of a differential voltage gain stage followed by a common source gain stage. Differential inputs are applied through the M1 transistor along with the M2 transistor. Op-amp Biasing is furnished with the transistors M5 and M8 to ensure all transistors in saturation. The current mirror formed by the transistor M3 and M4 mirrors current from transistor M1 and is subtracted from the transistor M2. If sufficient gain is not obtained during the differential stage then we use a common source amplifier as the gain stage which is formed by transistors M6 and M7. In this paper, the comparator is operated with sinusoidal input of 1.8 volts. It compares with the reference voltage which is obtained from the resistive ladder network and provides logic high or logic low. Ultimately square waveform will be generated.

IV. PROPOSED METHOD

In the proposed method, an improved way to implement full adder using mux is implemented in QCA technology. By comparing the previous suggested QCA architectures like 2:1MUX, 4:1MUX, from which full adder circuit is implemented.

A. Pseudo Logic

In Pseudo NMOS Logic the PDN is like that of an ordinary static gate, but the PUN has been replaced with a single pMOS transistor that is grounded so it is always ON as in Fig. 4(b). The pMOS transistor widths are selected to be about 1/4 the strength (i.e., 1/2 the effective width) of the nMOS PDN as a compromise between noise margin and speed; this best size is process-dependent. In this way the area required to implement logics have been reduced which in turn increases the speed. But these Pseudo NMOS logics have various other drawbacks such as slow rising transitions, contention on the falling transitions, static power dissipation.

In this chapter, the flash ADC is presented in a novel architecture. Here, the structure of Op-amp and Mux is modified. The architecture of operational Amplifier is designed using Power Gating Technique. And the schematic of Mux is drawn using Pseudo NMOS Logic. This modified architectures of operational Amplifier and Mux is used as comparator and Encoder in the design of Flash ADC.

B. Power Gating Technique:

An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

Power gating affects design architecture more compared to the clock gating. It increases time delays as power gated modes have to be safely entered and exited. The possible amount of leakage power saving in such low power mode and the energy dissipation to enter and exit such mode introduces some architectural trade-offs. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations.

C. Operational -Amp

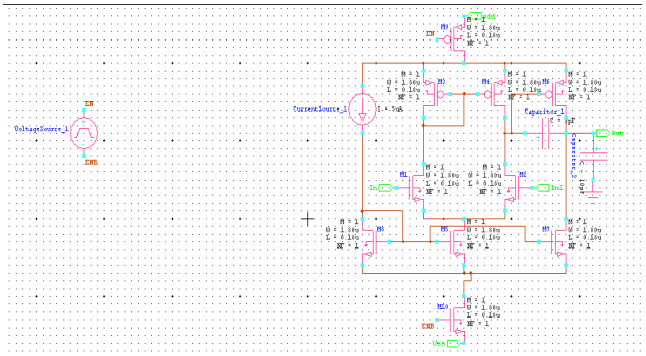

Figure 4: Modified Schematic of Op-Amp

In this modified architecture of operational Amplifier, two additional transistors are inserted at the connections of Vdd and Gnd in order to disrupt the path between supply to ground. These two transistors are considered as header transistor and footer transistor. These two transistors are driven by complementary enable gate signals. Due to complementary inputs, these two transistors operates under similar moments of enable signal.

D. MUX structure

The below figure represents the design of MUX using Pseudo NMOS Logic. In the Pseudo NMOS Logic, the gate of input of Pull Up transistors is grounded. The Pull-Down Network comprises the structure of respective behavior. Here, the Pull-Down Network consists of the design of MUX using only NMOS

Transistors. The output considered is the inverted of Pseudo NMOS node.

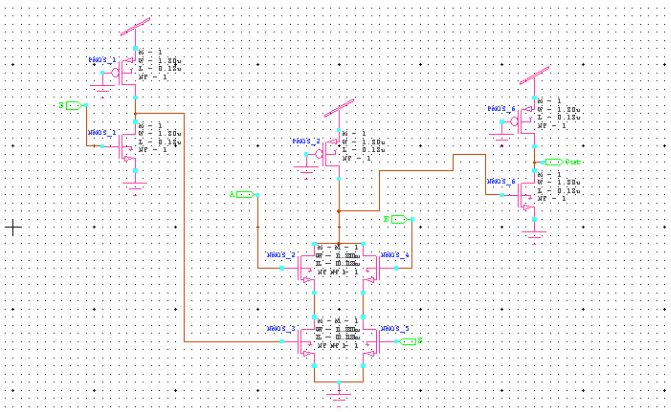

Figure 5: Modified Mux Structure

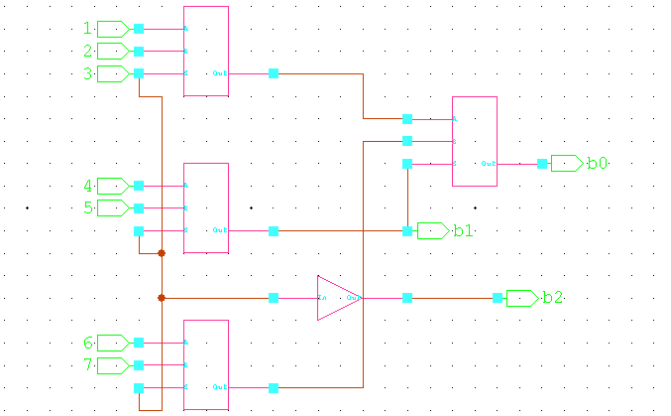

Figure 6: Mux based encoder

V. SIMULATION RESULTS

The entire work has been implemented using the back-end tool Tanner which is supported by Windows operating system. It works under 180nm with an operating frequency of 2.8GHz.

A. Existing System

The construction of MUX using Domino logic is just as same as that of the Pseudo NMOS logic. The only difference is that the PUN that has been grounded is supplied with a high clock skew which is provided by the Vpulse.

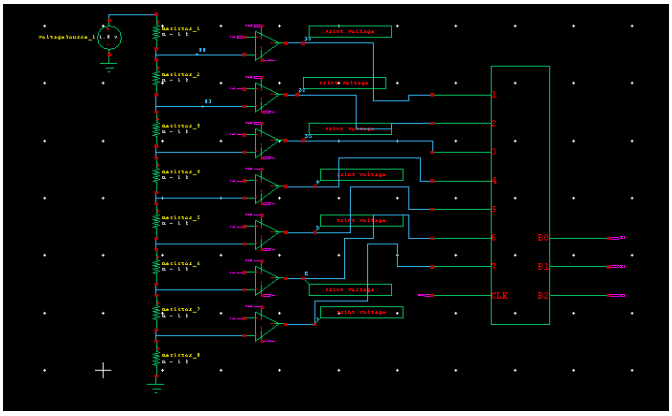

Figure 7: Schematic of flash ADC using Domino Logic

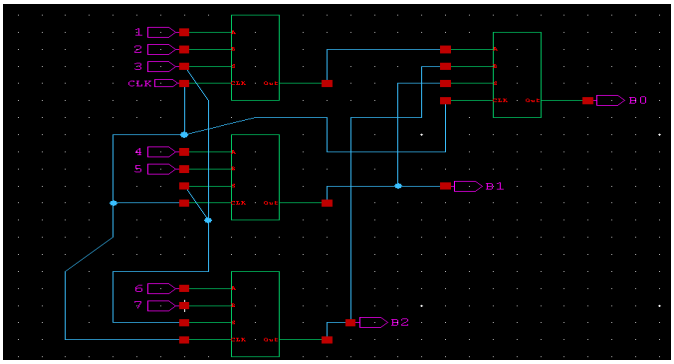

Figure 8: Mux based encoder using domino Logic

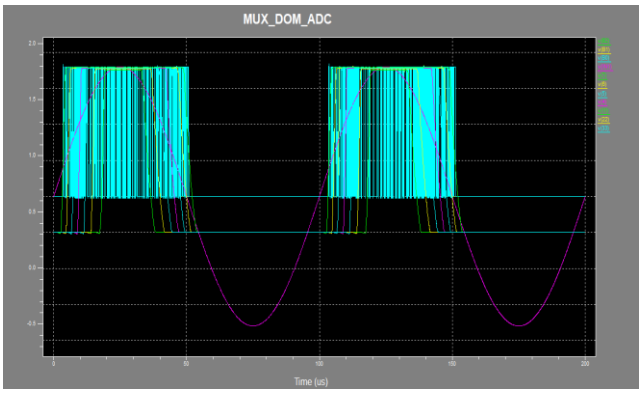

Figure 9: Output wave form

The output is connected to a CMOS inverter to overcome monotonicity problem and to improve the circuit performance as shown in the Fig.8. VDD is used to provide the power supply to the circuit connected to the pull-up circuit and the other inputs provided through Vpulse. The output waveform of the Domino logic is shown in Fig.9.

B.Proposed System

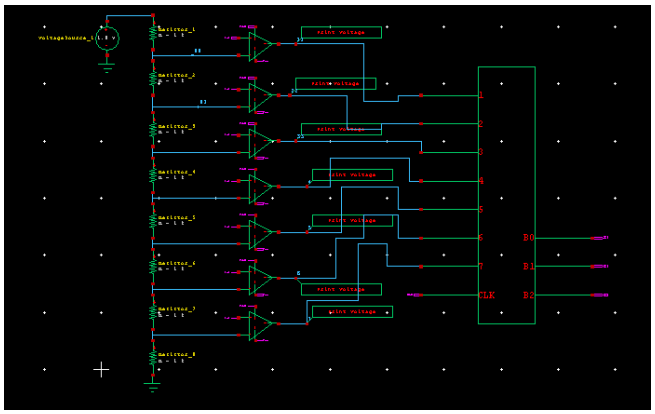

Figure 10: Schematic of flash ADC using Pseudo Logic

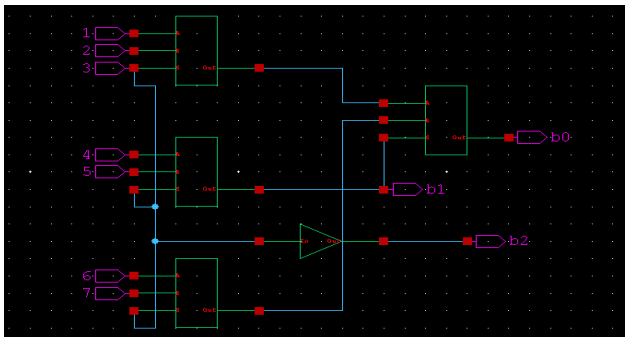

Figure 11: Mux based encoder using Pseudo Logic

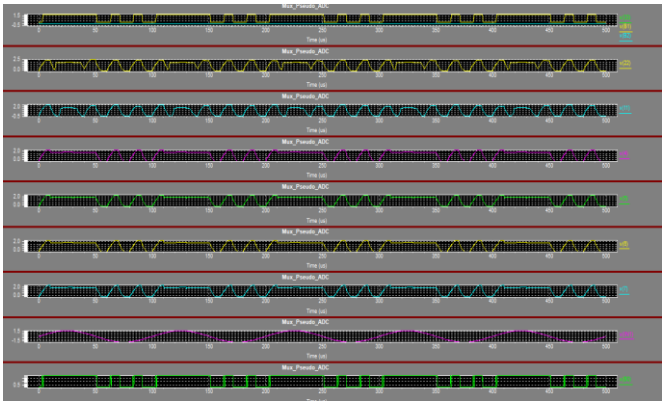

Figure 12: Output waveforms of flash ADC.

The design of 2:1 MUX using Pseudo NMOS logic by a single pMOS transistor and grounded permanently to reduce the transistor count. The output of the Pseudo NMOS is connected to an inverter to obtain the correct output as shown in Fig.6 and its test bench waveform is shown in Fig.11. The power supply is provided through VDD connected to the pullup circuit and the circuit inputs are given with the help of Vpulse as per the truth table of 2:1 MUX. The output waveform of the Domino logic is shown in Fig.12.

C. Performance Metrics

In this work the optimum design of MUX is identified experimentally by comparing the various performance metrics such as average power, static power, dynamic power and propagation delay.

a. **Average Power:** It is characterized as the power consumed by the circuit so as to give the output. By reducing the power supply from the circuit automatically the power consumed by the circuit will be reduced.

$$Average\ power = Static\ power + Dynamic\ Power$$

b. **Propagation delay:** It is the time required for a digital signal to travel from the input of a logic gate to the output switch.

$$Delay = \frac{T(rf)+T(fr)}{2}$$

Where, is the rise time, is the fall time

C. **Area:** It is the product of length, width and the number of transistors used to implement a circuit. It gives the amount of silicon area needed to implement a circuit. Unit: square meter (m2)

$$Area = L * W * (No.\ of\ transistors\ required)$$

Where, L is the length, W is the width

3. Comparison Table

TABLE I

COMPARISON OF DOMINO AND PSEUDO LOGIC

S. No	Domino MUX	Pseudo MUX
Power (W)	1.942×10^{-4}	8.7468×10^{-5}
Area	96	110
Delay (s)	2.613μs	0.502μs

Flash ADC implemented utilizing encoder with 2:1 mux in Pseudo NMOS and power gated op-amp logic offers less delay as well as less power consumption.

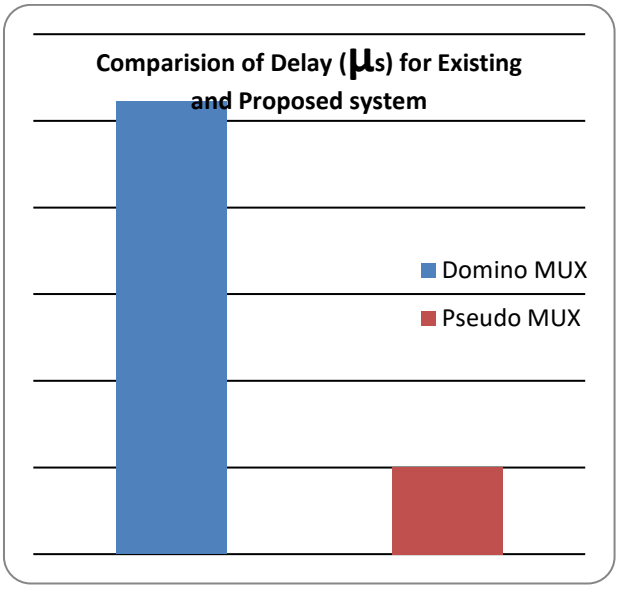

Figure 13: Delay Analysis of Domino and Pseudo Logic

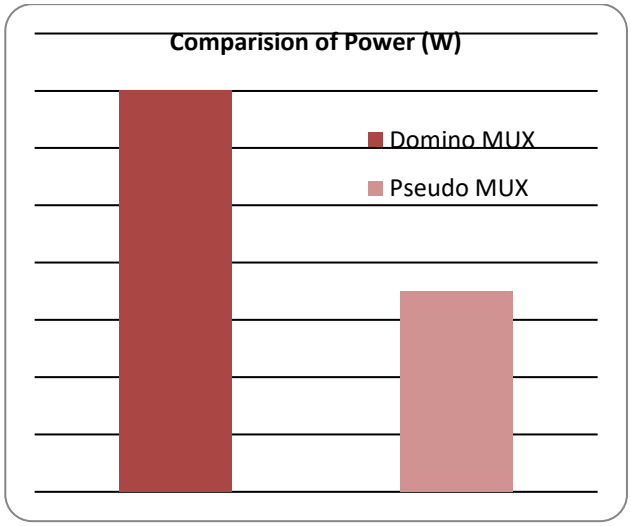

Figure 14: Power Analysis of Domino and Pseudo Logic

VI. CONCLUSION

In this paper, we have implemented flash ADC using novel architecture. Here, presented the design of op-amp is based on Power Gating Technique and the structure of MUX is based on the Psedo NMOS Logic. Design and simulation of 3-bit flash ADC are carried out using the Tanner tool employing 180nm technology model files. Parameters such as conversion time, the average power of 3-bit flash ADC are calculated and compared. Mainly we focused to reduce the propagation delay of 3-bit flash ADC by optimizing the encoder circuitry. We have implemented a 2:1 mux-based encoder employing Pseudo NMOS logic. 3-bit Flash ADC implemented utilizing encoder with 2:1 mux in Pseudo NMOS and power gated op-amp logic offers less delay as well as less power consumption.

Future works

In feature the proposed work can be extended to 4-bit Flash ADC.

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