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Design of an Efficient Low Power and High Performance Ternary Content Addressable Memory (TCAM) using 45nm

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ABSTRACT

In today's computing systems, memory has become a crucial resource. In the overall architecture of different computing systems, memory speed continues to be a bottleneck. To reduce memory access times, parallel search operations using CAM architecture are frequently used. To retrieve actual data from memory, the Ternary Content Addressable Memory (TCAM) subsystem contains a search operation via content addressing in the planned look-up table. Although the TCAM design's performance has improved noticeably over the years, there is still room for power exploitation.An innovative, performance-safe, and energy-efficient, binary and ternary CAM memory cells are proposed and put into practice. In this case, we're using the lector approach, one of the low-power design methods, to create both the and gate and the inverter that go into the CAM cell. CMOS technology is used to support the architectures of the AND gate and inverter. Better outcomes for characteristics like power and latency are obtained when using the lector approach.Keywords - TCAM, CAM, CMOS, Precharge elimination, Memory subsystem, Memory design, Lector approach, Low power technique.
Keywords: CMOS, CAM

I. INTRODUCTION

Internet Protocol (IP) packet classification and forwarding in network routers stands as the predominant commercial application of Content-Addressable Memories (CAMs) today. As technological landscapes evolve, there is a noticeable trend towards centralized servers facilitating the connection of applications spanning from edge to cloud. This progression is amplified by the rapid advancements in artificial intelligence (AI), which is approaching levels of speed and precision akin to human cognitive processes. In response to the surge in connected devices and the exponential surge in

Internet traffic, contemporary systems face the imperative of executing swift searches with remarkable efficiency. This imperative has stemmed from the proliferation of Internet-enabled devices and the subsequent upsurge in online data transmission. In order to perform Internet Protocol (IP) forwarding or IP routing, routers—a crucial piece of networking hardware—need to receive data packets before deciding where to send them. In order to provide quick data packet routing, modern routers need to perform extremely quick lookups among massive volumes of data. Furthermore, completely associative cache controllers in CPUs, database engines, and neural networks, as well as translation look aside buffers (TLB), are applications that call for fast searches.

While there exist a multitude of methods for designers to undertake such searches, the utilization of content-addressable memories (CAMs) emerges as the optimal and efficient approach. CAMs employ a mechanism wherein they analyze search data in contrast to a pre-existing table of stored data and subsequently furnish the address of the matching dataset. Particularly in tasks demanding extensive search operations such as address lookup within Internet routers, data compression, and the acceleration of databases, CAMs are supplanting software counterparts. This transition is driven by the inherent swiftness of CAMs' search operations, outpacing the performance of their software-based alternatives. The implementation of this technique in hardware is known as CAMs. A list's linear search resembles a serial search in which the searcher goes over every position in memory and compares it to a key. In the realm of resources, a content-addressable memory (CAM)-based search stands as the pinnacle of efficiency. This mechanism entails simultaneous comparison against all stored contents, promptly yielding the address corresponding to the successful match. While the construction of CAM-based systems might pose greater complexity, their inherent design translates to significantly accelerated operations—a foundational characteristic that sets them apart.

The advantages in performance achieved through CAMs do, however, come hand in hand with certain drawbacks, notably increased size and higher power consumption, as illustrated in Figure 1. Unlike static RAM (SRAM) that relies on basic storage cells, a fully parallel CAM necessitates an independent comparison circuit for each memory bit. This requirement arises from the need for each memory bit to effectively discern a match between the input bit and the stored bit. In the context of CAMs, a comprehensive data word match signal is derived by merging the match outputs from all cells corresponding to the data word in question.

The CAM's physical size grows as a result of the extra circuitry. Since every entry is searched simultaneously, a sizable portion of the circuitry is active during a given cycle. So, reducing CAM power consumption, which rises in direct proportion to CAM configuration size, represents a significant challenge.

In today's world, mobile communication is quite significant. Numerous applications are being developed as a result of advancements in telecommunications technology, including video streaming, online gaming, navigation, etc., many of which call for high throughput, high data rates, and low communication latency. Fast packet routing and data searching are thus two essential needs for 4G/5G network routers. Data searches can be done quickly and in parallel using ternary content addressable memory (TCAM). The goal of quick routing can be easily attained by the routing table used with TCAM. Due to the high number of transistors employed, this desirable feature would however result in significant leakage power. Numerous methods have been suggested over the past ten years to lower TCAM leakage (static) power usage. Using dual-voltage architecture, optimizing SRAM structure, and dynamic power sources are some of the ways some of them lower leakage power. These techniques all

successfully lower TCAM's power usage, but when the power source or data signals are gated, the majority of them would corrupt any data that may have been stored. If the lost data needs to be recovered, external storage or control signals are needed. In order to recover these data, it would appear that the TCAM would need to use a lot of power and time. To decrease the leakage power consumption of TCAM, a novel TCAM design with data retention methodology, known as data retention based TCAM (DR-TCAM), is developed in this study. Each TCAM entry in our design is split up into several portions.

Internal mask cells in each segment are powered by the cells with the most and least significant bits (MSB and LSB), respectively. With the exception of the border segment, all segments would be deactivated due to the continuous nature of mask data to reduce leakage power usage. The mask data are still kept in low-leakage mode in DR-TCAM, in contrast to the earlier efforts [3-5], therefore no external control or TCAM rewriting behavior is required when the mask data need to be restored.

The speed of CAM lookup is substantially faster than that of software lookup due to content addressable memory (CAM)'s ability to compare the search data with all the stored data in simultaneously. Due to the need for quick table lookup in these and other applications that require it, such as translation look aside buffers, high associative caches, image processing, databases, and network routers, CAM is frequently utilized. Binary and ternary CAM (TCAM) are the two varieties of CAM. The main distinction between the two CAMs is that TCAM performs the wild match using an additional "don't care" ("X") state, making it uniquely suited to the longest prefix matching duty in network routers. But because TCAM uses parallel comparison and has a lot of transistors, it typically consumes a lot of power.

The proportion of leakage power (LP) to the overall TCAM power is anticipated to increase significantly as the technological feature size lowers, particularly for a large table size, because the TCAM dynamic power has been successfully lowered by a variety of ways [1]–[3]. In this article, we suggest a technology termed dynamic power source (DPS), which attempts to lessen the LP dissipated in the TCAM cell and is leakage-suppressed. The main concept behind the DPS technique is to destroy the prefix data to lower the LP when the TCAM cell state is "X." This is done by taking use of TCAM's special property that makes the prefix data redundant in the wild match.

Cisco switches use a unique form of memory known as CAM, or content addressable memory. When operating with conventional RAM, the Input/Output System (IOS) employs a specific memory address to fetch the data stored at that particular location within the memory module. In contrast, the dynamic shifts when dealing with Content-Addressable Memory (CAM). Here, the IOS takes advantage of the actual data itself, prompting the CAM to promptly furnish the corresponding memory address where the sought-after data is stored. Notably, the CAM's distinctive capability to perform simultaneous searches across every memory bit confers it with the reputation of being inherently faster in comparison to RAM. This acceleration stems from the CAM's ability to undertake exhaustive searches spanning the entire memory in a singular operation, thereby augmenting its speed relative to traditional RAM setups.

The only outcomes offered by CAM tables are 0 (true) and 1 (false). Building exact match searchable tables, like MAC address tables, is where CAM is most helpful. Decisions on Layer 2 forwarding are typically made using the CAM table.

Layer 2 switching tables demand a precise correspondence with the destination MAC address to avert the undesired flooding of packets across all ports within the VLAN. In order to establish this preventive measure, the database responsible for Layer 2 switching tables is constructed by incorporating the source address and the incoming port of every individual frame.As frames traverse switch ports, their respective source MAC addresses

are identified and subsequently stored within the CAM table. This progression unfolds in real-time as frames arrive on switch ports. Notably, the CAM table encompasses a timestamp alongside comprehensive details such as the associated VLAN and the port of initial arrival. This amalgamation of data serves to facilitate efficient and accurate Layer 2 switching operations, mitigating the risk of unnecessary packet flooding.

In scenarios where a MAC address previously learned on a specific switch port has been shifted to another port, the MAC address itself and its corresponding timestamp are recorded. This practice supersedes the prior entry related to the MAC address. Alterations solely affect the timestamp when the MAC address already resides in the table under the correct arrival port.

Upon the arrival of a frame at the switch, bearing a destination MAC address corresponding to an entry within the CAM table, the frame is exclusively forwarded via the port linked to that specific MAC address. This ensures targeted and efficient data transmission.

At the core of this process lies the concept of a "key" — the crucial piece of information that empowers a switch to execute a lookup within the CAM table. For instance, in the context of a Layer 2 lookup, this "key" encompasses both the destination MAC address and the VLAN ID. This combination of key elements is pivotal in orchestrating effective Layer 2 operations.

Ternary Content Addressable Memory (TCAM), which can match any value as a third state, goes by the name TCAM. Due to their ability to store their routing tables in TCAMs, which enables for extremely quick lookups and is far better than routing tables kept in regular RAM, Cisco Layer 3 switches and current routers use TCAM as a very key component. Fast table lookups are the focus of the specialized CAM known as TCAM. There are three outcomes offered by TCAM: 0, 1, and "don't care." The true utility of Ternary Content-Addressable Memory (TCAM) comes to the fore when constructing databases tailored for longest match searches. This is especially evident in scenarios involving IP routing tables organized based on IP prefixes. Within this context, TCAM stands as an invaluable resource. The TCAM table assumes the responsibility of storing data predominantly associated with upper-layer processing functionalities. This encompasses a spectrum of functions ranging from Access Control Lists (ACL) to Quality of Service (QoS) specifications and other pertinent data points. TCAM's unique characteristics make it a pivotal tool in optimizing these complex networking operations.

Applying ACLs has no impact on the switch's performance because TCAM is used. A prevalent characteristic among most switches is the incorporation of multiple Ternary Content-Addressable Memories (TCAMs). This strategic design empowers the switches to undertake Layer 2 or Layer 3 forwarding determinations seamlessly, even as they conduct simultaneous reviews of inbound and outbound security measures, as well as Quality of Service (QoS) Access Control Lists (ACLs). This parallel processing capability greatly enhances the efficiency of network operations.

Within the TCAM structure, the entries are formatted in what is known as VMR—Value, Mask, and Result. This format encapsulates the key components necessary for precise pattern matching. Notably, various patterns such as IP addresses, protocol ports, and Differentiated Services Code Point (DSCP) values are among those that can be effectively matched using the "value" component within the VMR structure. This distinctive setup renders TCAM an indispensable tool for achieving accurate and efficient networking functionalities.

The "mask" is the term used to describe the mask bits connected to the pattern and establishes the prefix. If a lookup yields a match for the pattern and mask, the "result" denotes the outcome or action that transpires in that situation. In the realm of TCAM applications, the resulting outcome is diverse, tailored to the specific context in which it is employed. For instance,

within the domain of Access Control List (ACL) TCAMs, the outcome might manifest as either a "permit" or "deny" decision, serving as a determinant for access permission. In the context of Quality of Service (QoS), the outcome could manifest as values corresponding to QoS rules, contributing to traffic prioritization. Additionally, in scenarios involving IP routing TCAMs, the outcome might entail a pointer directing to a particular entry within the hardware adjacency database. This entry, in turn, contains vital information pertaining to next-hop MAC rewriting data, pivotal for effective IP routing. The diverse and contextual outcomes achieved through TCAMs underscore their versatility in enhancing various networking functionalities.

With packet classification, which compares a number of pertinent packet header fields against a set of forwarding rules and performs the necessary actions in response to a rule match, modern network routers and switches impose policy-based forwarding. The bottleneck of advanced forwarding, packet classification, has drawn study interest for a long time [1]. Multi-field packet categorization at line speed is still a difficult challenge, despite substantial research on algorithmic solutions. Ternary Content Addressable Memory (TCAM) is frequently used in industry because it allows for concurrent lookups against all the rules to get the best match in a single pass. But in addition to being pricey, this technology for brute force consumes a lot of power. The cost and power consumption of TCAMs have been the subject of extensive research, which has included both architectural and algorithmic approaches. The TCAM device is organized into discrete, unchanging blocks of fixed sizes. As required, a specific subset of these blocks can be activated to perform lookups.

Block-based TCAM designs are already available from top TCAM providers. With this improved architecture, prospective power reductions have a solid foundation. The issue is how to set up the TCAM's rules so that each incoming packet can only be classified according to a few TCAM blocks.

Access to stored data is made possible by contents (data words), not addresses, and Ternary Content-Addressable Memory (TCAM) outputs the match address. To ascertain the presence of a particular data word within CAM memory, the Content-Addressable Memory (CAM) conducts a comprehensive scan across every memory bit simultaneously. This scan is executed concurrently, assessing every bit of memory to determine if the data word is stored. Upon completion of the scan, CAM generates a list comprising one or more storage addresses where the specific word was identified.

The prime incentive for adopting a CAM lies in its remarkable capacity for swift searches. While it's theoretically possible to perform the search function using conventional random-access memory (RAM) by repetitively reading and comparing each RAM entry, CAM's inherent architecture greatly expedites this process, rendering it significantly faster and more efficient. As a result, for the same search request, the RAM search time takes far longer than the CAM search time.

For applications needing high-speed search, like local-area networks, database management, pattern recognition, and artificial intelligence, CAM is a desirable option due to its high-speed search function. Contemporary applications of content-addressable memory (CAM) encompass real-time pattern matching in virus detection and intrusion detection systems, gene pattern searching in bioinformatics, data compression, and image processing, to name a few. Notably, in the realm of virus and intrusion detection systems, CAM facilitates instantaneous pattern recognition. Similarly, in bioinformatics, the capacity to search for specific gene patterns is expedited through CAM technology. Moreover, CAM is leveraged for data compression and enhancing picture processing

techniques, where its capabilities are employed to streamline these processes.

A distinctive type of CAM known as a Ternary Content Addressable Memory (TCAM) stands out due to its fully associative nature. This specialized form of CAM seamlessly executes lookup-table functions with the assistance of dedicated comparison circuitry, often performing these operations within a single clock cycle. This swiftness and efficiency make TCAM a pivotal component for rapid pattern matching and data retrieval in various applications.

The entered search data is compared to a table of previously recorded information, and the address of any matched information is then returned. '1', '0', and '2' are the three states that are stored in the memory cell of a TCAM. When matching to a '0' or '1' in the input search data process, the additional state '2'—also known as the "mask" or "don't care" state—is used. TCAM finds its specialized role in performing particular application tasks, notably excelling in functions like longest prefix matching within network search engines. Additionally, TCAM demonstrates its utility in applications requiring support for both exact and partial matches. This adaptability showcases TCAM's effectiveness in accommodating a range of search scenarios, further underscoring its significance in networking and pattern recognition domains.

Although chip designers typically aim to lower these design parameters at the nonmetric scales, the use of a TCAM comes at the expense of higher area and power consumption. Additionally, an ever-increasing number of applications necessitate TCAMs of ever-larger sizes, significantly escalating power usage.Content-Addressable Memory (CAM) operates by comparing input search data against a stored data table and promptly furnishing the corresponding address of the matching data. In contrast to alternative hardware- and software-based search systems, CAMs stand out with their exceptional throughput, performing these operations within a mere single clock cycle. This instantaneous processing capability underscores CAMs' efficiency and suitability for rapid data retrieval and matching tasks. Applications requiring quick searches across a wide range of fields can employ CAMs. Programmers employ various techniques such as Lempel-Ziv compression, image coding, Huffman coding and decoding, parametric curve extraction, and Hough transformation to optimize data processing. In contemporary times, the predominant commercial application of Content-Addressable Memories (CAMs) revolves around Internet protocol (IP) packet classification and forwarding functions in network routers.

The process of transmitting messages, such as emails or web pages, across networks like the Internet involves breaking down the message into smaller data packets, each containing a few hundred bytes. These individual data packets are then transmitted independently through the network. Upon reaching their destination, the packets are reassembled to reconstruct the original message. This transmission and reassembly procedure necessitates the routing of these packets from the source through intermediate nodes, commonly referred to as routers, within the network.

A router's job is to determine the best route by comparing a packet's destination address to all other potential routes. Due to its quick search capabilities, a CAM makes a viable choice for implementing this lookup procedure.

II.EARLIER WORK

TCAM, short for "Ternary Content-Addressable Memory," represents a specialized form of memory with distinct applications in the realms of computer networking and digital systems. It has been

ingeniously crafted to excel in high-speed table lookups, rendering it particularly advantageous in scenarios such as routing and packet forwarding within network devices like routers and switches.

While conventional memory types like RAM necessitate an address for data retrieval, the unique feature of CAM lies in its ability to perform data searches based on content. In simpler terms, instead of providing an address, you input the data you seek, and CAM furnishes the precise address where that data is stored. What distinguishes TCAM from standard CAM is its capability to execute ternary (three-state) search operations. Unlike traditional binary CAM that allows exact matches only, TCAM expands this scope to include partial or exact matches, enhancing its versatility in various applications.

In a ternary CAM, you can search for an exact match, a mismatch, or a "don't care" condition for certain bits in the search key.

TCAM is widely used in networking for tasks such as IP routing and access control list (ACL) matching. In IP routing, for example, a router uses TCAM to quickly determine the next hop for an incoming packet based on its destination IP address. TCAM allows routers to perform complex pattern matching and route lookups in a single clock cycle, which is crucial for maintaining high network speeds.

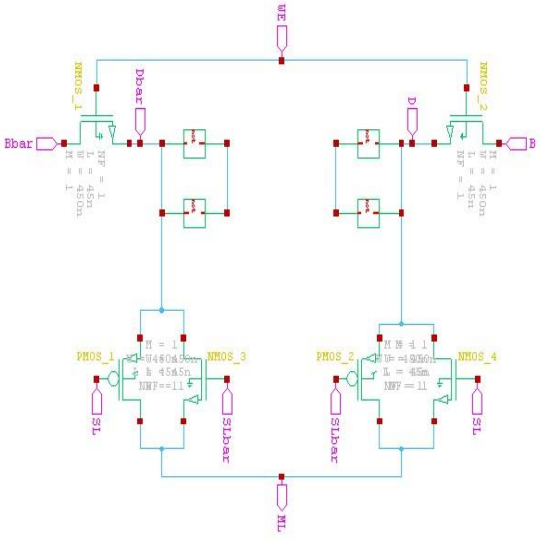

Fig 1 : TCAM ARCHITECTURE:

The internal structure of TCAM includes inverter terminals. These inverter terminals are connected to the end of NMOS terminal. Below shows the schematic of the CMOS inverter.

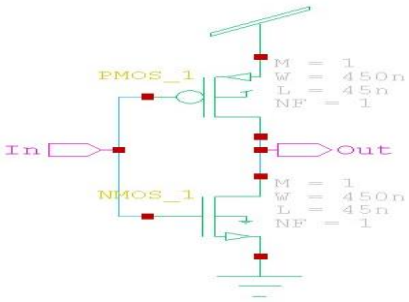

Fig 2: CMOS inverter

The inverter cell and TCAM designs are converted to the symbols to design 2-TCAM, 4-TCAM, 8-TCAM, and 16-TCAM.

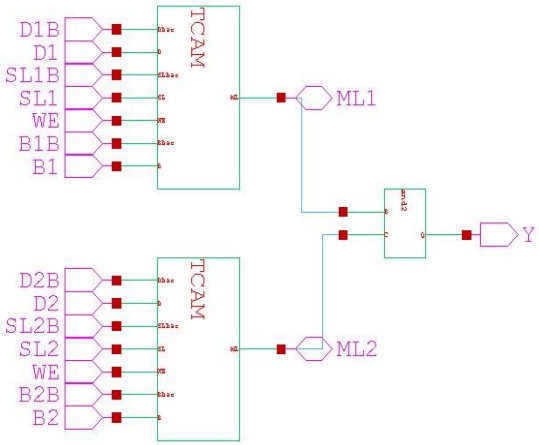

Fig 3: 2 bit-TCAM

In the design of 2bit-TCAM we are using 2-TCAM symbols and one 2-input and gate. The outputs of TCAM are connected to the And gate and it provides the required output.

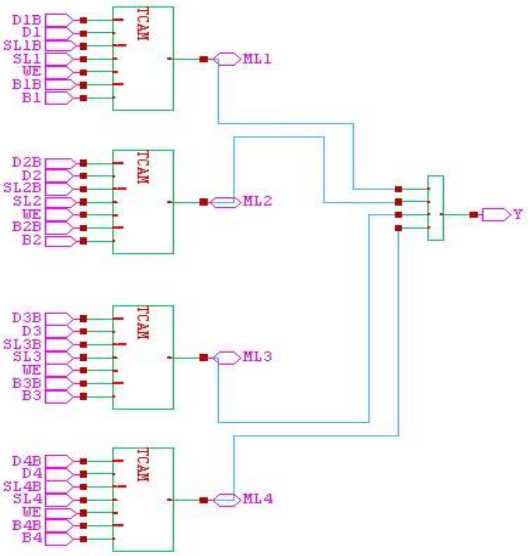

Fig 4: 4bit-TCAM

In the design of 4bit-TCAM we are using 4-TCAM symbols and one 4-input and gate. The outputs of TCAM are connected to the And gate and it provides the required output.

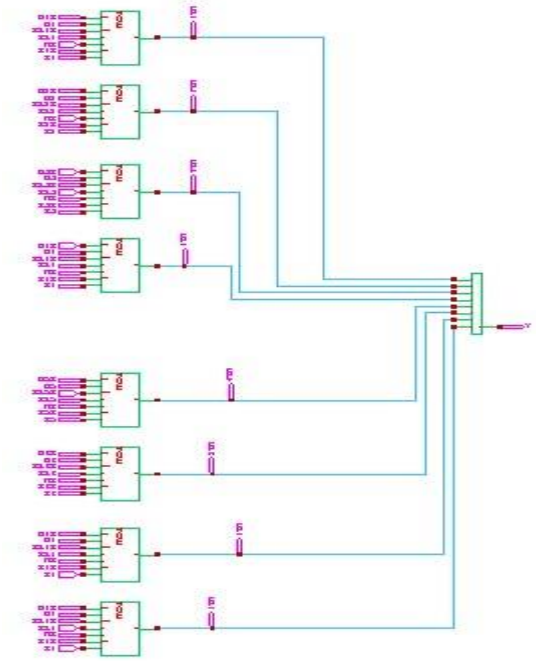

Fig 5: 8bit-TCAM

In the design of 8bit-TCAM we are using 8-TCAM symbols and one 8-input and gate. The outputs of TCAM are connected to the And gate and it provides the required output.

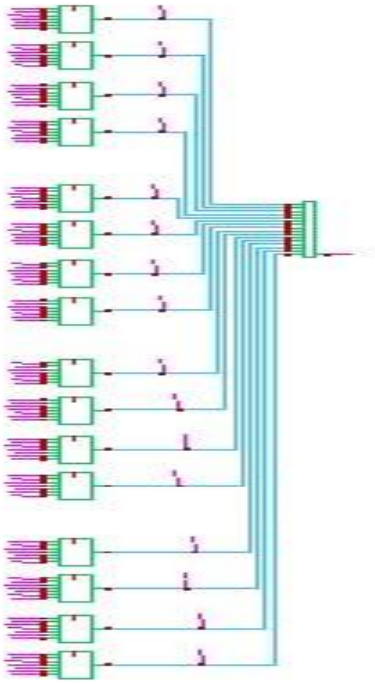

Fig 6: 16bit-TCAM

In the design of 16bit-TCAM we are using 16-TCAM symbols and one 16-input and gate. The outputs of TCAM are connected to the And gate and it provides the required output.

TCAM with sensing circuit:

To cut down on energy use or improve the latency of the search operation of TCAM designs, a number of sensing systems have been put forth. Match lines (ML) are frequently precharged highly in conventional sensing techniques. Only the rows with perfect matches stay high during the evaluation phase, while the rows with imperfect matches stay low. The TCAM either evaluates to a mismatch state or to a full match state (fm), when all of its cells match the input bits. Here, the terms ML pre and MLSA stand for Match-Line Sensing Amplifier and NOR type TCAM cell, respectively, indicating that the Match-Line is precharged.

Purpose of Sensing:

Storage reliability and Sensing speed are the two key factors that affect content addressable memory performance. Due to frequent switching during search, the majority of power loss in a CAM is connected to the search line and Match-Line. It is done to compare the power usage and performance of different sensing techniques. In order to conserve energy, these sensing techniques typically reduce the ML voltage swing or supply voltage. The time for assessment is a crucial factor in determining the search speed in ternary content addressable memory (TCAMs), where sensing is typically done by match-lines. The ML power consumption can be decreased by using effective ML sensing techniques.

There is typically a voltage drop in both the match and mismatch situation when a search operation is carried out in conventional higher order TCAMs [20]. Sensing methods are therefore suggested in order to increase the Match-Line (ML) voltage in a match instance. Capacitive Match-Line Sensing is used in this instance in place of the conventional method. By using this Match-Line Sensing approach, the TCAM uses less power while improving the match voltage. A

resistive ML sensing technique is suggested in order to decrease power consumption and increase ML voltage.

Operation of Capacitive Sensing with TCAM Circuit:

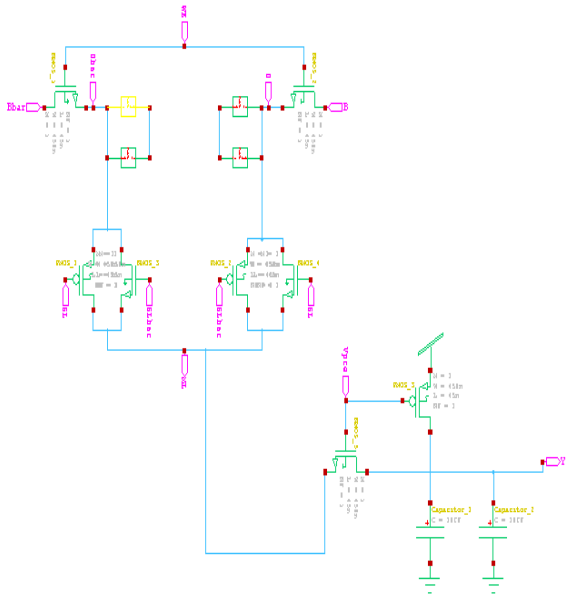

Figure 7: TCAM Cell with Capacitive Sensing Circuit

In the illustrated diagram, a TCAM cell of the AND type is interconnected with a capacitive sensing circuit. Based on the preceding description, two distinct scenarios emerge—the match case and the mismatch case. To effectively differentiate between these match and mismatch conditions within the capacitive sensing mechanism, a capacitor is employed. This capacitance-based component plays a pivotal role in accurately identifying and distinguishing the varying states, thus contributing to the precise functioning of the TCAM cell. Precharge and evaluation phases are both present.

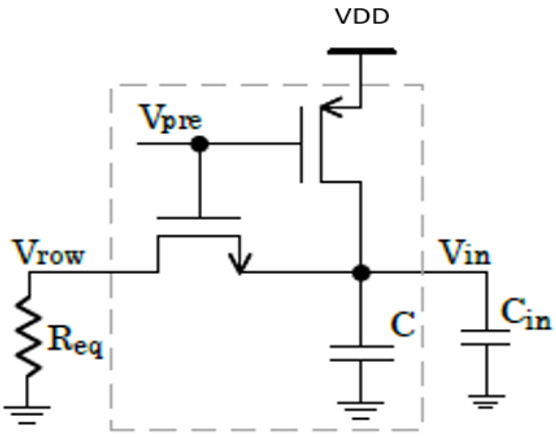

Figure 8: Capacitive Sensing circuit

Both match and mismatch instances result in charging of the capacitor C during the precharge phase. However, ML discharges through a resistor equivalent to the effective resistance of the TCAM row of cells during the mismatch case evaluation phase, whereas ML is maintained at a high level in the match case. For evaluation in a match or mismatch instance, the voltage at ML is employed. The capacitor discharges gradually when the conditions are right, and quickly to ground when they are wrong [21].

Consequently, in the match case, the introduction of a TCAM cell with a capacitive sensing circuit leads to an elevation in the Match-Line voltage. However, this enhancement in voltage comes at the expense of increased power consumption. To mitigate this power overhead and concurrently amplify the Match-Line voltage, a resistive Match-Line sensing system is employed. This alternative sensing approach serves to efficiently manage power usage while still achieving elevated Match-Line voltages compared to the conventional sensing scheme.

Resistive ML Sensing:

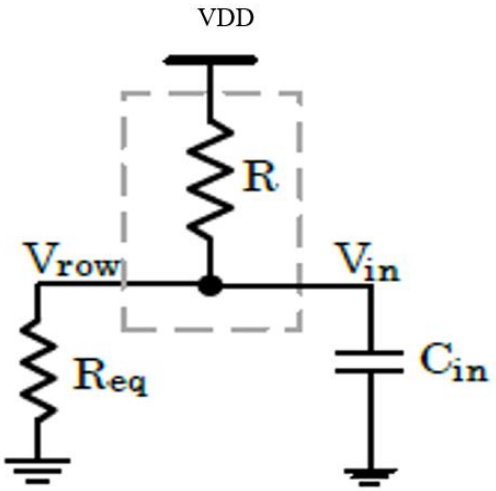

Figure 9: Resistive Sensing circuit

Figure 9 illustrates a resistive sensing circuit. As demonstrated in Figure, the TCAM's voltage is divided by a resistor in this resistive sensing method. As a voltage divider across the equivalent resistor of the TCAM row of cells, the voltage that separates the mis-match states from the match states is therefore shown. This method of resistive sensing does not use a

precharge transistor. As a result, only an assessment step is required in order to compare the various states; no precharge phase is required. The cycles of match and mismatch are taken into consideration. Only the evaluation phase is included in each cycle under this arrangement. A good voltage drop differential between the match and mismatch states is maintained while this design assesses significantly more quickly. Also, this design consumes less power than the conventional Match-Line Sensing scheme.

Operation of Resistive Sensing TCAM Circuit:

The circuit for resistive sensing, which is coupled to a TCAM cell of the AND type, is shown in Figure. There are two possible scenarios for each content accessible memory. Both are mismatch cases, with one being a match case. Any content addressable memory search operation is conducted in two stages. The first is the precharge phase, and the second is the evaluation phase. With the aid of precharge transistor ML, this precharge phase is charged to a high level. Contrarily, during the evaluation stage, it is determined whether a match case or a mismatch case exists based on the Match-Line voltage. However, the precharge phase is not required in this resistive sensing technique.

The resistive sensing circuit depicted in Figure 10 distinctly omits a precharge transistor. In this configuration, solely the evaluation phase is requisite to access both match and mismatch states. In the event of a mismatch, the Match-Line discharges via a resistor equivalent to the effective resistance of the TCAM row of cells. Conversely, in the evaluation phase of a match case, the Match-Line maintains a high voltage.

The determination of whether a match or mismatch is present relies on the voltage of the Match-Line, as indicated [22]. In this resistive sensing approach, the voltage divider mechanism for the TCAM is realized through a resistor. Acting as a voltage divider spanning the TCAM cells' equivalent resistor, the voltage level demarcating the mismatch states from the match states is thereby illustrated. This distinctive setup enables the identification and differentiation between match and mismatch scenarios within the TCAM system.

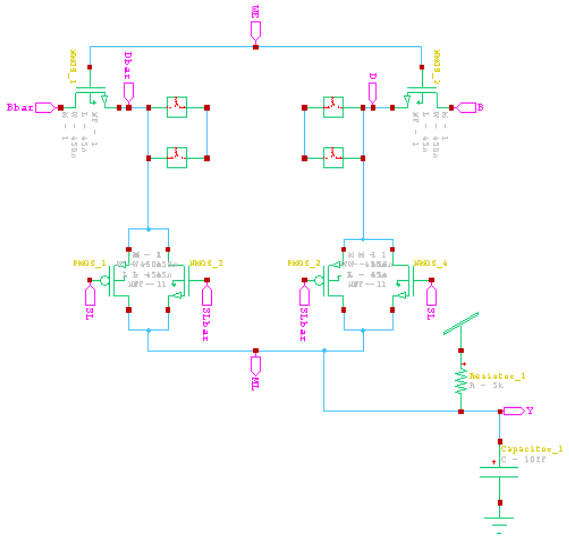

Figure 10: TCAM Cell with Resistive Sensing Circuit

Incorporating the resistive sensing circuit yields an augmented voltage level at the Match-Line in comparison to the conventional Match-Line sensing approach. In instances of a mismatch, the Match-Line voltage experiences a more rapid decrease compared to the traditional capacitive Match-Line sensing method.

Notably, capacitive sensing employs a precharge transistor to initialize its configuration, whereas resistive sensing does not necessitate this component. As a result, capacitive sensing encompasses two distinct phases: precharge and evaluation. Conversely, in the domain of resistive sensing, it is unequivocally evident that this design offers considerably swifter assessment, while simultaneously maintaining a substantial voltage drop discrepancy between the fully matched and mismatched states. This attributes to the efficiency and differentiation capabilities of resistive sensing in comparison to capacitive sensing.

It also consumes significantly less power. Comparatively speaking, the capacitive sensing design requires nanoseconds to evaluate all three states, whereas the resistive sensing design requires picoseconds. All this capacitive and resistive sensing are applied for 2-TCAM, 4-TCAM, 8-TCAM, and 16-

TCAM to reduce the power dissipation and maintain storage stability and sensing speed.

III. PROPOSED WORK

There are only a few small changes made to the current system in this area. The CMOS technology and lector method are both used to support the structure of the AND gate. Lector methodology is one of the Low power approaches. Additionally, when designing the inverter utilized in CAM cells, we applied the Lector technique. There are several low power approaches, including transistor stacking, clock gating, and power gating, to obtain low power. Leakage currents in the MOSFET device are mostly to blame for this situation's static power usage. It happens as a result of an undesirable current (sub threshold current) flowing through the transistor's channel even when the transistor is off. The transistors in the circuits' threshold voltages are significantly impacted by this. Many power gating solutions have been developed by academics to lessen this flaw.

The AND gate and NOT gate that we developed in this paper employ a novel lector method. Power gating strategies include the Lector approach as one of the methods. By cutting off the electricity to the circuit, this method allows us to reduce power consumption.

Basic Lector Approach:

By placing two leakage control transistors in the midst of pull-down and pull-up channels, the LECTOR method effectively reduces leakage power. Due to the fact that the NMOS transistor's source controls the PMOS transistor's gate and the PMOS leakage transistor's source terminal controls the NMOS leakage transistor's gate terminal, these leakage transistors don't need any external control circuitry. In contrast to NMOS, whose substrate is connected to GND, PMOS's is connected to power supply VDD. Out of the two leakage transistors, one is constantly operating close to the cutoff zone due to the placement of the transistors.

It operates on the idea of stacking, where more than one off transistors provide higher resistance than a single off transistor. As a result, leakage power is reduced as resistance increases. Nevertheless, the technique's disadvantage is increasing delay; as resistance rises, RC delay also rises. Here, the development of a reverse bias junction between the source and substrate results in a decrease in sub threshold leakage while simultaneously increasing latency.

The effective stacking of transistors in the circuit from supply voltage to ground is the fundamental concept underpinning our strategy for reducing leakage power. A state in which multiple transistors are switched off along a pathway from the supply voltage to the ground exhibits significantly lower leakage compared to a state where only one transistor is turned off along any pathway connecting the supply voltage to the ground.

In our approach, we add two leakage control transistors (LCTs) so that one of them is close to its cutoff area of operation in each CMOS gate.

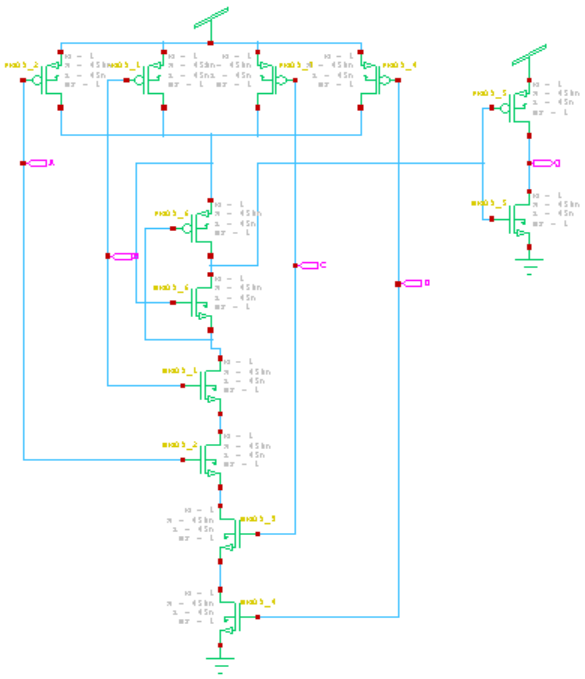

Fig 11: 4-input AND gate using Lector approach

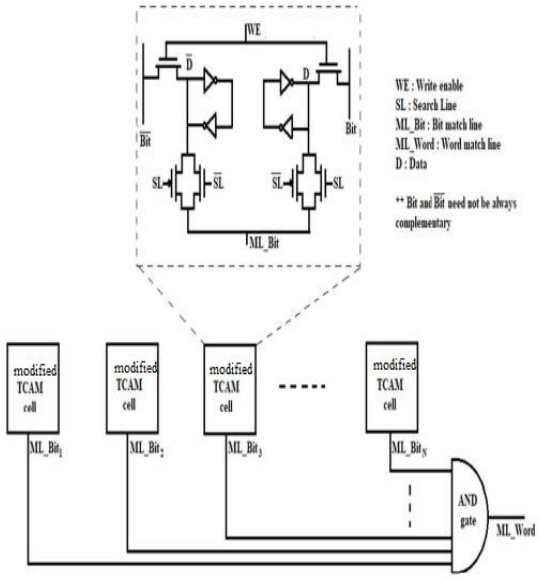

Fig 12: Proposed TCAM structure using modified inverter and AND gate.

Better power and delay results than the current TCAM structure are the primary goals of the suggested architecture. Because the Lector method was used to install LCT transistors. The Area will be larger than the current system. The number of transistors utilized in the design is used here to define the term "area."

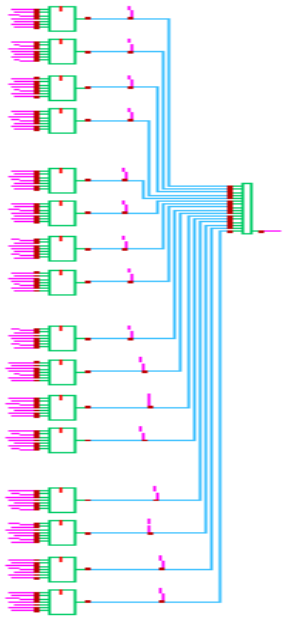

Fig 13: Proposed 16-bit TCAM structure using modified inverter and AND gate.

IV.EXPERIMENTAL RESULTS

The comparison of the proposed design is done for the TCAM using lector approach technique. Generally, the performance analysis of TCAM is based on certain parameters such as Power Consumption, Delay, and Stability and Area occupancy of the transistor. The performance comparison of the Conventional 2-bit, 4-bit, 8-bit and 16-bit TCAM, other existing techniques (capacitive sensing and resistive sensing) and the Proposed lector approach technique based modified TCAM transmission gate and sensing techniques also used in modified lector approach TCAM is done in CMOS 45-nm Technology.

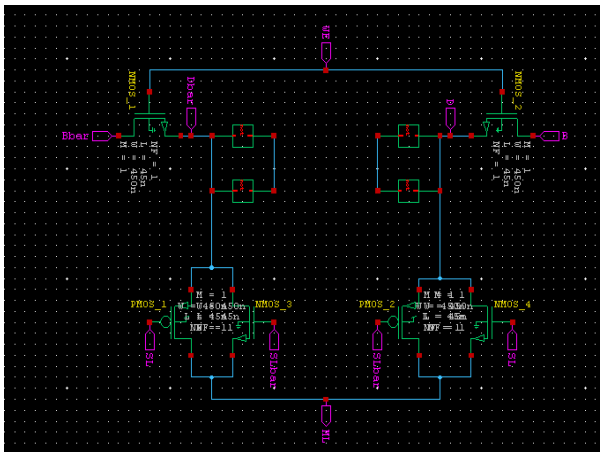

Fig14: Schematic of 1-bit TCAM

This schematic shows the modified 1-bit TCAM using AND gate lector approach.

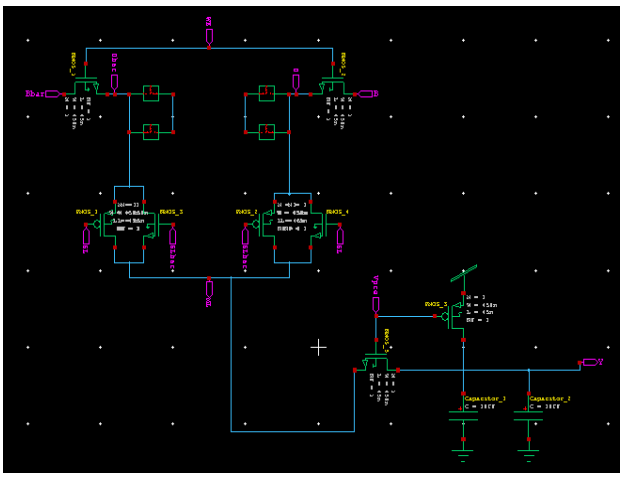

Fig15: Schematic of 1-bit TCAM using capacitive sensing

The provided diagram illustrates the adapted 1-bit TCAM configuration featuring capacitive sensing, employing an approach centered around the use of

AND gate logic.

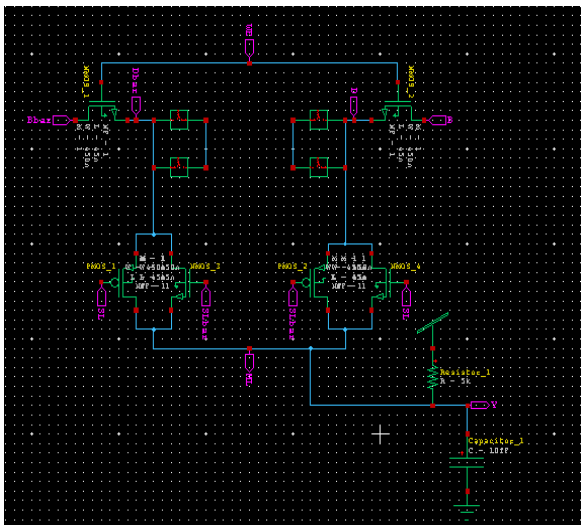

Fig16: Schematic of 1-bit TCAM using Resistive sensing

This diagram presents the revised 1-bit TCAM employing resistive sensing, employing an AND gate logic approach.

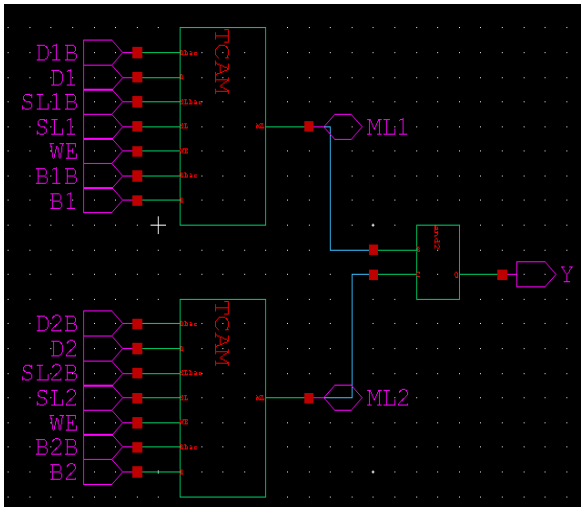

Fig17: Schematic of 2-bit TCAM

The provided diagram portrays the updated 2-bit TCAM design, utilizing an AND gate logic approach.

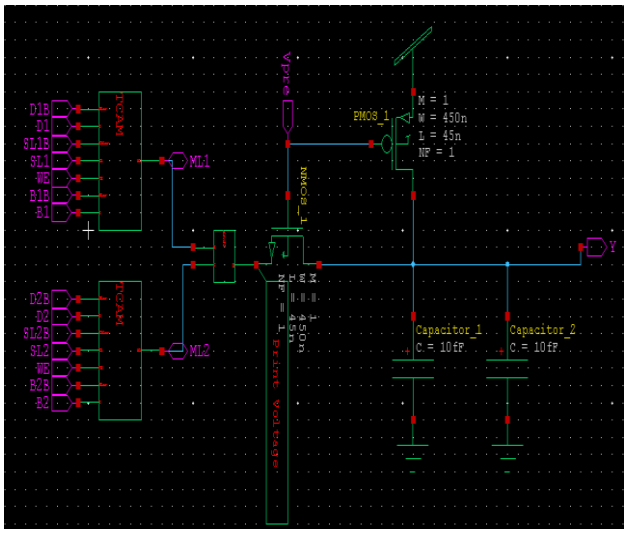

Fig18: Schematic of 2-bit TCAM using capacitive sensing

This schematic shows the modified 2-bit TCAM with capacitive sensing using AND gate lector approach.

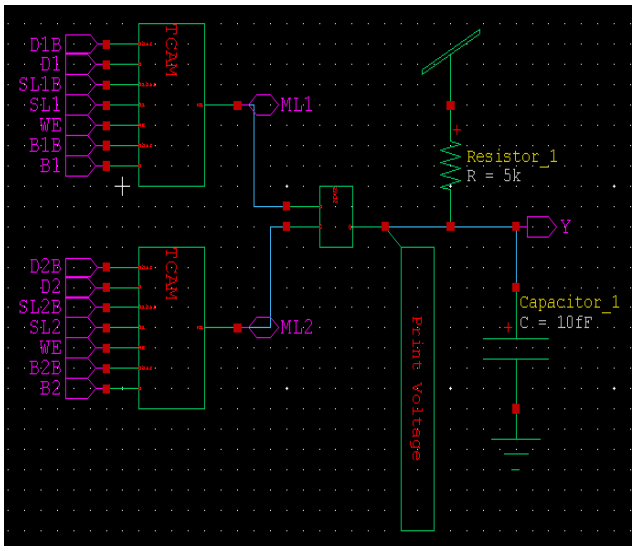

Fig19: Schematic of 2-bit TCAM using Resistive sensing

This schematic shows the modified 2-bit TCAM with Resistive sensing using AND gate lector approach.

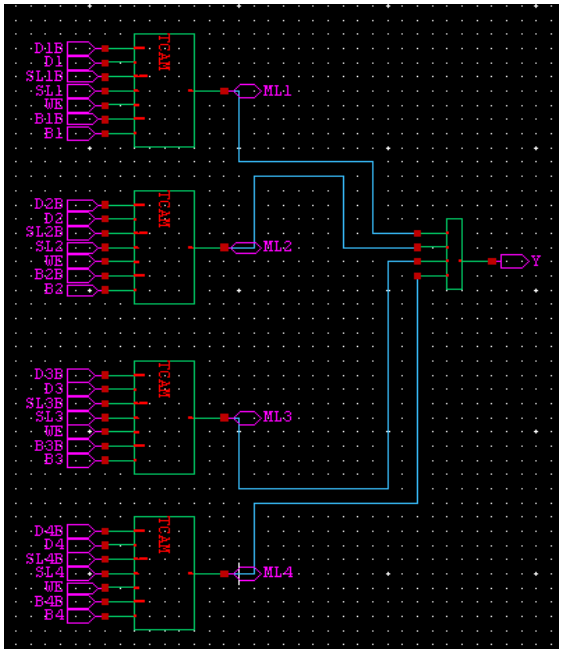

Fig20: The schematic diagram of a 4-bit TCAM.

This schematic shows the modified 4-bit TCAM using AND gate lector approach.

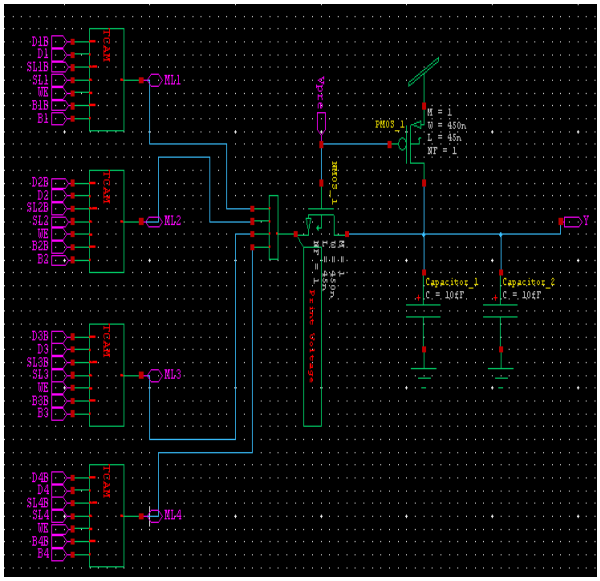

Fig21: Schematic of 4-bit TCAM using capacitive sensing

This schematic shows the modified 4-bit TCAM with capacitive sensing using AND gate lector approach.

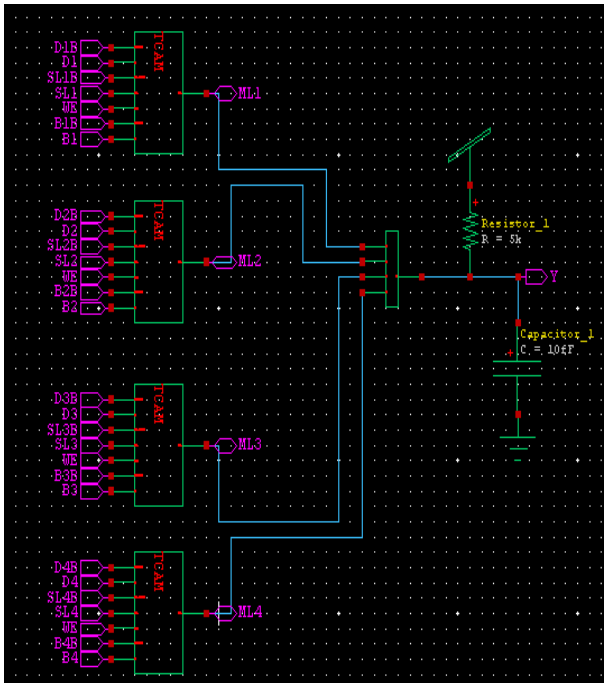

Fig22: Schematic of 4-bit TCAM using Resistive sensing

This schematic shows the modified 4-bit TCAM with Resistive sensing using AND gate lector approach.

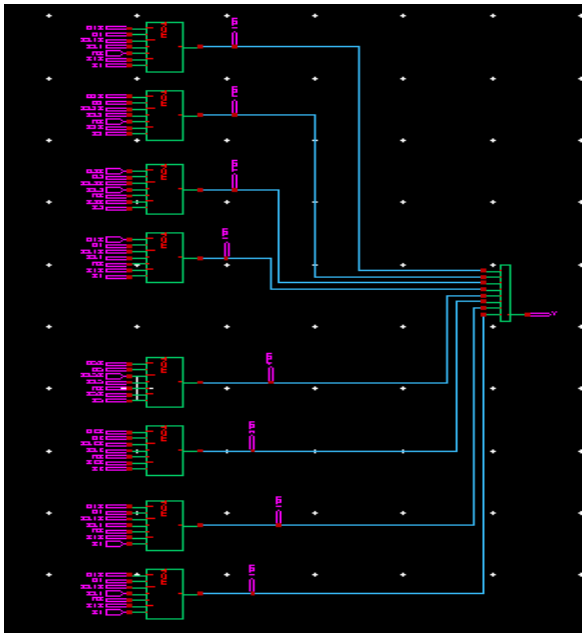

Fig23: Schematic of 8-bit TCAM

This schematic shows the modified 8-bit TCAM using AND gate lector approach.

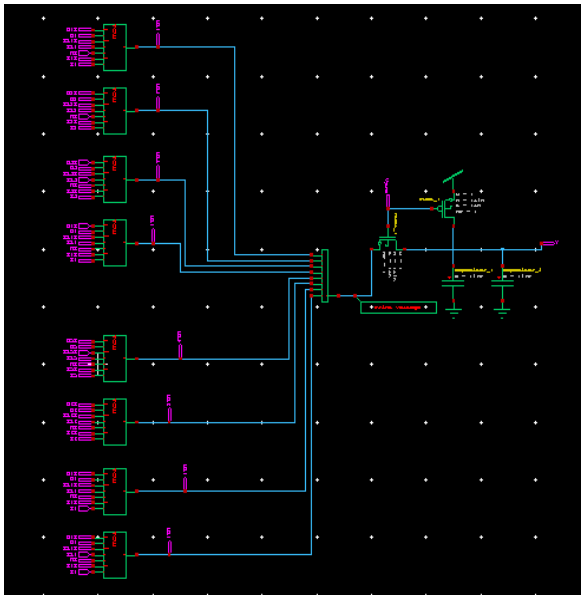

Fig24: Schematic of 8-bit TCAM using capacitive sensing

This schematic shows the modified 8-bit TCAM with capacitive sensing using AND gate lector approach.

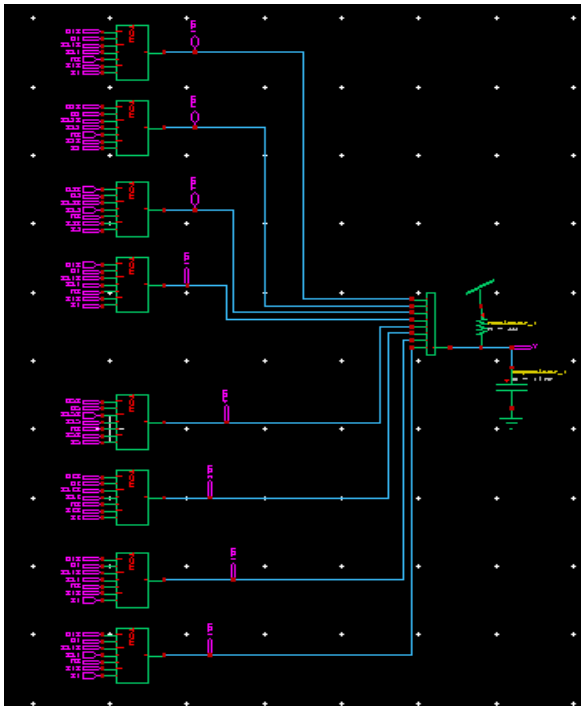

Fig25: Schematic of 8-bit TCAM using Resistive sensing

This schematic shows the modified 8-bit TCAM with Resistive sensing using AND gate lector approach.

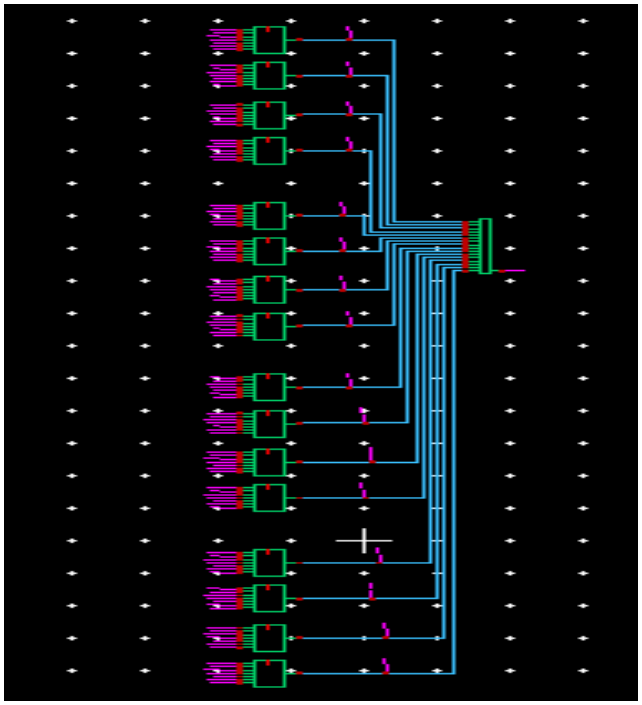

Fig26: Schematic of 16-bit TCAM

This schematic shows the modified 16-bit TCAM using AND gate lector approach.

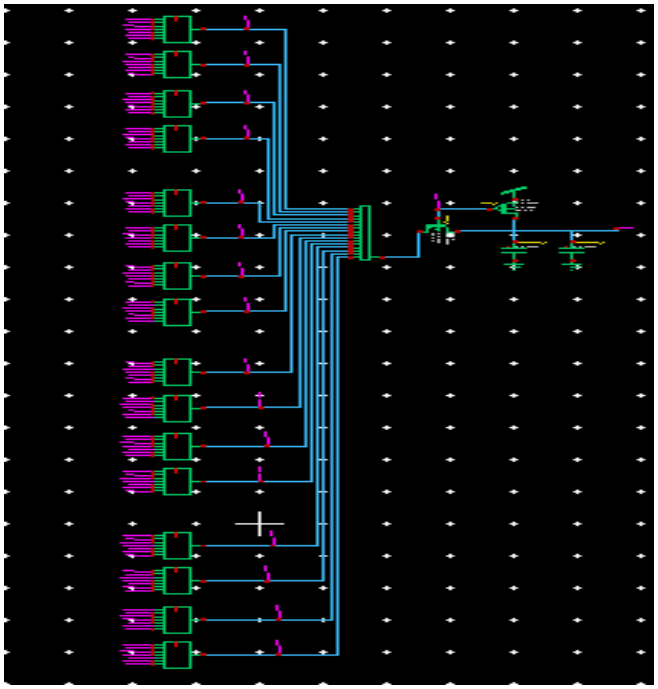

Fig27: Schematic of 16-bit TCAM using capacitive sensing

The illustrated diagram depicts the enhanced 16-bit TCAM configuration incorporating capacitive sensing, achieved through the utilization of an AND gate logic approach..

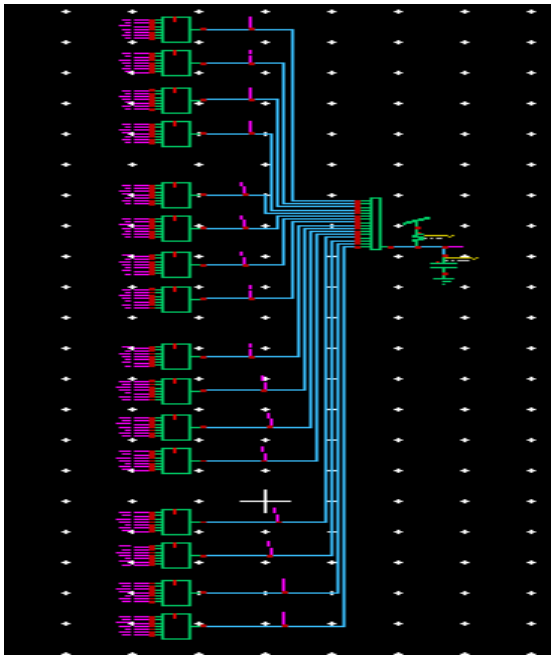

Fig28: Schematic of 16-bit TCAM using Resistive sensing

The presented schematic showcases the modified 16-bit TCAM configuration featuring resistive sensing, achieved through the utilization of an AND gate logic approach.

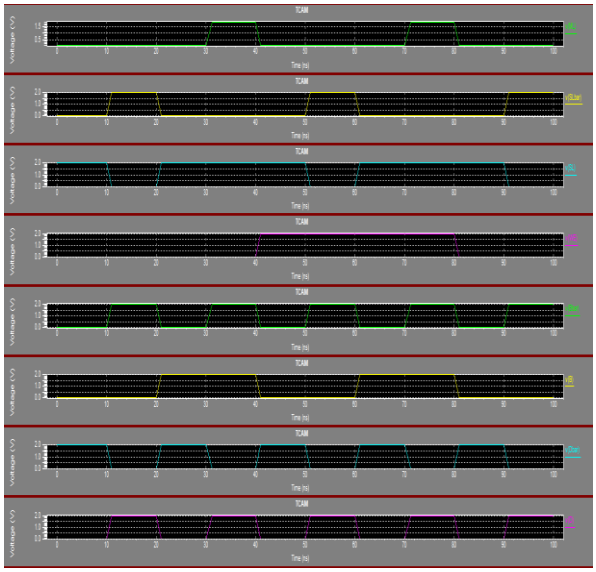

Fig29The waveform illustration of a 1-bit TCAM.

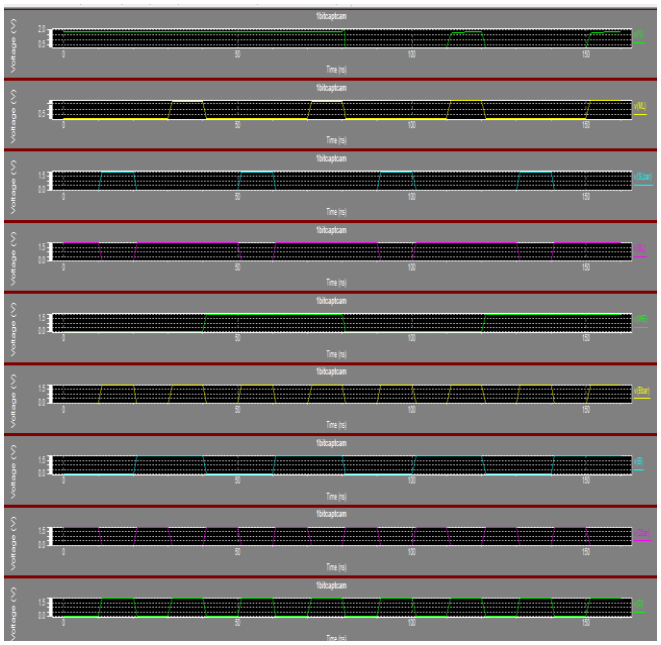

Fig30: The waveform representation of a 1-bit TCAM employing capacitive sensing.

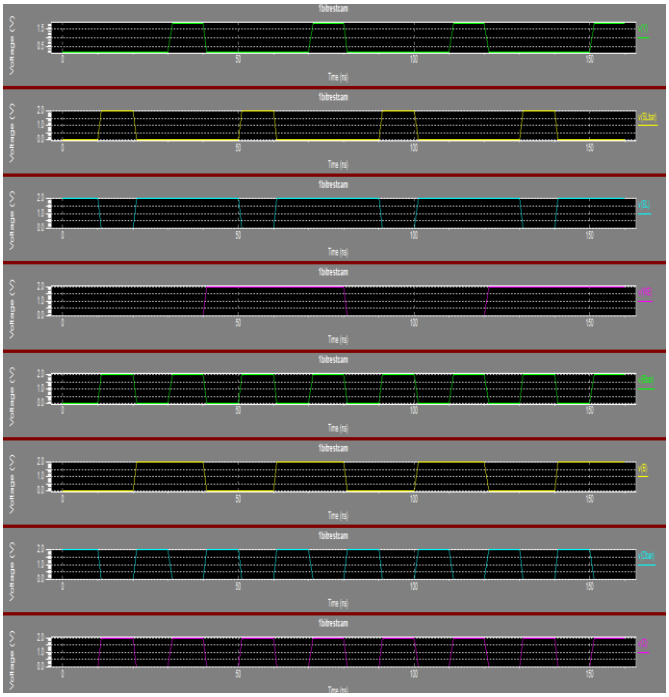

Fig31The waveform depiction of a 1-bit TCAM utilizing resistive sensing.

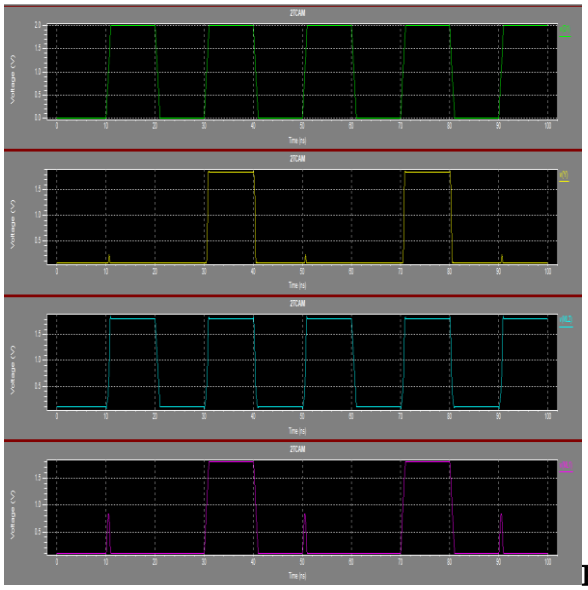

Fig32: The waveform illustration of a 2-bit TCAM.

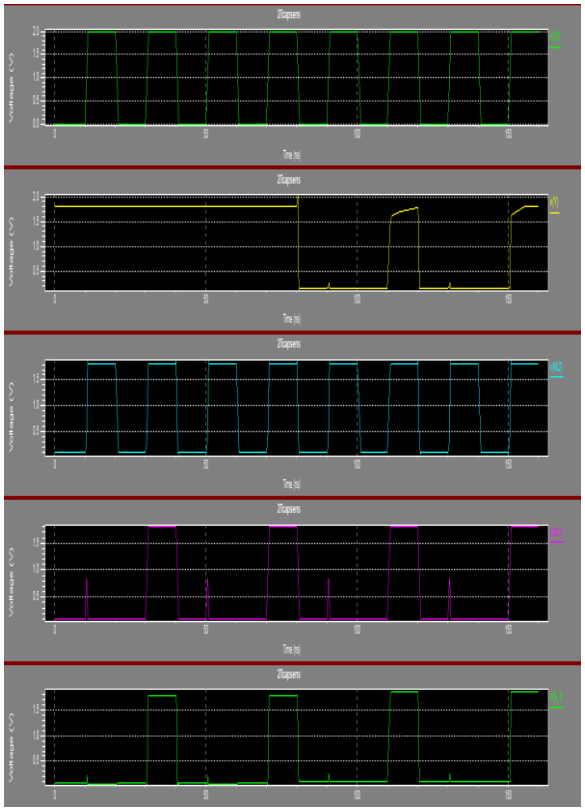

Fig33: The waveform presentation of a 2-bit TCAM utilizing capacitive sensing.

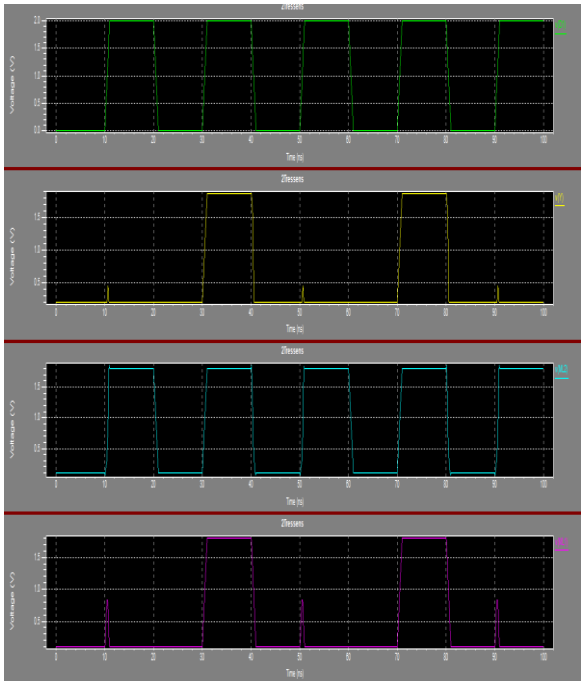

Fig34: Waveform of 2-bit TCAM with Resistive sensing

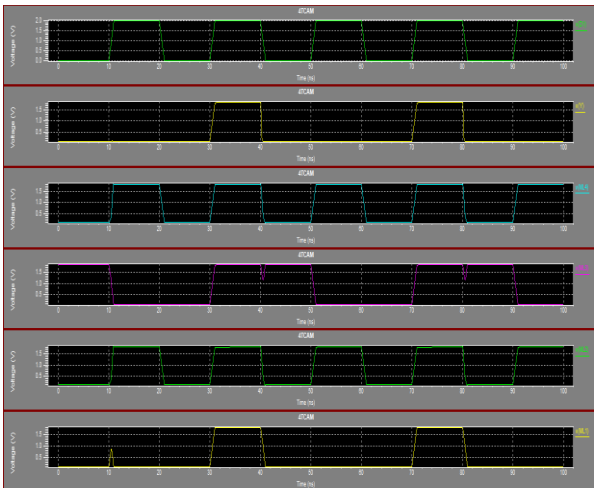

Fig35The waveform depiction of a 4-bit TCAM.

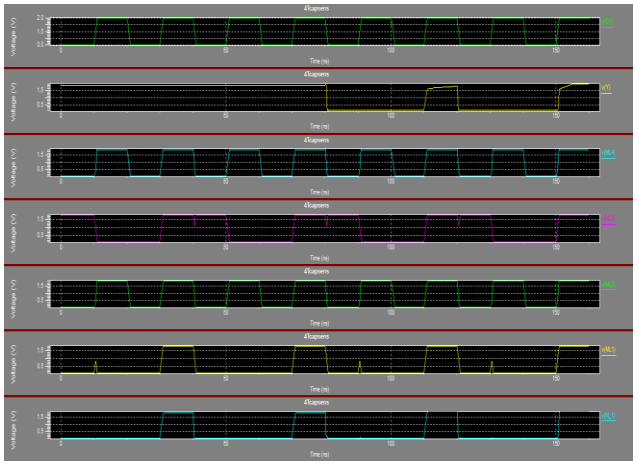

Fig36: The waveform representation of a 4-bit TCAM employing capacitive sensing.

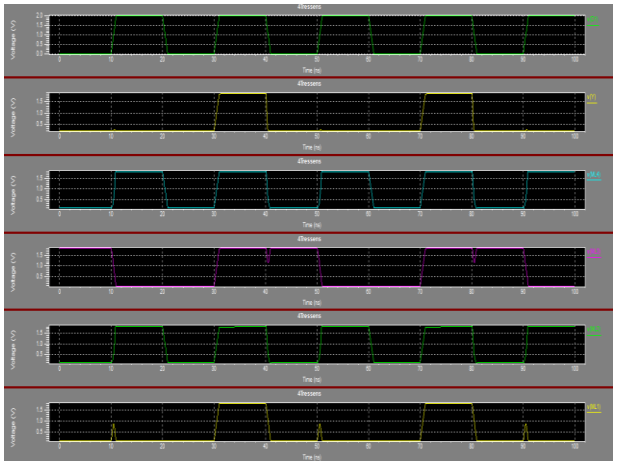

Fig37: The waveform visualization of a 4-bit TCAM utilizing resistive sensing.

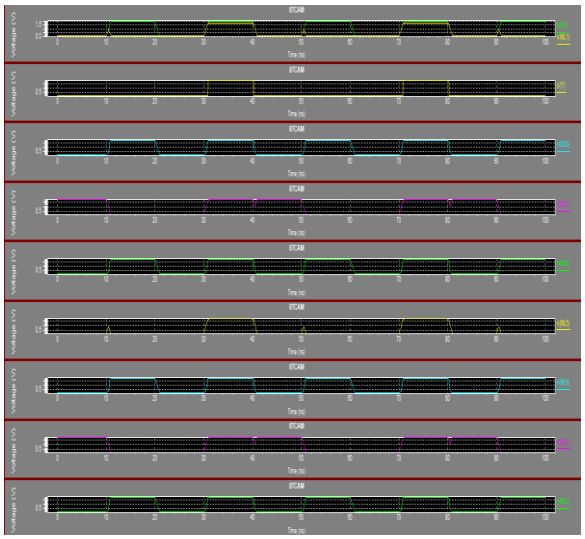

Fig38: The waveform representation of an 8-bit TCAM.

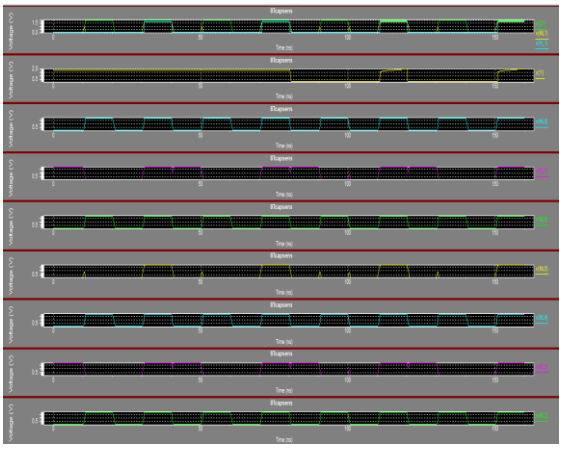

Fig39: The waveform illustration of an 8-bit TCAM utilizing capacitive sensing.

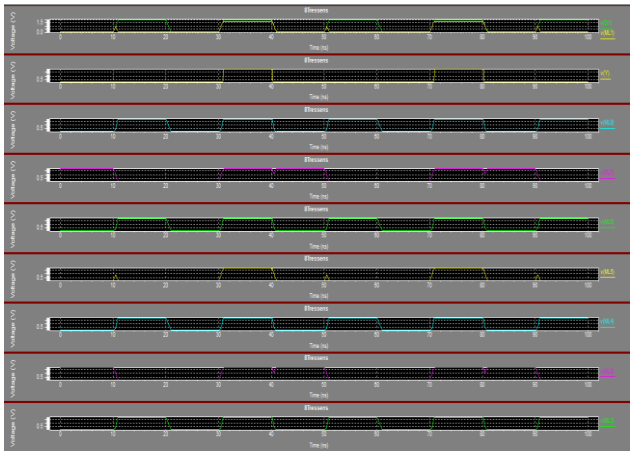

Fig40: The waveform depiction of an 8-bit TCAM employing resistive sensing.

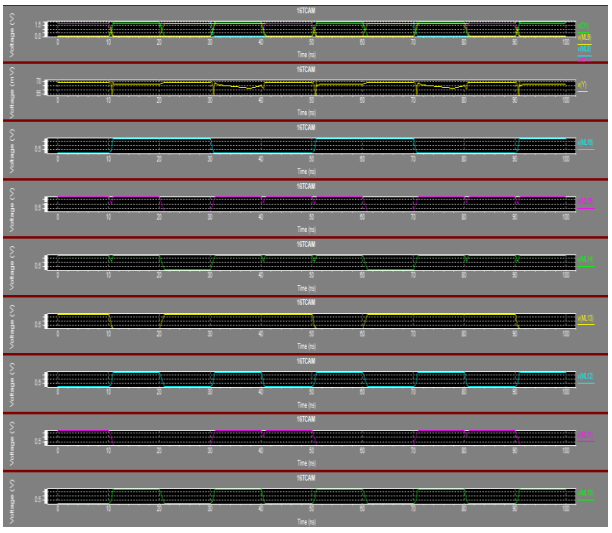

Fig41: The waveform depiction of a 16-bit TCAM.

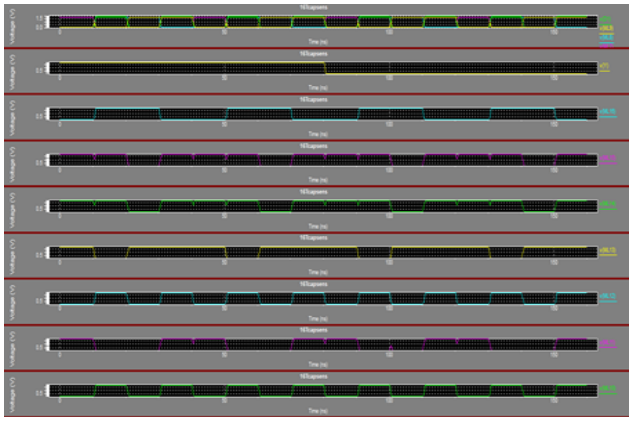

Fig42: The waveform illustration of a 16-bit TCAM employing capacitive sensing.

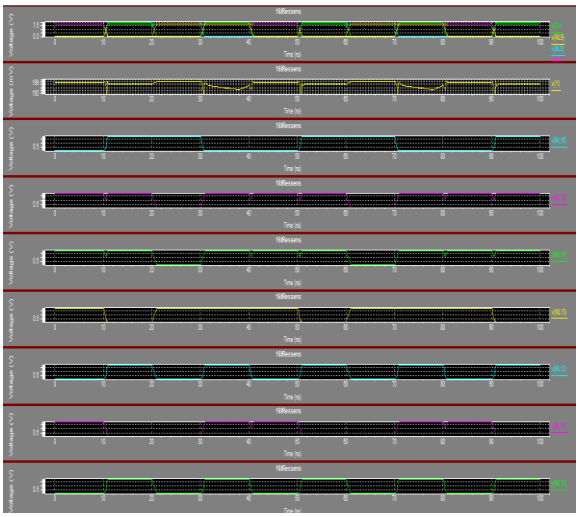

Fig42: The waveform representation of a 16-bit TCAM employing resistive sensing.

V. Comparison table

TECHNOLOGY	AREA	POWER	DELAY
2TCAM	34	3.602643e-003W	6.4139e-010
2TCAM CAPSENSING	36	3.85606e-003W	8.067e-008
2TCAM RES SENSING	34	4.0464e-003W	2.1035e-010
4TCAM	66	6.81959e-003W	7.735e-010
4TCAM CAPSENSING	68	7.07473e-003W	8.0808e-008
4TCAM RES SENSING	66	7.258048e-003W	7.6949e-010
8TCAM	138	1.4303e-002W	2.0539e-008
8TCAM CAPSENSING	140	1.455949e-002W	1.0056e-007
8TCAM RES SENSING	138	1.476262e-002W	2.054e-008
16TCAM	258	2.633422e-002W	9.4595e-011
16TCAM CAPSENSING	260	2.658286e-002W	7.0247e-008
16TCAM RES SENSING	258	2.685237e-002W	1.6544e-010
EXTENSION			
2TCAM	36	3.446421e-003W	5.717e-010
2TCAM CAPSENSING	38	3.685520e-003W	8.0292e-008
2TCAM RES SENSING	36	3.87949e-003W	2.0984e-010
4TCAM	68	6.58167e-003W	2.6890e-010
4TCAM CAPSENSING	70	6.83889e-003W	8.0293e-008
4TCAM RES SENSING	68	7.046394e-003W	2.1247e-010
8TCAM	144	1.360436e-002W	2.0526e-008
8TCAM CAPSENSING	146	1.38737e-002W	1.0055e-007
8TCAM RES SENSING	144	1.40559e-002W	2.0522e-008
16TCAM	260	2.600188e-002W	5.5091e-010
16TCAM CAPSENSING	262	2.62627e-002W	7.0239e-008
16TCAM RES SENSING	260	7.0239e-008W	4.7208e-010

Here is the comparison table for conventional TCAM with sensing technique and modified TCAM with sensing technique.

VI. CONCLUSION

In this paper we implemented TCAM using sensing techniques and lector approach. The analysis that has been presented is responsible for the decrease in power use. By using a lector method in the AND gate design in the TCAM schematic and capacitive and resistive sensing techniques on the redesigned TCAM, the major goal is to reduce power consumption. In comparison to the TCAM's current structure, the suggested architecture minimizes both power dissipation and delay characteristics. Tanner EDA, which uses 45nm technology, is used in this to simulate the complete design.

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