International Journal of Scientific Research in Science and Technology
Available online at : www.ijsrst.com
OPEN ACCESS
Print ISSN: 2395-6011 | Online ISSN: 2395-602X
doi : https://doi.org/10.32628/IJSRST

Efficient PMOS-Biased Sense Amplifier Design Using Lector Biasing Technique for Low Power Applications

[1]U.Sri Sai Vihari, [2]Dr.CH.Hima Bindu

[1]PG Student, Department of Electronics and Communication Engineering, QIS College of Engineering and Technology, Pondur Road, Vengamukkapalem, Ongole, Andhra Pradesh, India.
[2]Professor, Department of Electronics and Communication Engineering, QIS College of Engineering and Technology, Pondur Road, Vengamukkapalem, Ongole, Andhra Pradesh, India.

ARTICLEINFO

Article History:

Accepted: 01 Sep 2023
Published: 10 Sep 2023

Publication Issue
Volume 10, Issue 5
September-October-2023

Page Number
117-122

ABSTRACT

The sensing amplifier is a key component in the circuits of a semiconductor memory chip. Its functioning has a significant impact on the reliability, operational efficacy, and efficiency of core memory designs. This analysis delves into the examination of two distinct circuit configurations. The first circuit design introduces a novel sensing amplifier that employs a PMOS biasing approach. This innovative implementation yields output outcomes equivalent to those previously established in prior research. However, a remarkable enhancement in both reduced sensing delay and diminished power dissipation is observed. This advancement is attributed to the utilization of a novel lector approach within the power gating strategies. Notably, this technique results in a lower output impedance. In summary, the simulation outcomes of the proposed sensing amplifier align harmoniously with the functions traditionally achieved by established circuits. A noteworthy distinction, however, lies in the consumption of energy. The utilization of the suggested sensing amplifier design demands notably less energy, without compromising on functionality. The comprehensive evaluation was conducted using Tanner EDA software and was executed utilizing the 180nm technology file. Through rigorous simulation and meticulous analysis, the overall performance of the newly introduced sensing amplifiers was ascertained and interpreted. The outcomes of this study contribute to the ongoing advancement and optimization of semiconductor memory chip circuitry.

Keywords: Sense delay, Sense Amplifier, lector approach, Power gating techniques.

I. INTRODUCTION

In contexts ranging from computer-oriented functionalities to image sensing and digital cameras, the integration of flash drives serves as a vessel for diverse data types including photos, audio, video, and voice. The enhancement of stored data quality hinges upon achieving minimal detection latency and an expanded capacity.

To amplify the minute voltage disparity along the bit lines during synchronized sensing intervals, sense amplifiers [1] are frequently employed [2-11] to accomplish remarkable staging rates. However, if the signal enabling the sense amplifiers is triggered prematurely, these amplifiers might struggle to sufficiently magnify the minor voltage difference.

A vital element within memories is the sensory amplifier, playing a pivotal role in their operation. Among its various functions, the sense amplifier's primary task is to accurately gauge memory access times. In the event of alterations detected in the bit-lines, the amplifier promptly steps in. Its role involves intensifying these signals before delivering them to the memory module. This process ensures the integrity and reliability of memory operations.

Sense Amplifier:

The electronic configuration comprises of sensory amplification apparatus within a semiconducting storage unit (integrated circuit) present in contemporary computer memory. The nomenclature for this arrangement finds its roots in the era of superconductor memory. Within this framework, a sensing amplifier constitutes a crucial element of the scanning circuitry, facilitating the retrieval of data from the memory. Its core purpose revolves around the task of distinguishing low-power signals originating from a specified bit line. This process, in turn, signifies the specific data bit either 1 or 0 stored within an associated memory cell. Additionally, the sensing amplifier undertakes the task of augmenting the restricted power supply fluctuation to levels that promptly correspond to recognizable logic thresholds. This augmentation ensures that data remains intelligible to the logic components even in instances where the memory itself might not be accessible.

There are two types of sense amplifiers. Non-differential amplifiers are also referred to as current mode sense amplifiers. At the start of a read cycle, the bitlines are precharged. Consequently, in memory arrays featuring enlarged bitline capacitances, current mode operation is often adopted along with sense amplifiers. Current mode sensing amplifiers also find standalone applications. The bitlines are connected to the inputs of the amplifier, and as the bitline discharges, a reduction in the output voltage level occurs, governed by the subsequent current flow following the precharge phase.

The effectiveness of integrated memory and its surrounding circuits can impact the overall speed and power of the entire system. The Sense Amplifier is a peripheral circuit that is of utmost significance in CMOS memory. It is essential for locating or sensing read-only memory's stored data.

II. EARLIER WORK

A memory's sensing amplifier [22] is one of its crucial parts as well as has a big impact on the process, especially on the duration of memory accesses. The amplifier recognises alterations that take place in the bit-lines, strengthens the signals, as well as transmits them to the memory. Crafting rapid and energy-efficient sensing amplifiers, especially in submicron CMOS technology [23-25], presents a challenging endeavor for designers.

PMOS Bias Sense Amplifier:

A. Sense amplifier-1:

Sense amplifier operation involves two key elements: precharging and signal amplification. The sensor nodes are forced to reach preset potentials by the

requisite signals being delivered to them during the precharge phase.

During the sensing phase, the currents of the sensor nodes are contrasted. This comparison gives the contents of the memory cell. The output impedance of Circuit 1 of the Sense amplifier is high as well as there are no static problems. This is due to the fact that the amplifier circuit's T1, T2, and T17 all have gate contacts that are shorted-circuit. As current travels over both bit lines in this design, Ir exceeds Ic, resulting in a little discrepancy.

Thus, the current Ii-Id will be transmitted via bit-line BL2, whereas the current I1 will be transmitted through BL1. Figure 1 depicts a proposed sensing amplifier circuit employing PMOS biasing.

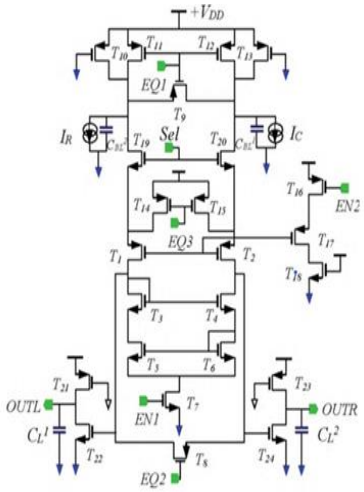

Fig1: A sensing amplifier's-1 circuit

In optimal synchronization, transistor pairs T3-T4 and T5-T6 operate. Thus, the input as well as the output currents are potentially regulated when the potentials at the input as well as output are identical. This design minimizes the transistor count compared to traditional sense amplifiers, leading to reduced power consumption and lower latency. Colonial PMOS bias-type sense amplifiers, on the other conjunction, demand greater power as well as employ more transistors. The Sense amplifier circuit stirs OUTL as well as OUTR from T1 and T3, as well as T2 and T4, accordingly. The power usage of the sensing amplifier is decreased, as well as the sensing latency is decreased as a result.

B. Sense amplifier -2

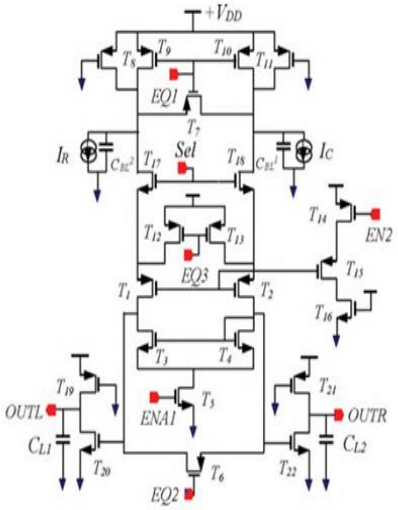

Fig2: A sensing amplifier's circuit -2

The second recommended sense amplifier architecture is demonstrated in Figure 2. OUTL and OUTR are each connected to T1 and T5, whereas OUTL and OUTR are connected to T2 and T6. The enhanced amplification system has a shorter sensing latency as well as requires less power.

The two sense amplifier circuits that are suggested have the following input configuration: The circuit-2 upper segment's preamplifier phase precharges the bit lines using T7 to T11 transistors. The ability to supply the circuits with several currents is made possible by the use of a selection input. This is achieved by connecting two constant current sources to the bit-line capacitance. Although the potential of the bit lines can be controlled by three equitable distribution inputs, EQ1 is often used in these situations. The outputs outL as well as outR are delivered to the inverters via the load capacitance.

III.PROPOSED WORK

Reduced power consumption is the goal of the techniques of transistor stacking, clock gating, and power gating. The main contributor to static power consumption in MOSFET devices is attributed to leakage currents.

Researchers have developed several power gating techniques to address this issue. In this paper, we introduce two sense amplifier circuits that utilize the

lector technique. Among the power gating methods available, the lector approach stands out. By employing this technique, we can conserve energy by deactivating the circuit's power supply.

Lector technique basics:

At the core of our plan to curtail leakage power lies the adept arrangement of transistors throughout the circuit, spanning from the supply voltage down to the ground. The strategic deactivation of multiple transistors along the route from the supply voltage to the ground results in a significant decrease in leakage, as opposed to a scenario where only a solitary transistor within that pathway is powered down. In accordance with our methodology, each CMOS gate is enriched with a pair of transistors dedicated to leakage control (referred to as LCTs). These LCTs are thoughtfully positioned, with one of them intentionally placed in close proximity to the cutoff zone.

Sense Amplifier with A PMOS Base:

A. First proposed circuit of sensing amplifier:

To be employed in the suggested sense amplifier arrangement, we modified the conventional pmos bias sense amplifier circuit. We utilised the lector technique to the load inverters to reduce static power use.

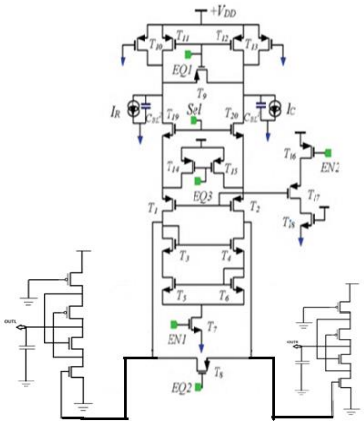

Fig3: Proposed sense amplifier circuit-1

B. Sensitivity Amplifier 2 Proposed Circuit:

In order to reduce power consumption, the suggested sense amplifier circuit-2, as shown below, uses the lector approach at the load inverters.

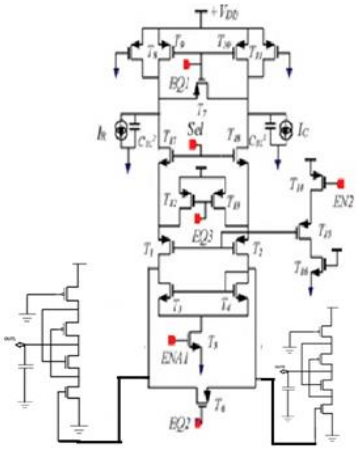

Fig4: A sense amplifier-2 proposed circuit

In the load inverters of the second suggested sense amplifier circuit, which is depicted below, the lector technique is used. This approach is pursued to achieve the goal of reducing power consumption.

Transistors T7 through T11 play a role in precharging the bit lines within the preamplifier phase at the upper section of the circuit. Differential currents for the connections are supplied utilising the selection input. The bit-line capacitance is connected between two sources of continuous current to accomplish this. Equilibrium is created between the bit lines by using three inputs for reconciliation. In most instances, EQ1 is set for equalization purposes. The outputs, designated as outL and outR, are delivered to the coupled inverters across the load capacitance.

IV. EXPERIMENTAL RESULTS

The Cadence Virtuoso Tool was employed to simulate circuits created using 180 nm CMOS technology. Consistent fan-in and fan-out configurations were maintained across all simulation scenarios. The transistors within the current mirror and the sense amplifiers depicted in Figure 1 were designed with uniform dimensions, specifically a length (L) of 0.18 micrometers (μm). It's worth noting that "Ir" corresponds to the memory component, while "Ic"

corresponds to the reference cell current. The utilization of standardized components and the precision of the Cadence Virtuoso Tool enabled accurate and reliable simulations of the circuit behavior..

The operational efficacy of the sensing amplifier is notably influenced by the capacitance of the bit-lines. This connection is elucidated in Figure 5. To evaluate the proposed sense amplifier's functionality, an in-depth transient analysis was conducted.

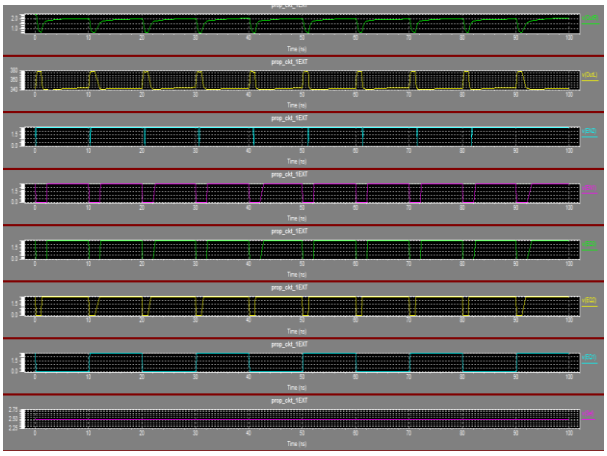

Fig5: Transient outcomes of the suggested sense amplifier-1

However, Figure 6 shows the results of the transient analysis performed for the suggested sense amplifier.

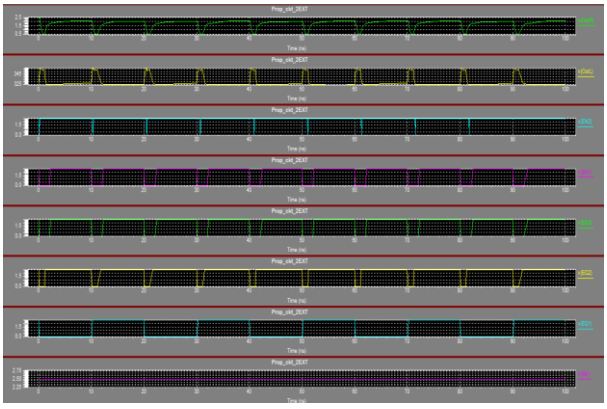

Fig6: Transient outcomes of the suggested sense amplifier-2

V. CONCLUSION

Two innovative sense amplifiers were constructed using Tanner EDA, employing the 180nm CMOS technology. The transient outcomes of the suggested sense amplifiers aligned closely with the theoretical analyses of the original sense amplifiers. Additionally, a graphical representation depicting the simulated sensing delay at different supply voltages was generated. The proposed circuits incorporated a lecturer technique, effectively reducing both power consumption and delay by employing forward biasing for load transistors.

VI. REFERENCES

[1]. Chrisanthopoulos, Y. Moisiadis, Y. Tsiatouhas and A. Arapoyanni, “Comparative study of different current mode sense amplifiers in submicron CMOS technology”, IEE Proc.-Circuits Syst., Vol. 149, No. 3, June 2002, pp.154-158.

[2]. S. Yang, W. Wang, N. Vijayakrishnan, and Y. Xie, “Low-leakage robust SRAM cell design for sub-100 nm technologies”, in Proc. ASPDAC, 2005, pp.539-544.

[3]. Mahendranath. B and Avireni Srinivasulu, “Performance analysis of a new CMOS output buffer”, in proc. of IEEE International Conference on Circuit, Power and Computing Technologies, Kumaracoil, India, Mar 21-22, 2013, pp. 752-755. Dol: 10.1109/ICCPCT.2013.6529041.

[4]. T. Srivyshnavi, and A. Srinivasulu, “A current mode Schmitt trigger based on Current Differencing Transconductance Amplifier: without any passive components”, in proc. of IEEE International Conference on Signal Processing, Communications and Networking, Chennai, India, March 26-28, 2015, pp. 1-4. DOI: 10.1109/ICSCN.2015.7219884.

[5]. Madira Suma, V.Venkata Reddy and Avireni Srinivasulu, “Current mode Schmitt trigger

based on ZC-current differencing transconductance amplifier", in proc. of IEEE International Conference on Inventive Computation Technologies, pp. 439-443, Aug 26-27, 2016, Coimbatore,India.DOI:10.1109/INVENTIVE.2016.7823226.

[6]. Sayeed Ahmad, Mohit Kumar Gupta, Naushad Alam, and Mohd. Hasan, "Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol.24, No. 8, August 2016.

Cite this article as :

U. Sri Sai Vihari, Dr.CH.Hima Bindu, "Efficient PMOS-Biased Sense Amplifier Design Using Lector Biasing Technique for Low Power Applications", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 10 Issue 5, pp. 117-122, September-October 2023.
Journal URL : https://ijsrst.com/IJSRST52310514