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ASIC Implementation of Duty Cycle Correction Circuit

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ABSTRACT
Duty cycle is a crucial component of VLSI circuits and this paper introduces an accurate Duty cycle correction circuit with high measurement accuracy and range of correction. Experimental and theoretical results are closely correlated.

Keywords—duty cycle, multiplexer, clock, delay line

I. INTRODUCTION

In this study, a circuit for fine duty-cycle control in high- frequency systems is presented. The suggested digital circuit is more reliable, simpler to use, and capable of higher- frequency resolution improvements. It is crucial for high- speed circuits and logic families because it determines how much time is allotted for the precharge and evaluate phases; if this time is off from the desired value, performance will suffer. The clock signal can be further weakened by environmental and process variables, making it challenging to produce and disseminate high-frequency clocks with a fixed duty cycle[2].

Before giving the clock signals to sensitive parts of the design the duty cycle value is measured. The measurement is based on a specific logic and once the measurement is done, based on the duty cycle value the clock is switching to the correction circuit.[1] The correction can be controlled from the controller. The amount of correction required is controlled by the selection bits from 0 to 15. Each bit's selection will correct the input clock signal by a fixed amount.

II. TECHNOLOGY AND TOOLS USED

A. 90 nm Technology

Leading semiconductor companies such as Toshiba, Sony, Samsung, IBM, Intel, Fujitsu, TSMC, Elpida, AMD, Infineon, Texas Instruments and Micron Technology have commercialized the 90 nm process for MOSFET (CMOS) production between 2003 and 2005 with historic associated with a 70% upward trend every two to three years. The International Technology Roadmap for Semiconductors (ITRS) specifies the designation. For base layer lithography, mostly at the 90nm node, many (but not all) companies have adopted the 193nm wavelength. The significant costs associated with this change were reflected in performance concerns (due to the use of new photoresists). The 300 mm wafer is also important

B. CADANCE

The Cadence Virtuoso® System Design Platform offers the capability to drive simulation and LVS-clean layout of ICs and packages from a single schematic. It offers two main flows: implementation and analysis. The implementation flow generates an IC package design, while the analysis flow isolates and simulates any system component.

III. DUTY CYCLE CORRECTOR

By altering the adjuster circuit's control bits, the duty-cycle of the input clock can be corrected. By adjusting these control bits to reach a 50% duty-cycle, the detector determines the duty cycle.

There are delay lines in the suggested duty-cycle adjuster. The adjuster consists of two rising edge generators: one fixed rising edge generator with dummy delay lines, latch, and MUX, and the other variable rising edge generator with 6-bit programmable delay lines. The falling edge generator changes the duty-rate using the input clock's non-inverted or inverted signal, MUX selection, and 6-bit control signals of the programmable delay line.

In older duty-cycle adjuster circuits based on delay lines, the duty-rate modification is performed using falling edge generators or by employing both rising and falling edge generators

The duty-cycle adjuster's schematic is depicted in Figure 1. By turning on the PFET stack for a brief period of time (17-inverter delay) and latching one in the feedback circuit, the circuit sends the rising edge of the input clock directly to the node X. A delay line with programming options delays the falling edge. This delayed edge turns off the feedback when it arrives, pulling down the node X by activating the NFET stack. Up to the appearance of the subsequent rising edge, the feedback circuit remains latched in a zero state. Controlling the delay through the programmable delay line allows one to alter the duty-cycle of the input clock. Designing an adjuster with a specific resolution and tuning range allows for control.

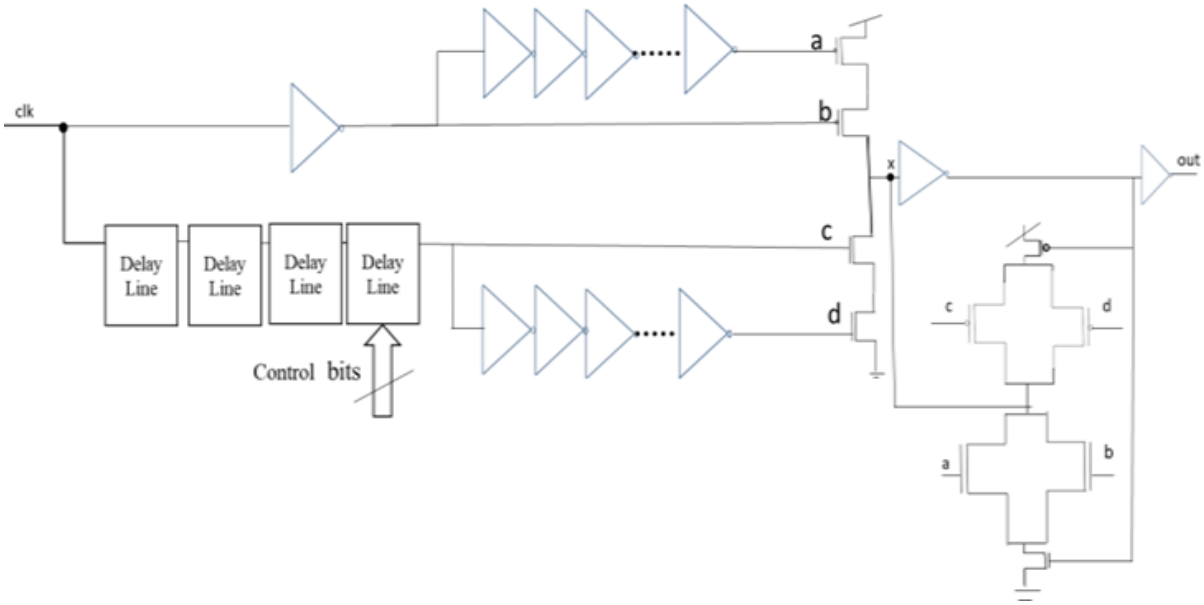


Figure1. Circuit diagram of duty cycle adjuster

If used in these circuits, the period of the lowest operating frequency is the minimum length of the delay line required to give the entire 50% correction range. To reduce delay lines, we just use a falling edge generator for

duty-rate control with a 16x1 input-inversion MUX. While conventional 1 delay line circuits without signal inversion need at least 128 delay inverter cells to achieve the required correction range for this study, our adjuster uses delay line cells that are 512 lengths long.

The adjuster circuit plays a significant role in the duty-cycle correction circuit. In order to alter the duty-cycle of the input clock, it is responsible for controlling the delay between two complementary signals. Using the phase detector's false signal as input, the charge pump generates a DC voltage from the loop filter and sends it into the adjuster circuit. The adjuster circuit then changes the distance between two complementary signals to fix any duty-cycle issues with the input clock.

In other words, the correction circuit consists of a phase detector, charge pump, loop filter, and adjuster, among other components. An essential component of this circuit, the adjuster, works with other circuits to rectify any duty-cycle errors in high-frequency clocks with very low.

There is no duty-rate change during the initial period of duty rectification for the Sign determination of the input clock duty- cycle. The duty-cycle adjuster's clock input for the Sign can be either an uninverted or an inverted clock input. There is no guarantee of the rising-edge (or falling-edge) clock having a set delay. However, Figure 4 shows the clock input as being made up of a combination of D-Flip flops and AND gates as a clock generator with the selectable edge comparison of the falling edge. The D-Flip flop, which can be used as the synchronization information of the delay line, can be given the Sign information. According to the control signal Sign from the DCC, the major drawback of this adjuster edges is that the DLL requires a specially constructed phase detector that analyses only the rising and falling edges, leading to a complex DLL design.

A. Abbreviations and Acronyms

VLSI -very large-scale integration

ASIC- Application Specific Integrated Circuit.

PFET-P-channel Metal oxide semi-conductor field effect transistor

NFET-N-channel Metal oxide semi-conductor field effect transistor

MUX-multiplexer

DCC-duty cycle corrector DLL-delay locked loop

ITRS–International Technology RoadMap for Semiconductors.

nm- Nano meter

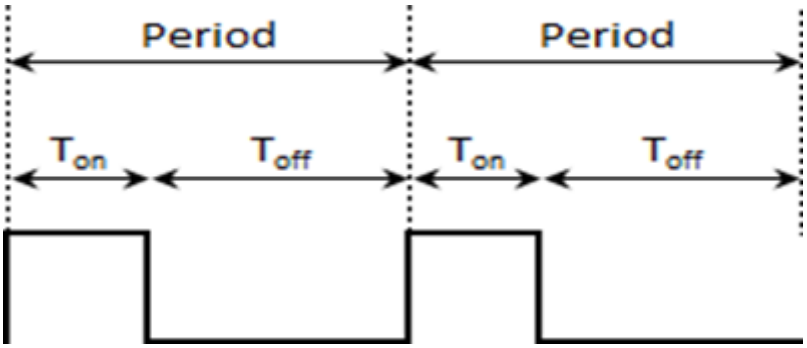
LVS- Layout Versus Schematic

PCB- Printed Circuit Board.

IC- Integrated circuit BOM- Bill of Materials.

B. Duty cycle.

The idea of duty cycle correction circuits, its significance in ASIC design, and typical implementation methods. ASIC implementation of duty cycle correction circuit and frequency range design considerations for duty cycle correction circuit performance jitter. To identify the proper circuit clock skew on the signal topology, the frequency range of the signal that the circuit should be designed to better needs to be corrected, taken into account, and reduced. A signal's duty cycle tells you how much of the time it is ON (at logical high-high voltage).



period = 1 / Frequency period=Ton+Toff

Duty cycle = Ton (Ton+Toff) *100 (on percentage)

The duty cycle adjuster is vital component of the circuit, which works on the principle of adjusting the pull up and pull- down strength of the inverter via fed back digital signals. This circuit uses two steps of correction with first stage doing coarse correction and second stage doing fine correction.

ON time / (ON time + OFF time) = Duty Cycle

Example for 35% - 63%:

Let's take a look at the first simulated output i.e 35% - 63%.Here we have given clock as input in the form of pulse. We have taken 10ns as period and 3.5ns as pulse width which makes 35% duty cycle to the clock signal and fed it to circuit. As we simulate the results by selecting the input and output lines on ADE L suite, we obtain the output that is Vout as 63%

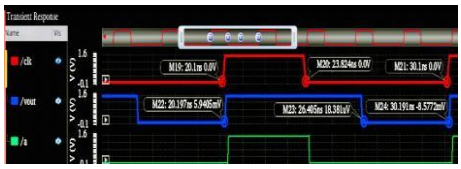
.It means that we get 6.3ns as ON time and 3.7ns as OFF time. By this we can conclude that we have enhanced duty cycle by 28% of the input value.

IV. RESULTS

By adjusting the parameters of the programmable delay line, we can measure the duty-cycle of the output while feeding the adjuster the same 8-GHz clock.

The graphic demonstrates that less than 1% steps can be used to adjust the input clock's duty cycle from 15% to 63%.

The feedback loop chooses the adjuster's ideal settings. Our findings demonstrate that the loop can accurately output a 50% duty-cycle for a wide range of input duty-cycles.

ENHANCED DUTYCYCLE	SIMULATED OUTPUTS
35-63%	

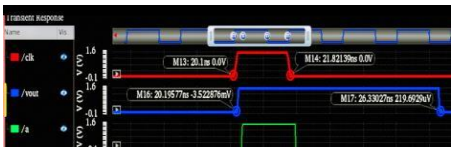
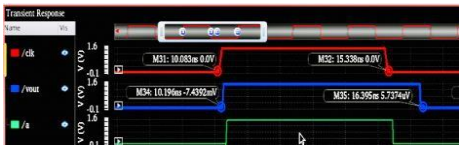
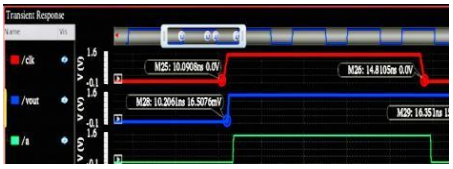
15-62%	
50-62%	
45-61%	

Figure 2: Enhanced duty cycle simulated outputss

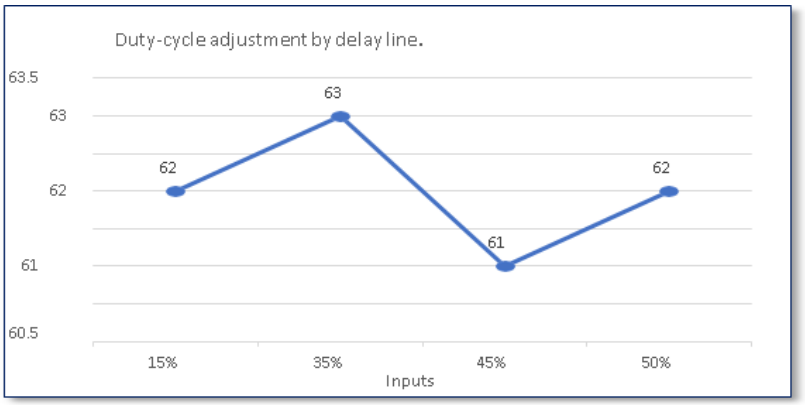


Figure 3: Duty cycle adjustment by Delay line

V. APPLICATIONS

In real-time systems where precise timing is important, the duty-cycle correction circuit has a wide range of applications.

i. High-speed communication systems:The duty-cycle correction circuit is used in high-speed communication systems to ensure accurate timing for data transmission.

ii. Digital signal processing:It is used in digital signal processing applications to improve the accuracy and efficiency of operations such as filtering, modulation, and demodulation.

iii. Microprocessors and microcontrollers: In microprocessors and microcontrollers, accurate timing is essential for executing instructions and controlling peripherals.Test and measurement equipment:It is used in test and measurement equipment to generate and measure signals with high precision by ensuring accurate timing.

Overall, the duty-cycle correction circuit has a wide range of applications in real-time systems where accurate timing is critical.

VI. ADVANTAGES AND LIMITATIONS

A. Advantages:

i. Limited input frequency range:- The duty-cycle correction circuit provides very presise resolution and great accuracy for adjusting the duty-cycle of high-frequency clocks.

ii. Limited output voltage swing:- It is digital and does not need outside references or matching devices, making it more durable and less susceptible to changes in the environment and manufacturing

iii. processes sensitivity to noise: The duty-cycle correction circuit is ideal for a variety of applications because it can correct the duty-cycle of an input clock with a wide range of duty-cycles, typically from 25% to 75%.

iv. Noise sensitivity: the duty-cycle correcting circuit is perfect for a wide range of applications because it can correct the duty-cycle of an input clock with a wide spread of duty-cycles generally from 25 to 75

B. Limitations

i. Power utilization: As the number of inverters increases, so does the area. As a result, we utilise more power consumption.

ii. Complexity: It may be more difficult to develop and implement the duty-cycle correction circuit due to its possible complexity when compared to more traditional analogue duty-cycle correction processes.

VII. CONCLUSION

For instances it is demonstrated how to control the duty cycle of clocks in high-performance systems using a digital circuit. The circuit can be used to correct for duty-cycle inconsistencies caused by environmental and process fluctuations. The results show that the circuit is more resilient and capable of producing very fine resolution when compared to analogue techniques currently being used for duty- cycle correction.

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