

Use of Resonance in Induction Cooker

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ARTICLE INFO

Article History:

Accepted: 10 Nov 2023

Published: 30 Nov 2023

Publication Issue

Volume 10, Issue 6

November-December-2023

Page Number

291-295

ABSTRACT

Resonance is a highly helpful tool for induction heating processes, such as melting, heating, and of course, using induction cookers and other household appliances. The investigation of resonance is done in this publication. Their fundamental circuit schematic, a two-series and parallel resonance comparison. Next, choose the most effective resonance methods, such as the induction cooker's series resonance.

Keywords : Induction heating, series resonance

1. Introduction

When the impedance and resistance of a circuit become equal at a given frequency, this is termed the resonance frequency. Basically, resonance is separated into two categories:

Resonance in series

Resonance in parallel

A circuit is referred to as serial resonance when a circuit capacitor is linked in series with a load. A circuit is referred to be parallel resonance if a circuit capacitor is linked in parallel with the load. The series and parallel resonance results are also produced by simulation. Current is magnified in a series resonance situation, whereas voltage is magnified in a parallel resonance situation.

2. Design Considerations

A series circuit is connected across an a.c. source of constant voltage V but of frequency varying from zero to infinity. There would be a certain frequency of the applied voltage, which would make X_L equal to X_C in magnitude.

In that case, $X = 0$ and $Z = R$, as shown in figure 3.

3. Requirement for Induction Cooker

The following are the specifications for induction cookers: Ultrasonic switching frequency, dependability, large power range (usually 10% to 100%), high efficiency, cheap cost, and power factor almost equal to unity.

Typically, induction cookers are meant to be used with cooking vessels composed of a particular material, most commonly ferro-magnetic stainless steel or cast iron. Therefore, the following features should be present in the converter:

1. Only the heating coil and no other reactive parts range for a workable range of frequencies,
2. Clamped current and/or voltage on switches, 3.50% duty ratio, making gating and control simpler circuits
4. Making use of a voltage source under control.

4. Choice of Converter

The following factors led to the selection of the full-bridge, series resonant topology [2, 3, 4]: A clamp is applied across the semiconductor voltage. Because switching is done at a 50% duty ratio, no feedback is required. As seen in Fig. 3, anti-parallel composite switches (CS), which are composed

of an anti-parallel diode (D) and a double switch (S), are required. The reason why silicon control rectifiers (SCRs) are displayed is that they are an excellent fit for this medium-frequency application. The 50% duty ratio allows for the usage of a modest isolation transformer. This converter can use either of two switching techniques—forced commutation or load commutation—to provide the required power control without changing the input voltage [1,10]

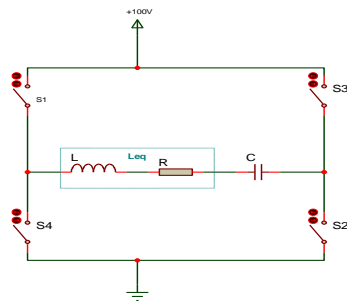


Fig. 3 Full Bridge circuit with series resonant

A. Load Commutation

The switching frequency (f_s) is lowered below the damped resonant frequency (f_r) to reduce power. This has the following benefits and drawbacks:

Benefits

No way to cut off the power to the individual switches, and no activate the anti-parallel diodes' power loss.

Negative aspects

2. Switch on the individual switches' power loss and turn shutting down power loss and reversing the anti- diodes in parallel.

3. At the maximum limit of the available power, the frequency of switching.

Commutation under duress

Increasing f_s above f_r reduces the power and has the following benefits and drawbacks:

Benefits

The anti-parallel diodes do not experience reverse recovery current or turn-off power loss, and the solitary switches do not experience turn-on power loss.

2. Maximum power is obtained at the lower limit of the switching frequency.

Disadvantages

Turn-off power loss for the singular-switches and turn-on power loss for the anti-parallel diodes.

The forced commutated converter was chosen due to the elimination of the reverse recovery current of the diodes and the maximum power being obtained at the lowest point of the switching frequency range, usually about 2.5 kHz.

5. Load Arrangement

For induction cooking, a flat heating coil is utilized, as illustrated in Fig. 4. To prevent the heating coil from overheating and to support the cooking pot, a thermal insulator is positioned between it and the coil [8]. Usually, the coil needs to be cooled by forced air. Fig. 4 depicts the load arrangement's comparable circuit. The heating coil and cooking vessel are represented by the series combination of C1 and L, and the cooking vessel can be represented by an equivalent series inductance (L_r) and resistance (C1), which are provided by the resonant capacitance, which is typically metallized polypropylene. To get an initial voltage across S, S1 and S2 are closed first, and S3 and S4 are left open. S1 and S2 are activated and S3 and S4 are then closed to obtain resonance between C.

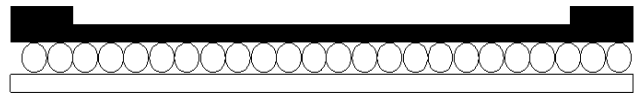


Fig. 4 Load arrangement of Induction cooker

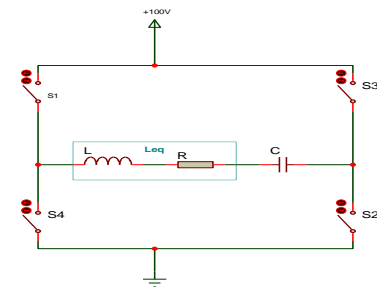


Fig. 5. Equivalent circuit of Load arrangement of Induction cooker

6. Proposed Block Diagram of the System

Proposed block diagram as shown in fig. 6 consist of the three parts [14,15,16]

- A. High Frequency Circuit
- B. Firing Circuit
- C. DC Source
- D. Thyristor Bridge

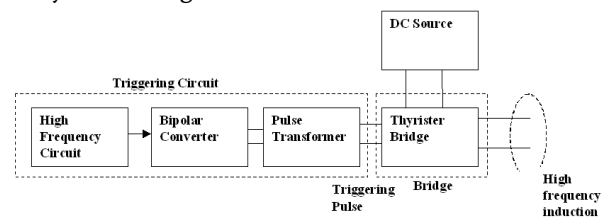


Fig. 6 Block diagram of the Project

6.1 High Frequency Circuit

This circuit is designing using IC 555 Timer as a astable multivibrator here frequency is generated of 1 KHz square wave which is given to the input firing circuit as clock for the IC 7473. A detail analysis is given in the design section.

Features

- High Current Drive Capability (200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C

6.2 Firing Circuit

This firing circuit uses an isolation transformer to isolate the high voltage. It also includes a bipolar converter. Here, the SCRs are fired by the produced pulses. Primarily, we ignite the initial two SCRs (S1, S2) and SCRs (S3, S4), necessitating four firing pulses—two of which are identical and produce the positive half cycle, and the other two, the negative half cycle. To be isolated from high-voltage and high-current thyristor bridges, a pulse transformer is utilized. Fig. 7 displays a block diagram of the firing circuit.

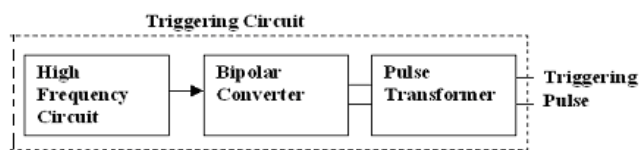


Fig.7 Block diagram of Firing Circuit

6.3 DC Source

The DC source can generate 100V and 10A by design. It is made up of a filter capacitor and a bridge rectifier. 230V AC is converted to 100V pulsing DC by a bridge rectifier, and the ripple content is eliminated using a capacitor.

6.4 Thyristor Bridge

This is essentially a chopper design in which the average DC output is produced by firing SCRs concurrently while they are coupled in a bridge. The firing frequency has an impact on the average DC output. When this DC high current output passes through an inductor coil, heat is produced that is utilized for induction heating.

7. Implementation of Proposed System

DESIGN CONSIDERATIONS

To bridge inverter topologies, a few design specifications are required. These are covered below:

Two 100 V input voltages are the input voltage (V_{rms}). Peak power output (P_{max}): Maximum power output One thousand W of power was assumed. P_{min} , or minimum

output power, is the minimum power When requested, it was regarded as 25% of the upper limit. strength. Switching frequency (f_{sw}): For the design's maximum powers, a switching frequency of 5 kHz was taken for granted; it can be changed to achieve lower powers. Additionally, it was presumed that every device had SCRs. Additionally, a common value of 0.5 for the pan-inductor coupling's power factor is assumed in the design (1).

$$FP = \frac{R_{eq}}{\sqrt{R_{eq}^2 + \{L_{eq} \cdot 2\pi \cdot f_{sw}\}^2}} \approx 0.5 \quad (1)$$

7.1 High Frequency Circuit

As shown in fig. 8 we used IC555 as timer in astable mode here the frequency used is 5 KHz. Supply current when output is high is typically 1mA less at $V_{CC} = 5V$

2. Tested at $V_{CC} = 5.0V$
3. This will determine maximum value of $R_9 + R_8$ for 5V operation, the max. total $R = 20M\Omega$, and for 5V operation the max. total $R = 6.7M\Omega$

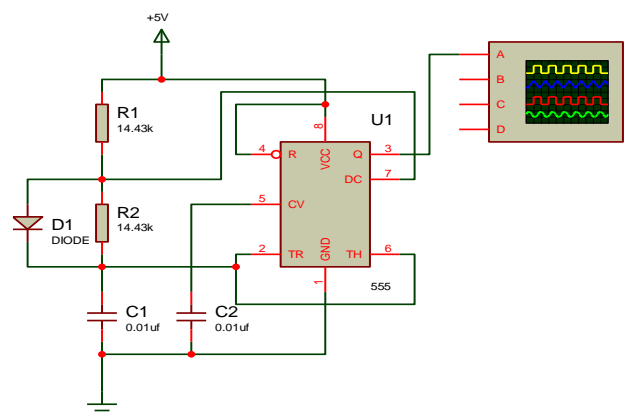


Fig. 8 High Frequency Circuit

An astable timer operation is achieved by adding resistor R2 and R1 as shown in figure 8. In astable operation, the trigger terminal and the threshold terminal are connected so that a self-trigger is formed, operating as a multi vibrator. When the timer output is high, its internal discharging T_r turns off and the VC1 increases by exponential function with the time constant T_{on} or $T_r \cdot 0.693(R1) \cdot C1$. When the VC1, or the threshold voltage, reaches $2V_{cc}/3$, the comparator output on the trigger terminal becomes high, resetting the F/F and causing the timer output to become low. This in turn turns on the discharging C3 through the discharging channel formed by R8 and the discharging internal transistor and given by T_{off} or $T_d \cdot 0.693(R2) \cdot C1$.

When the VC1 falls below $V_{cc}/3$, the comparator output on the trigger terminal becomes high and the timer output becomes high again. The discharging transistor turns off and the VC1 rises again. In the above process, the section where the timer output is high is the time it takes for the VC1 to rise from $V_{cc}/3$ to $2V_{cc}/3$, and the section where the timer output is low is the time it takes for the VC1 to drop from $2V_{cc}/3$ to $V_{cc}/3$. When timer output is high, the equivalent circuit for charging capacitor C1 is as follows:

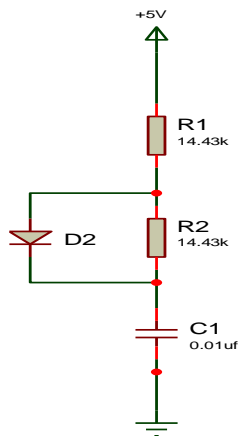


Fig. 9 Charging circuit of IC 555

A Diode is connected across the Resister R2 to get 50% duty cycle. Hence formula for the calculation of Frequency, T_{on} and T_{off} is as given,

For 5 KHz,

$$T = 1/5\text{KHz} = 0.2\text{ms}$$

$T_{on} = T_{off} = 0.1 \text{ ms}$ required for 5 kHz frequency

$$T_{on} = 0.693 * R1 * C1$$

$$0.1 \text{ ms} = 0.693 * R1 * C1$$

Assume $C1 = 0.01 \mu\text{F}$.

$$R1 = 0.1\text{ms} / (0.693 * 0.01\mu\text{f})$$

$$= 14.43\text{Kohms.}$$

$$T_{off} = 0.693 * R2 * C1$$

$$0.1 \text{ ms} = 0.693 * R2 * C1$$

Assume $C3 = 0.01 \mu\text{F}$.

$$R8 = 0.1\text{ms} / (0.693 * 0.01\mu\text{f})$$

$$= 14.43\text{Kohms.}$$

For 5 KHz frequency a components values are chosen

$$R2 = 14.3 \text{ K Ohms}$$

$$R1 = 14.3 \text{ K Ohms}$$

$$C1 = 0.01 \mu\text{F}$$

A Diode is connecte across the Resister R8 to get 50% duty cycle.

7.2 Firing Circuit

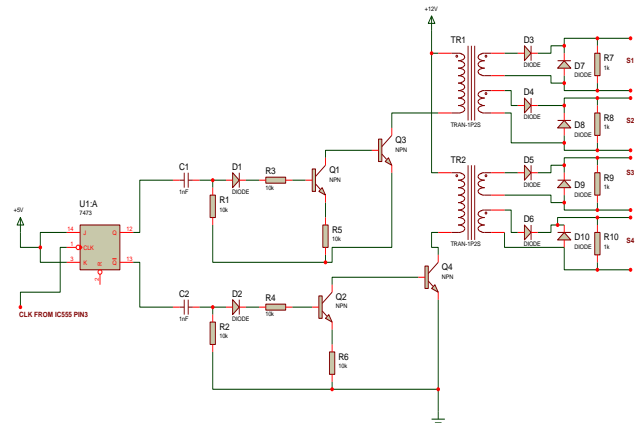


Fig. 10 Firing Circuit

As shown in fig 10 This circuit consist of transistor Q1 as switch which is driven by the high frequency IC555. This will generate firing pulses at the output of the pulse transformer. Diode D3, D4, D5 and D6 are used to stop negative pulses and allowed to pass only positive pulse to the firing circuit. This also used to protect the firing circuit from the high voltage available at the SCR's. Capacitor C1 and C2 is pass only AC to the base of the transistor and block the DC component. IC 7473 is JK FF which is configured in T Flip flop and generate the equal and opposite signal for the firing of SCR's

7.3 DC Source

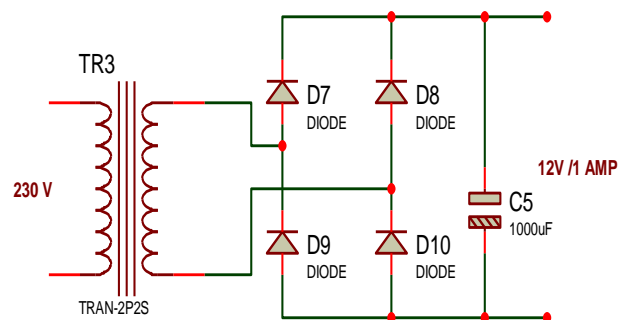


Fig. 11 DC Source

Fig. 11 is DC Source which generate the high current (Appr. 10A) and voltage (100 V DC). Here transformer is 230V/100-0 V. and D7, D8, D9 and D10 are used in the bridge configuration which gives the output 100 V DC. Capacitor C5 1000uF/450V acts as filter to give pure DC. This 100 V DC is fed to the SCR's where it is chopped at high frequency 2.5 KHz which generate output of 1000W and 2.5 KHz

7.4 Thyristor Inverter topology

A. Full-bridge inverter

The full-bridge topology is the most complete allowing many control possibilities. In this case the full bridge topology with a series resonant load LC is analyzed (Fig. 12). The following characteristics were assumed for the design at maximum output power:[9]

□□*Square wave*: since it provides the highest rms voltage in the load (V_{LOAD}). Equation (2) shows the decomposition in harmonics.

□□*Switching frequency equal to natural oscillation frequency of the load (fn) (3)*: since it provides that the power factor for the load at the switching frequency is one[12].

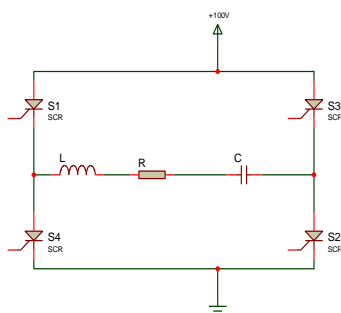


Fig. 12 full bridge topology with a series resonant load LC

$$f_{res} = \frac{1}{2\pi\sqrt{L_{eq}C_{res}}}$$

where V is the input dc bus voltage (Fig. 12).

The devices must be chosen in order to withstand the maximum voltage and have the appropriate performance in conduction. The devices used for the implementation of the topologies for the cases of 1000 W and 100V As consequence the full-bridge inverter is the most efficient topology.

C) Power control

The inverter must be able to let the power control in order to be adjusted to the user's requirements. This control is normally carried out by varying the switching frequency. This variation is defined by the modulation factor (m) related to the frequency at maximum power ($f_{sw} P_{max}$) (15). The frequency variation necessary to let the power control with each inverter topology is shown in Fig. 12.

$$f_{sw} = m \cdot f_{sw} P_{max} \tag{15}$$

5 Results

Experimental converters have been used to validate topology designs. SCR transistors were utilized in their construction. Thyristors have been used to create the control circuits, and the firing circuits are displayed.

9. Conclusion and future scope

The common topologies for resonant inverters used in induction cookers have been developed and put into use. Because it uses less current to power its components, the full-bridge architecture is the most efficient; yet, it is more difficult to build.

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Cite this article as :

S. R. Ghuge, S. U. Borade, R. R. Gaikwad, " Use of Resonance in Induction Cooker", International Journal of Scientific Research in Science and Technology(IJSRST), Print ISSN : 2395-6011, Online ISSN : 2395-602X, Volume 10, Issue 6, pp.291-295, November-December-2023. Journal URL : <https://ijsrst.com/IJSRST52310645>