International Journal of Scientific Research in Science and Technology
Available online at : www.ijsrst.com
OPEN ACCESS
Print ISSN: 2395-6011 | Online ISSN: 2395-602X
doi : https://doi.org/10.32628/IJSRST

Enhancing Pll Performance with An Advanced Ring VCO Design Utilizing the Sapon Method

[1]S.R. Sree Phani Monish, [2]Dr. G. Hemalatha

[1]M.Tech Student, Department of Electronics and Communication Engineering, K.S.R.M College of Engineering (Autonomous), Kadapa, Y.S.R (D.t), Andhra Pradesh, India

[2]Professor and HOD, Department of Electronics and Communication Engineering, K.S.R.M College of Engineering (Autonomous), Kadapa, Y.S.R (D.t), Andhra Pradesh, India

ARTICLEINFO

Article History:

Accepted: 10 Dec 2023
Published: 20 Sec 2023

Publication Issue
Volume 10, Issue 6
November-December-2023
Page Number
418-424

ABSTRACT

This research describes a novel technique to improving PLL performance by adding an advanced Ring Voltage-Controlled Oscillator design based on the SAPON (Systematic Approach for Performance Optimization) method. The traditional PLL architecture has limitations in terms of power consumption. To address this, we propose a comprehensive design methodology that leverages the SAPON technique for systematic optimization. We discuss the theoretical framework behind our design, provide simulation results to validate its effectiveness, and compare it to conventional PLL implementations. The proposed system demonstrates substantial enhancements in lower power consumption, making it suitable for a wide range of applications, including wireless communication and high-speed data transmission. This research offers valuable insights into optimizing PLL performance and presents a promising solution for achieving superior stability and precision in modern communication systems.

Keywords : PLL, SAPON, High-Speed Data Transmission

I. INTRODUCTION

In order to provide a clock signal that consistently relates to a reference clock signal and allow systems to be synchronised, developers developed the Phase-Locked Loop (PLL), a system of feedback controls [1]. Employed for an extended duration, the PLL technique serves various purposes, including power generator phase maintenance, synchronization with TV pulse signals [2], recovery of clocks from asynchronous data, and FM signal demodulation, among other applications. Although it has diverse uses, its primary application lies in frequency synthesis. Figure 1 shows a schematic illustration of a PLL. The primary goal of the PLL is to synchronise the VCO output with an externally supplied standard

signal as well as the frequency divider output. These signals ensure that a VCO's phase remains stable over time.

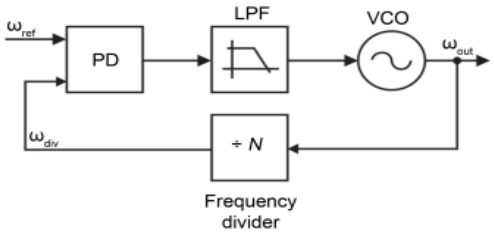

Fig.1: Phase-Locked Loop block diagram

Principle of PLL:

At the core of a PLL is the essential task of understanding and adjusting the phase disparity between two signals. The information regarding the phase error or difference between these signals serves as the basis for regulating the loop's frequency.

For a more profound comprehension of the concept of phase and phase difference, consider visualizing two waveforms, usually depicted as sine waves, as they appear on an oscilloscope. When the trigger is engaged simultaneously for both signals, they will appear at separate positions on the screen.

Phase-locked loops (PLLs) have been widely used in high-performance microprocessors and high-speed digital communication systems as clock generators. As the speed of these systems is increasing PLLs with higher operating frequency and lower jitter are in demand [7]. An observed phase disparity exists between the two signals, and this distinction is measured as the angle between them. Importantly, this angle is calculated between corresponding points on the two waveforms. In this case, a zero crossing point has been chosen, but any consistent point on both waveforms can serve as a reference.

The phase difference can be visualized on a circle since the two waveforms occupy distinct positions in the cycle due to their phase disparity. This phase difference is quantified as an angle, precisely, the angle created by the lines emanating from the center of the circle to the points that symbolize the waveforms.

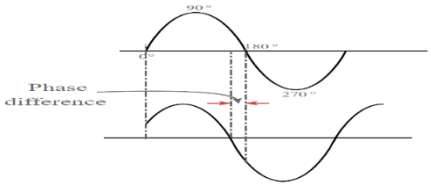

Fig.2: Difference in phase between two signals

When two signals display distinct frequencies, the phase offset between them undergoes continuous variations. This dynamic behaviour stems from the distinct time required for each cycle, resulting in their movement around the cycle at different rates.

From this observation, it can be inferred that when two signals share precisely the same frequency, their phase difference remains constant. Even though a phase difference may exist, it implies that they do not simultaneously reach identical points on the waveform. Consistency in the phase difference indicates a persistent lag or lead of one signal over the other by the same amount, affirming their synchronization at the same frequency.

Phase locked loop operation:

While certain operational aspects and mathematical analysis may add complexity, the fundamental principle that governs the PLL's functionality is fundamentally straightforward. The phase detector, the voltage-controlled oscillator, and the loop filter are the three main components of an elementary phase-locked loop, as depicted in the schematic.

The voltage-controlled oscillator signal and the reference signal are connected to these two phase detector input ports through the basic PLL architecture. Before the voltage-controlled oscillator is connected to the timing detector's output, it is first processed through a loop filter.

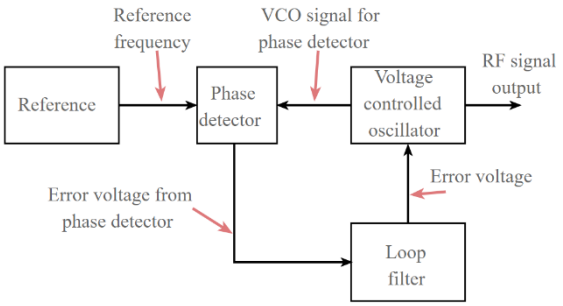

Fig.3: Phase loop Lock Diagram showing voltages

The Voltage-Controlled Oscillator (VCO) produces a signal when it is operating in phase detector mode ($PLL). This stage compares the phase of the VCO with the incoming reference signal to determine the phase difference between the two signals, which is represented by the error voltage. Following that, the phase detector error signal is filtered using a low-pass filter, moulding various loop properties and removing high-frequency components. The error signal serves as the tuning voltage for the VCO's control terminal shortly after filtering. The goal of adjusting this voltage is to reduce the signal's phase and, as therefore, the variance in frequency between the two signals.

The loop is initially misaligned, and the error voltage directs the VCO frequency towards the reference signal until further error reduction is impracticable, indicating the loop is now locked.

A steady error voltage is produced in the locked condition. The use of an amplifier between the phase detector and the VCO reduces the actual error between the signals to extremely low levels. However, a specific voltage must remain at the VCO's control terminal to ensure that the frequency is maintained.

A consistent error voltage denotes a constant phase difference between the reference signal and the VCO. The stability in the phase signifies that these two signals are precisely on the same frequency.

II. EARLIER WORK

The architecture exhibits enhanced performance, featuring reduced power dissipation, a smaller footprint, and an expanded frequency range for the PLL. This improvement is attributed to the utilization of A low-power Voltage-Controlled Oscillator (VCO) with a broad tuning range is designed, featuring nearly constant amplitude concerning the control voltage. Employing the switched capacitor technique, a capacitor and two transistors are used in place of the conventional resistor in the low-pass filter. The system's bandwidth and power consumption have both been verified through experimental testing. The system stands out due to its straightforward architecture, facilitating a robust dynamic response with minimized computational demands.

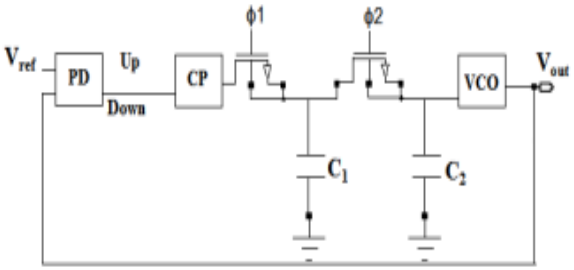

Fig.4: Schematic diagram of improved performance PLL

Proposed phase-frequency detector:

A logic high signal must be provided to the RESET input in order to reset the DFF and improve the output. The D flip-flop's D input is always connected to ground, so when the reference signal (Vref) rises, the first flip-flop (Up) delivers an output of zero. Further, a zero is sent to the second DFF's (Down) output as the VCO output (VVCO) develops. Once both signals are zero, the Up and Down signals go back to logic high, resetting both DFFs. This is accomplished by the multiplexer's output becoming one. If Vref surpasses VVCO, signaling the need for the VCO to catch up with Vref, this might cause an elevation in the VCO control voltage, subsequently increasing the output frequency of the VCO.

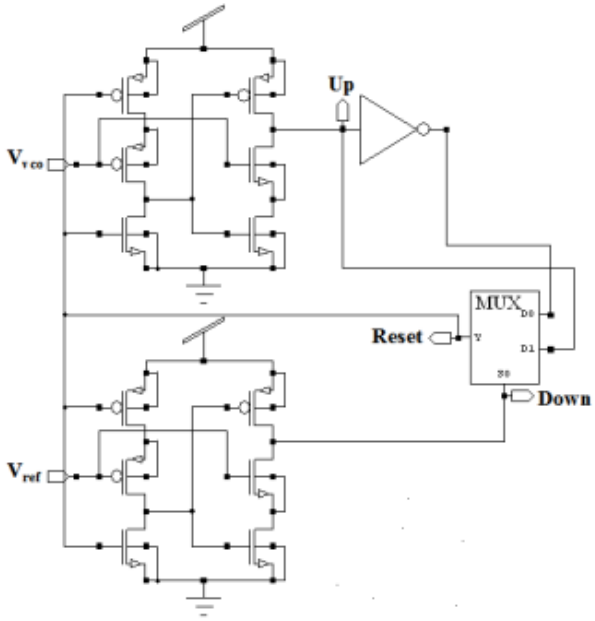

Fig.5: Schematic diagram of phase frequency detector based on multiplexer

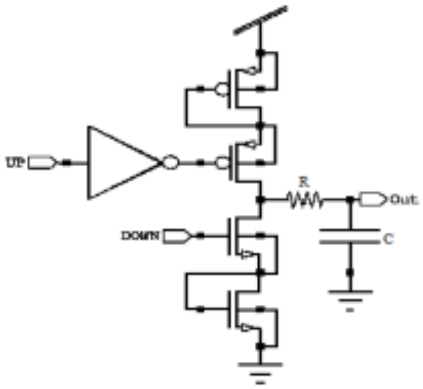

Fig.6: Low-pass filter schematic diagram using a charge pump

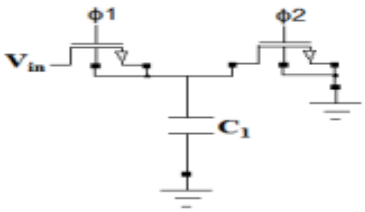

Fig. 7: Diagrammatic representation of a low pass filter employing the switched capacitor method

Charge Pump with Low-Pass Filter:

The charge pump has a major role in the Phase Frequency Detector (PFD) of a Phase-Locked Loop (PLL). By comparing the timing and phase of the Voltage-Controlled Oscillator (VCO) output with the reference signal, the PFD uses this configuration to create a current pulse via the charge pump. Error in timing/phase and coincidence in pulse duration. The loop filter then converts the PFD's output signal into a control voltage, addressing high-frequency noise. The charge pump comprises two switched current sources that transfer charge into or out of the Low-Pass Filter. The top PMOS and bottom NMOS act as current sources, while the middle PMOS and NMOS connect to the UP and DOWN outputs of the PFD, respectively (refer to Fig. 6). The current source can be connected to the loop filter when the PMOS opens and the PMFD UP signal is high. Likewise, an active corresponding NMOS occurs in response to a high PFD Down signal. Low-pass filters are often incorporated after the charge pump in order to minimise ripple. Instead of using a resistor, a switched capacitor technique can be used to fabricate the low-pass filter more quickly and compactly.

By activating and deactivating switches, a switched capacitor transfers the capacitor's internal and external charges. The signals φ1 and φ2, which do not overlap, as depicted in the diagram, are usually responsible for controlling these switches. One notable benefit of this approach is its adjustability, allowing modification of its value by manipulating the switching frequency.

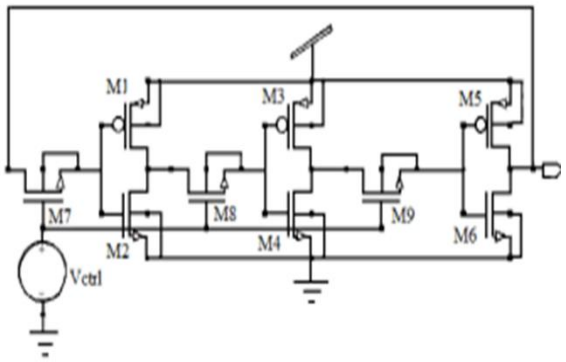

Fig.8: Diagram showing the improved performance of a three-stage voltage-controlled ring oscillator

In many different kinds of electronic systems, oscillators such as the Voltage-Controlled Oscillator (VCO) and others are essential components [11].

More specifically, the ring VCO includes an additional nMOS transistor in each inverter stage, with the variable resistance (RV) implemented using nMOS. The control of MOS transistor resistance is governed by the gate voltage. The illustrative image shows the inclusion of an additional nMOS transistor to- If we treat each inverter's MOS transistors as switches and keep both nMOS and pMOS equal, we can create a three-stage ring VCO. transistors' transconductance and parasitic capacitances (CG).

Voltage-controlled switching is the function of transistor M7. M7 gets biassed towards the conduction zone in the presence of a high Vctrl, which controls the switch. At the same time, the nMOS (M7) exhibits minimal resistance. This reduced resistance leads to a shorter delay, consequently elevating the VCO frequency.In the case of a low Vctrl, transistor M7 enters the cut-off region, resulting in a reduced output frequency. Consequently, it is essential for the resistance to undergo variations based on the control voltage. The inverter's rise and fall times hinge on the capacitor's charging and discharging. Furthermore, the current involved in these processes is affected by carrier mobility, which is greater for nMOS than pMOS, leading to an amplified drain current.

III. IMPLEMENTATION

This chapter discusses about the SAPON approach and its implementation in the design of our existing design PLL. Here, the SAPON approach is applied to MUX which acts as the submodule in the design of Phase Frequency Detector.

SAPON Approach:

In this method, the resistance between the supply voltage and ground is regulated by connecting two leakage-control transistors external to the logic. With this arrangement, leakage current is protected during the transition. Additionally, subthreshold leakage current during the levelling phase is controlled by using CMOS (Complementary Metal-Oxide-Semiconductor) SAPON transistors in series between the supply voltage and ground. The gate terminals of NMOS and PMOS SAPON transistors are connected to ground (GND) and Vdd (supply voltage), respectively.

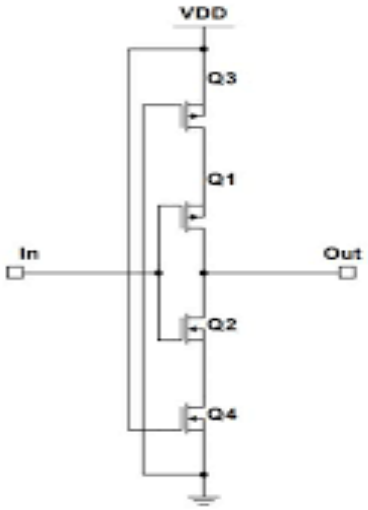

Fig.9: Block Diagram of SAPON Approach

Mux design using SAPON Approach:

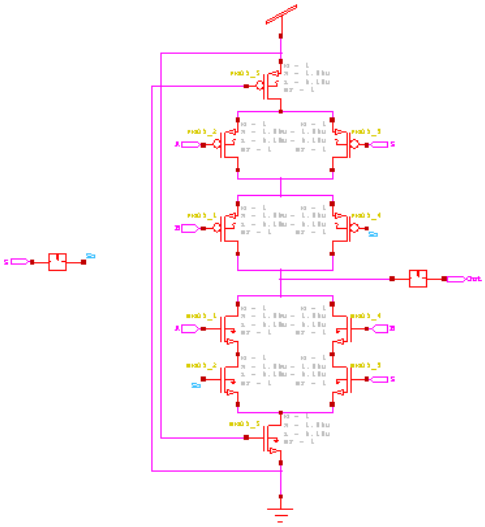

Fig.10: Schematic of Mux using SAPON

Phase-Frequency Detector Conceptualized:

Two D-flip-flops (DFFs) and a multiplexer make up the phase-frequency detector, as seen in the diagram. The RESET input restores the DFF, and increases the output level when a logic high signal is provided accordingly. It is always grounded when using the D flip-flop's D input. So, a zero is transmitted to the first

flip-flop's output (Up) when the reference signal (Vref) arrives on its rising edge. At the VCO output's rising edge (VVCO), the second DFF (Down) acquires a zero that is similarly divided. Up and Down signals are responded to through a logic high condition. when both are zero, which also resets both DFFs to make the multiplexer output one. If Vref exceeds VVCO, signalling that the VCO needs to catch up with Vref, the VCO control voltage may be increased, resulting in an increase in output frequency.

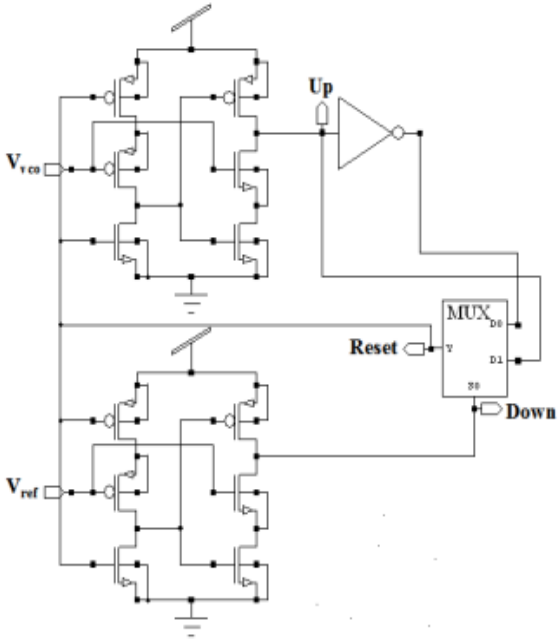

Fig.11: Diagram illustrating the phase frequency detector utilizing a multiplexer in schematic form

IV.RESULTS

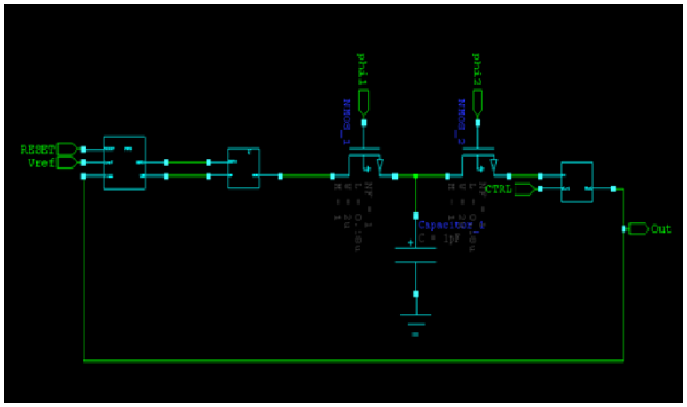

Fig.13: Schematic of PLL

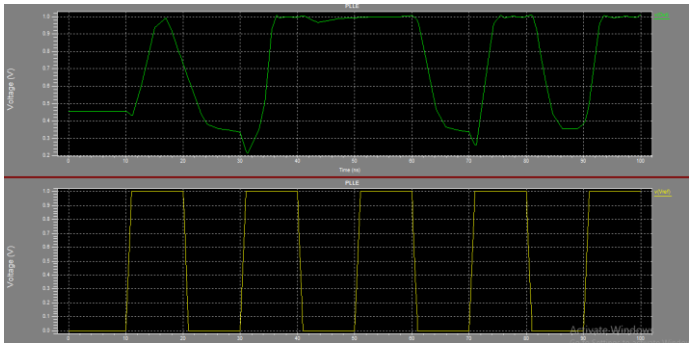

Fig.14: Waveform of PLL

Comparison Table

	Power	Delay	Area
Existing	96.22μW	26.39ns	43
Proposed	28.26μW	25.28ns	45

IV. CONCLUSION

In conclusion, the application of the SAPON method to enhance PLL performance through the utilization of an advanced Ring VCO design represents a significant step forward in the field of frequency synthesis and phase-locked loop technology. The systematic approach for performance optimization has allowed us to address several critical limitations associated with traditional PLL architectures. As technology continues to advance, the application of the SAPON method in PLL design promises to have a profound impact on various industries, ensuring that communication systems become more efficient and reliable in the future.

V. REFERENCES

[1]. Baranwal and Pateriya's study, published in January 2016, focuses on the development of IoT-based smart security and monitoring devices tailored for agricultural applications. This work was presented at the 6th International Conference on Cloud System and Big Data Engineering (Confluence), hosted by IEEE.

[2]. In a study conducted by Faical, B. S., Ueyama, and de Carvalho (2016), researchers explored the application of autonomous UAVs to enhance the distribution of pesticides in agricultural fields. This investigation was presented at the 17th IEEE International Conference on Mobile Data Management (MDM) in June 2016 (Vol. 2, pp. 32-33).

[3]. Suciu, G., Butca, Conu, Suciu, Hristea, Vochin, and Todoran (2016) conducted research in October 2016, focusing on the swift identification of pesticide residues using a telemetry platform. Their findings were presented at the 12th IEEE International Symposium on Electronics and Telecommunications (ISETC) (pp. 95-98).

[4]. Jaishetty, S. A., and Patil, R. A method utilizing an IoT sensor network for the monitoring and control of agricultural fields was presented in the International Journal of Research in Engineering and Technology (IJRET), with an electronic ISSN (eISSN) of 2319-1163.

Cite this article as :

S.R. Sree Phani Monish, Dr. G. Hemalatha, "Enhancing Pll Performance with An Advanced Ring VCO Design Utilizing the Sapon Method", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 10 Issue 6, pp. 418-424, November-December 2023.
Journal URL : https://ijsrst.com/IJSRST52310657