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Study of Scattering Cross Section and Scattering Mechanism for Mobility In Covalent Semiconductor

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ABSTRACT

In this paper, we present about the study of scattering cross section and scattering mechanism for mobility in covalent semiconductor (Si & Ge). Scattering in Silicon-Germanium With low power dissipation, high integration levels, good noise immunity, high cost-effectiveness and reliability, silicon CMOS Complementary Metal-Oxide-Semiconductor, technology occupies a dominant position in microelectronics. However, the low mobilities which is a figure of merit for semiconductor materials of electrons and holes in silicon limits its application to relatively low frequencies, leaving III-V materials such as Gallium Arsenide (and related materials) to fulfil roles in mobile communications and the like. Strained layers of silicon and silicon-germanium alloy offer scope for dramatic improvements in mobility, and therefore performance. New technology may possibly be incorporated into standard silicon CMOS processing, making the transition favourable to industry. Room temperature mobilities in silicon MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistor) tend to be around 300cm^2 V^{-1} s^{-1}for electrons, and less than 100cm^2 V^{-1} s^{-1} for holes, for sheet densities of the order of 10^{13} cm^{-2}.

Keywords: Scattering, Mobility, Semiconductor.

I. INTRODUCTION

The advantage of CMOS microelectronics is its very low power consumption compared to bipolar or NMOS technologies: ideally, a CMOS circuit only dissipates power as it is switching state and it is therefore desirable to equalize the switching time of n and p channel devices, and minimize the switching time overall. In practice this currently means that p-channel MOSFETs in CMOS integrated circuits must be made wider than corresponding n-channel MOSFETs for their conductances to match, and there

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is a trade-off between channel width and packing density. It would be advantageous to match the mobilities of electrons and holes, and to increase the mobilities of both electrons and holes overall. This will facilitate higher packing densities, higher operational frequencies or lower-power operation, depending on the requirements of the application. In addition to this desire to contribute directly to the semiconductor industry, silicon-germanium alloy strained-layer systems can be studied from the perspective of the fundamental physics of semiconductors. The results of these studies (often at liquid-helium temperatures or employing large magnetic fields, on devices with relatively poor characteristics) can then be considered when optimizing the design of industry-level devices for room-temperature operation. In the field of silicon-germanium research, the highest mobilities have been observed in systems with relatively low sheet carrier densities, meaning that the overall conductivity of the system is not necessarily impressive. The relationship between mobility and carrier density is fundamental to characterizing the mechanisms which limit the mobility and will be explored throughout this thesis, especially in the realm of higher sheet densities of both electrons and holes. This should lead, in conjuction with respectable mobilities, to the production of high conductivity devices with potential for high frequency operation. Additionally, research is traditionally carried out on devices which may be up to the order of a millimetre in length and measured parameters may or may not scale down to integration-scale devices on the scale of a few microns in length.

II. LOW-FIELD MOBILITY

Figure 1.1 shows the electron mobility versus electron sheet-density for Si and Ge substrates with SiO_2, HfO_2, $HfSiO_4$, and Al_2O_3 gate dielectrics. In this case EOT=1.0 nm and T=300 K. Ge [as seen in Fig. 1.1(b)] outperforms Si [shown in Fig. 1.1(a)] for all four dielectrics. This is due to the large bulk phonon-limited mobility which, in turn, is due to the smaller conductivity masses along the (111) in Ge. For both Si and Ge, HfO_2 yields the lowest mobility while the other dielectrics yield results on par with SiO_2. This is due to the low-energy phonons that give HfO_2 the largest dielectric constant of all four insulators considered [2]. Figure 1.2, illustrating the same data shown in Fig. 1.1, emphasizes the mobility reduction introduced by replacing SiO_2 with a high-κ dielectric, in this case HfO_2. Dielectric screening by carriers in the inversion layer reduces the strength of remote-phonon scattering at large electron densities. Thus, the percentage mobility reduction, $\Delta\mu = 38\%$ for Si, and $\Delta\mu = 46\%$ for Ge, is calculated at $n_s = 2 \times 10^{11}$ cm^{-2} . Of particular interest is the observation that the curves shown in the figures we have just discussed exhibit a maximum. This 'turn-around' is usually attributed to Coulomb scattering with the ionized dopants in the substrate. However, since this process is not included in our mobility calculations (Coulomb scattering is included in the Monte Carlo simulation), the turn-around appears to be due exclusively to scattering with SO modes. The strength of this process depends on the overlap between the SO-potential, φbfQ(z) ~ e^{-Qz} , and the initial, ζμ(z), and final, ζν(z), wave functions, In calculations bypassing the self-consistency between Poisson and Schr¨odinger equations, as the electron sheet density ns decreases, both the wave functions ζ and the SO-potential, e^{-Qz}, become less 'localized': The wave functions for obvious reasons, the SO-potential since wavevectors close to the Fermi wavevector, K_F , largely control the mobility, so that the function e^{-K_F} z becomes less 'squeezed' against the interface as ns decreases. Thus, the matrix element given by Eq. (1.1) above changes monotonically (and relatively slowly) with ns and no 'turn-around' is observed. On the contrary, when employing a self-consistent Poisson-Schr¨odinger approach with a large density of dopants, n_B, in the depletion layer, as the electron density is reduced, the confinement of the wave function decreases very

slowly at medium densities, since the confinement is largely due to the bulk dopant charge, en_B. Thus, the confinement of the wave functions changes slowly. On the contrary, the SO-potential, dependent only on ns via K_F, becomes less squeezed against the interface as before as ns decreases. This causes the matrix element, Eq. (1.1), to grow with decreasing ns as soon as n_B controls the confinement, resulting in the turnaround. Eventually, at even lower values of n_s, also the dopant bulk charge en_B will begin to drop, resulting in an increasing mobility.

III. SCATTERING-LIMITED ELECTRON MOBILITY

Figures 1.3 and 1.4 show the SO-limited and SR-limited mobility for Si on (001), respectively. Figures 1.5 and 1.6 show the SO-limited and SR-limited mobility for Ge on (111), respectively. SR-scattering is most important at high densities because the wavefunctions are "squeezed" tightly to the dielectric/substrate interface. The main factor determining the difference in SR-scattering among insulators is the permittivity of the insulator and substrate, see Figs. 1.4 and 1.6. An important factor in the expression for the SR-scattering rate, is the effect of image charges and the interfacial dipoles they induce [4]. This term is proportional to ϱ_s & ϱ_{ins}, where ϱ_s and ϱ_{ins} are the permittivities of the substrate and insulator respectively. The magnitude and even sign of this term is clearly dependent on the insulator and substrate materials considered. Notably, in high-κ materials ($\varrho_{ins} > \varrho_s$), this term acts as a screening component which reduces the strength of SR-scattering (Figs. 1.4 and 1.6). SR- scattering depends on the quality of the fabricated interface. Information about real interfaces, such as can be seen using an atomic force microscope [5], may make SR models more realistic. High-κ effects are more noticeable at lower densities, and hence for small values of the Fermi wavevector k_F, since carriers close to the Fermi surface contribute most to the mobility, and since the SO-scattering strength behaves as 1/q at small q. Instead, at large densities screening by the channel electrons results in an enhanced mobility. So far, the mobility in fabricated Ge MOSFETs has been disappointing [6]. These disappointing results have been attributed to the inability of Hydrogen to passivate the Ge dangling bonds (as is done for Si), resulting in non ideal interfaces with high-κ gate dielectrics and reduced electron mobility [7]. Hence our results set an upper limit on the mobility and comparison to fabricated Ge devices is not yet meaningful.

IV. TEMPERATURE DEPENDENCE

Figures 1.7 and 1.8 show the mobility, respectively, for Si and Ge for T = 77, 300,and 375 K. The left figure, (a), is for SiO_2, and the right, (b), for HfO_2. In both figures, EOT = 1.0 nm, and the sheet density is varied from 2×10^{11} to 2×10^{13} cm^{-2}. For all cases, the mobility increases as the temperature is increased. This is mostly due to the decrease in bulk phonon scattering with decreasing temperature. As the temperature decreases, the population of bulk phonons decreases in accordance with Bose statistics. At $n_s = 2 \times 10^{12}$ the total mobility decreases approximately as T−1.5 for SiO_2 with Si and Ge. For HfO_2, the dependence is closer to T−1 because the low energy SO phonons are easier to excite at low temperatures [8-10]. For lower temperatures, the mobility curves exhibit a large positive slope for smaller sheet densities. This is a consequence of stronger screening of SO phonons by electrons in the channel and a stronger contribution of SO phonons to the overall scattering rate at lower densities. Notice that Si (also Ge) with HfO_2 can exhibit a mobility larger than Si (also Ge) with SiO_2 for large electron sheet densities. This is due to the image term in the SR relaxation rate. For high-κ dielectrics this term can be negative -increasing the total mobility. This is even more noticeable at low temperatures, when the SR limited mobility plays a larger role at $n_s > 5\times10^{12}$ cm^{-2}).

Table 1.1: Mobility and Transconductance degradation for Si.

Gate length (nm)	EOT (nm)	$\Delta\mu$ (%)	Linear Δg_m (%)	Saturated Δg_m (%)
60	2.8	38	50	10
30	1.4	38	44	19
15	0.7	38	30	17

Table 1.2: Mobility and Transconductance degradation for Ge.

Gate length (nm)	EOT (nm)	$\Delta\mu$ (%)	Linear Δg_m (%)	Saturated Δg_m (%)
60	2.8	46	27	8
30	1.4	46	16	3
15	0.7	46	9	1

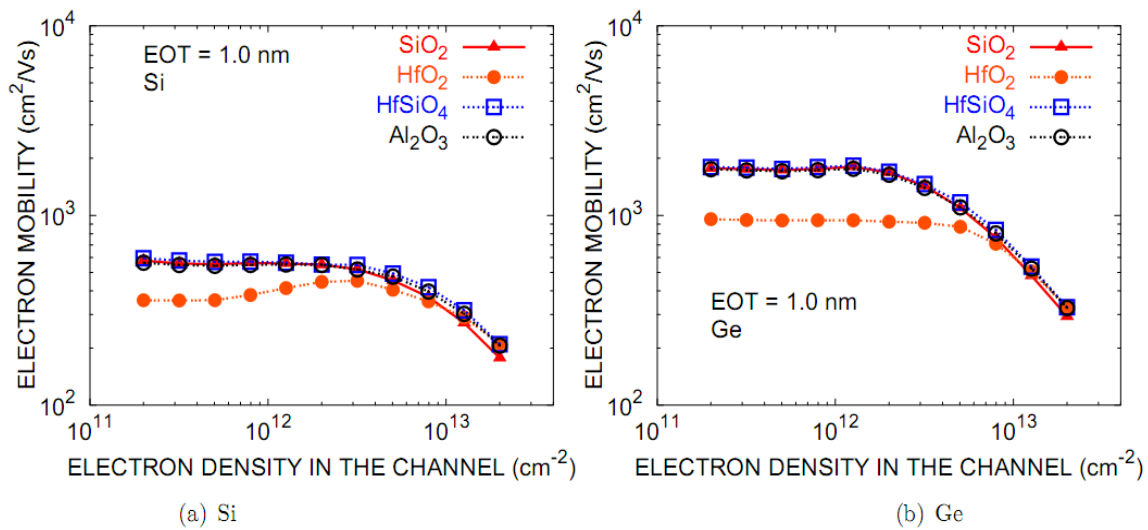

Figure 1.1: Total calculated mobility for Si and Ge substrates with four gate dielectrics: SiO_2, HfO_2, Al_2O_3 and $HfSiO_4$. A substrate doping concentration $N_A = 3\times10^{17}$ cm^{-3} is used throughout this work.

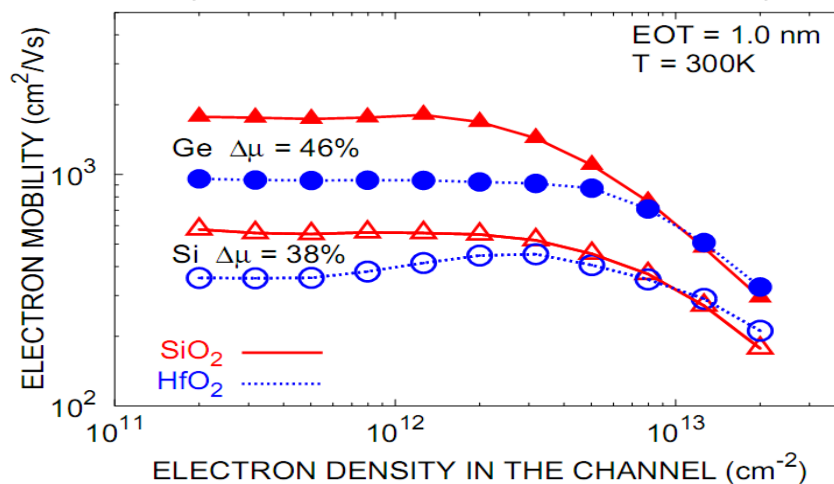

Figure 1.2: Total calculated mobility for Si and Ge substrates with both SiO_2 and HfO_2 gate dielectrics.

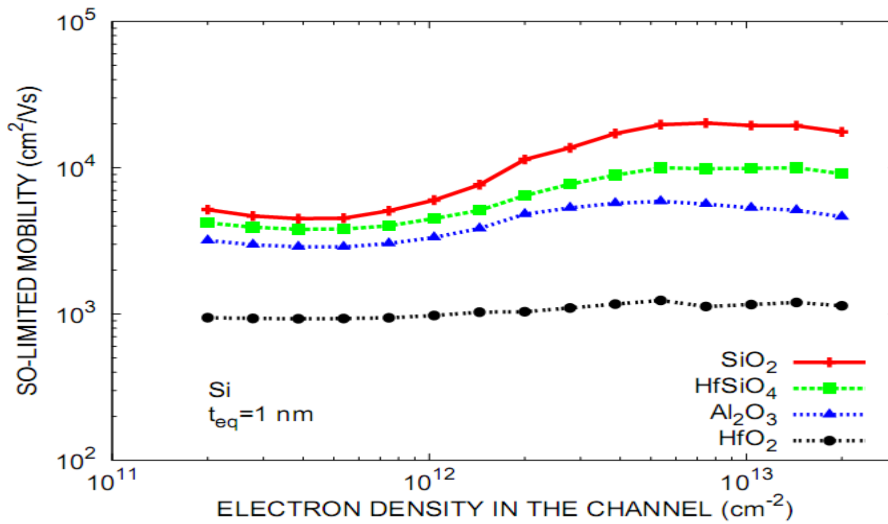

Figure 1.3: SO- phonon limited mobility for Si substrate.

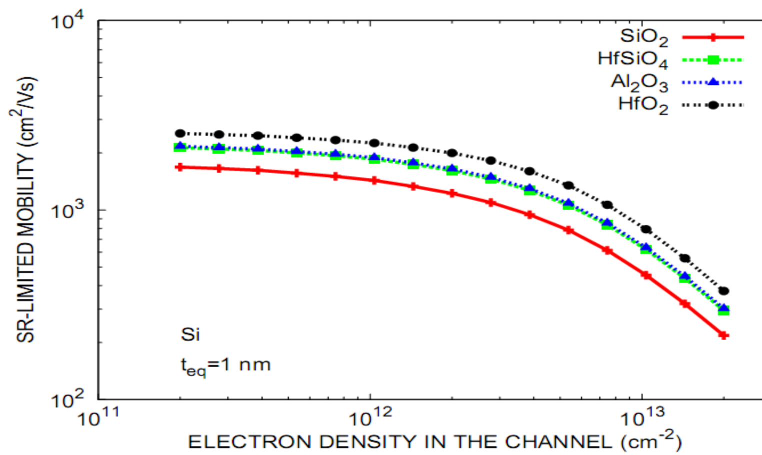

Figure 1.4: Surface roughness limited mobility for Si substrate (using an exponential distribution with step rms height $\Delta = 0.1$ nm and step correlation length $A = 2.5$ nm).

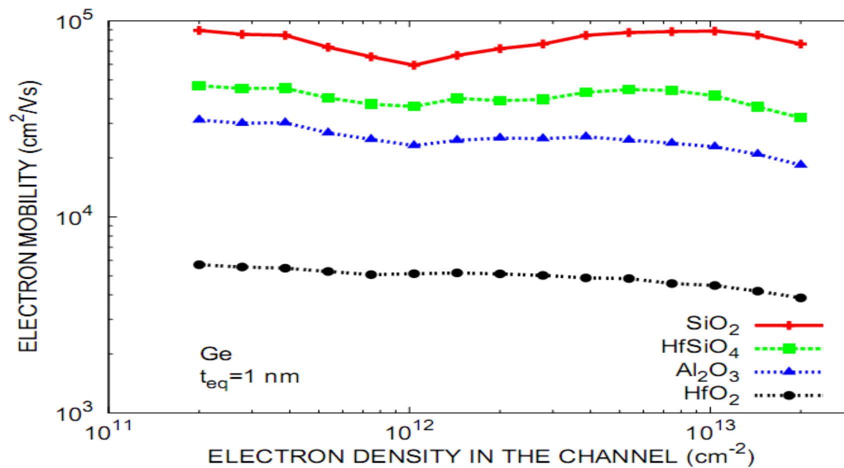

Figure 1.5: SO- phonon limited mobility for Ge substrate.

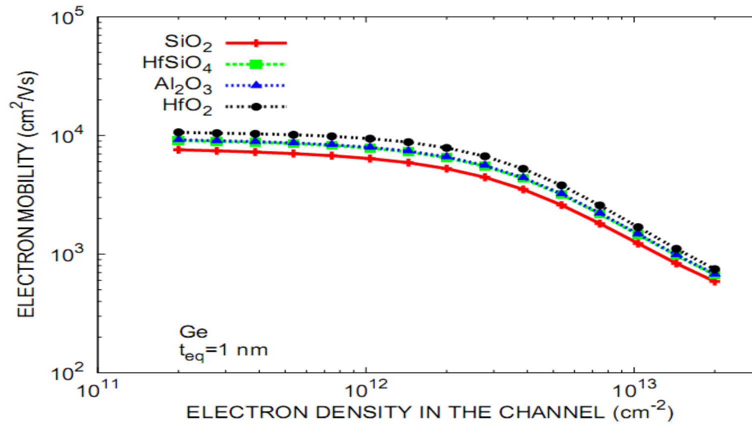

Figure 1.6: Surface roughness limited mobility for Ge substrate (using an exponential distribution with step rms height Δ = 0.1 nm and step correlation length A = 2.5 nm).

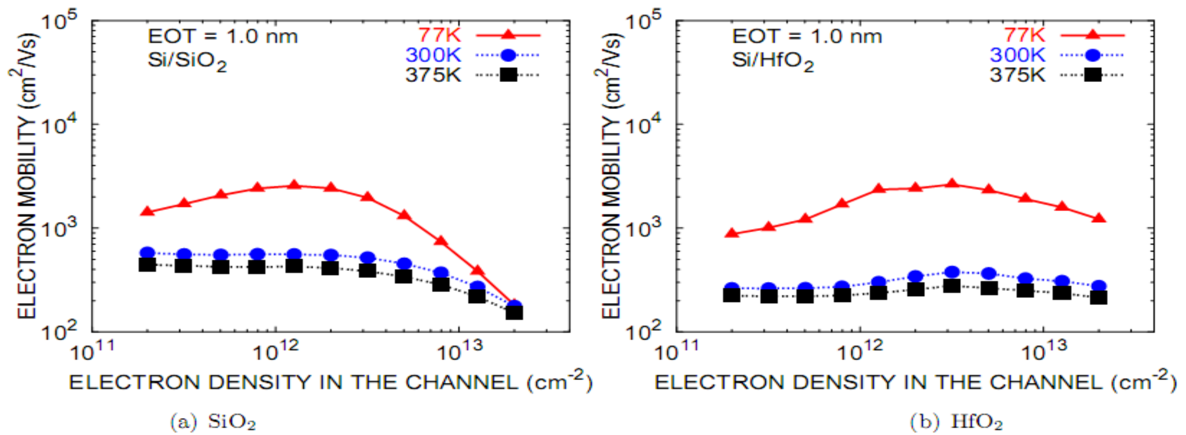

Figure 1.7: Total calculated mobility for Si substrates with both SiO_2 and HfO_2 gate dielectrics as the temperature is varied.

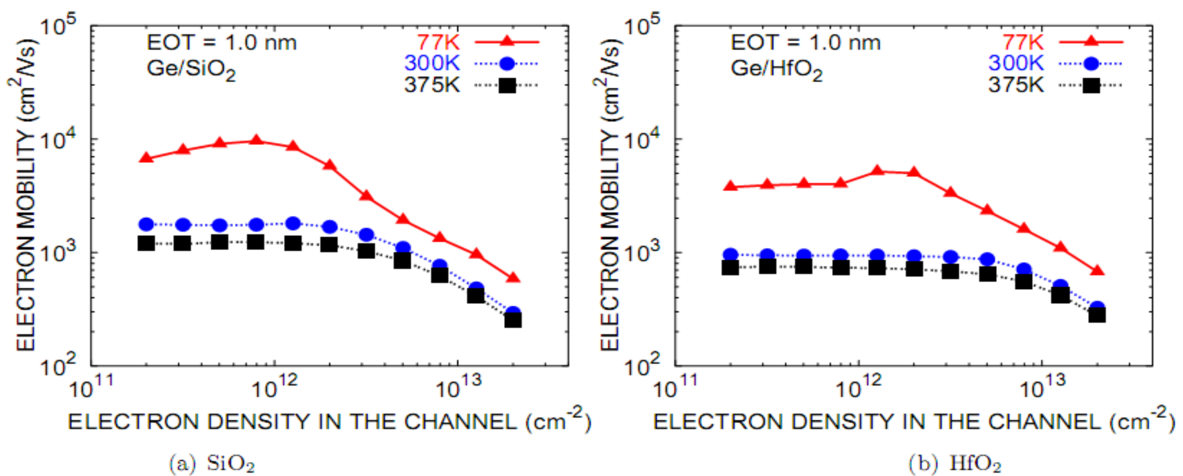

Figure 1.8: Total calculated mobility for Si substrates with both SiO_2 and HfO_2 gate dielectrics as the temperature is varied.

V. CONCLUSIONS

We have computed the electron mobilities for Si and Ge inversion layers including bulk phonons, surface roughness and SO-phonon scattering. Ge outperforms Si but is significantly affected by the introduction of high-κ insulators. Decreasing oxide thickness does not significantly increase remote phonon scattering. HfO_2 yields the lowest mobilities and other materials such as $HfSiO_2$ or Al_2O_3, or AlN should be considered over HfO_2. The low-field electron mobility reduction, due to surface-optical modes associated with high-κ dielectrics, plays less of a role in determining device performance as the gate length is scaled from 60 nm to 15 nm. This is especially true for devices operating in saturation and Ge MOSFETs. HfO_2, the dielectric with the largest dielectric constant and lowest energy SO modes, yields the lowest mobility. Other materials, such as $HfSiO_4$ and Al_2O_3, should be considered a good compromise, yielding mobilities close to SiO_2 while having a larger dielectric constant. A metal gate reduces phonon scattering when compared to a poly-Si gate. The performance gain is expected to be on the order of 10%.

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