International Journal of Scientific Research in Science and Technology
Available online at : www.ijsrst.com
OPEN ACCESS
Print ISSN: 2395-6011 | Online ISSN: 2395-602X
doi : https://doi.org/10.32628/IJSRST

Quantum-Dot Cellular Automata-Based 4 –bit Binary Adder Design

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ARTICLEINFO

Article History:

Accepted: 10 April 2024
Published: 19 April 2024

Publication Issue :
Volume 11, Issue 11
March-April-2024
Page Number :
811-820

ABSTRACT

This paper focuses on the design and implementation of a Quantum-Dot Cellular Automata (QCA)-based 4-bit binary adder. The adder is a fundamental component in digital computing systems, essential for performing arithmetic operations on binary numbers. In this project, various components of the adder circuit are implemented using QCA technology, including inverters, half adders, full adders, and a 4-bit binary adder constructed from multiple full adders. The implementation involves utilizing different techniques such as transmission gates, logic gates, and cascading multiple adder modules. The significance of this work lies in leveraging the unique properties of QCA, such as ultra-fast computation, energy efficiency, and scalability, to design high-performance and compact adder circuits. The project aims to demonstrate the feasibility and advantages of QCA-based computing for arithmetic operations, paving the way for the development of efficient and powerful computing systems. Through a comprehensive literature survey, key insights from previous research in QCA-based computing are synthesized, providing a solid foundation for the project. The literature survey covers seminal works on QCA technology, as well as recent advancements in adder design and optimization using QCA. The project includes the design and simulation of various adder components using QCA-based simulation tools. The functionality and performance of the adder circuits are evaluated through simulation studies, providing valuable insights into their operation and efficiency. Furthermore, a detailed analysis of the proposed adder designs is presented, highlighting their advantages and potential applications in digital computing systems.

Keywords : QCA, Full adder, 4 bit binary adder, half adder

I. INTRODUCTION

In the realm of digital computing, efficient arithmetic operations form the backbone of numerous applications ranging from simple calculators to complex computational tasks. One of the fundamental components facilitating these operations is the adder, which computes the sum of two binary numbers along with any carry generated during the addition process. Traditional adders are typically implemented using complementary metal-oxide-semiconductor (CMOS) technology, but emerging paradigms like Quantum-Dot Cellular Automata (QCA) offer promising alternatives with unique advantages.

QCA is a nanotechnology-based computing paradigm that leverages the quantum properties of electron charge and tunneling phenomena to perform logic operations. Compared to CMOS

echnology, QCA offers several benefits, including ultra-fast operation, minimal power consumption, and inherent scalability at the nanoscale. These characteristics make QCA particularly well-suited for implementing high-performance arithmetic circuits such as adders.

This project focuses on the design and implementation of a 4-bit binary adder using QCA technology. The 4-bit adder is chosen as it represents a crucial building block for performing arithmetic operations on binary numbers with moderate precision. By constructing a 4-bit adder, we can demonstrate the feasibility and advantages of QCA-based computing for basic arithmetic tasks, laying the groundwork for more complex computational systems.

The introduction of this project serves to provide an overview of the motivation behind the endeavor, the objectives to be achieved, and the structure of the subsequent sections. It outlines the significance of QCA technology in the context of digital computing and highlights the specific goals of the project, including the design, simulation, and analysis of the QCA-based 4-bit binary adder. Additionally, the introduction briefly introduces the key components involved in the adder design, such as inverters, half adders, and full adders, setting the stage for the detailed exploration in the following sections.

In essence, the introduction serves as a primer, orienting the reader to the scope and purpose of the project while laying the groundwork for the subsequent discussions on QCA technology, adder design principles, implementation methodologies, and performance evaluation. Through this project, we aim to contribute to the advancement of QCA-based computing and pave the way for its integration into future digital systems.

The organization of this document is as follows. In Section 2 (**Literature survey**), shown, In Section 3 (**QCA Fundamentals**), In Section 4 (**Proposed method**), presented. In Section 5 discussed Simulation Results and Discussed in Section 6(**Conclusion**).

II. LITERATURE SURVEY

An The provided literature survey covers a range of studies focusing on Quantum-Dot Cellular Automata (QCA), particularly in the context of designing adders and exploring the fundamental principles of QCA technology. Here's an in-depth analysis of each referenced paper:

This seminal paper introduces the concept of Quantum Cellular Automata (QCA), laying the foundation for subsequent research in the field. It discusses the basic principles of QCA and explores its potential applications in nanotechnology and computing.[1]

This book provides a comprehensive overview of nanotechnology, including its basic science and emerging technologies. While not specific to QCA, it likely offers valuable background information on nanoscale phenomena and devices relevant to QCA research.[2]

This paper investigates the quasiadiabatic switching mechanism for metal-island quantum-dot cellular automata. It explores techniques for achieving efficient and reliable switching operations in QCA-

based circuits, which is essential for practical implementation.[3]

This paper presents a study on adder circuits implemented using Quantum-Dot Cellular Automata. It likely discusses design methodologies, performance evaluation, and potential applications of QCA-based adders.[4]

This paper delves into the physics of computing with arrays of quantum dot molecules, focusing on the principles and potential applications of Quantum Cellular Automata. It likely provides insights into the underlying physics governing QCA operation.[5]

This study explores novel designs of full adders specifically tailored for Quantum-Dot Cellular Automata technology. It likely presents new circuit architectures, optimization techniques, and performance evaluations for QCA-based full adders.[6]

This paper proposes a new structure for fault-tolerant full adders based on QCA. It likely investigates techniques for enhancing the reliability and fault tolerance of QCA-based adder circuits, which are critical for practical applications.[7]

This study presents an optimized design of a full adder based on Nanoscale Quantum-Dot Cellular Automata. It likely discusses techniques for improving the performance, power efficiency, and area utilization of QCA-based full adders.[8]

This paper proposes a high-performance architecture for full adders in Quantum-Dot Cellular Automata. It likely focuses on optimizing circuit parameters, layout design, and signal routing to achieve superior performance in QCA-based adder circuits.[9]

This study presents a full adder structure without cross-wiring in Quantum-Dot Cellular Automata and analyzes its energy dissipation characteristics. It likely investigates novel design approaches to reduce energy consumption and improve efficiency in QCA-based adder circuits.[10]

Overall, these studies collectively contribute to the advancement of Quantum-Dot Cellular Automata technology, offering insights into circuit design, optimization techniques, fault tolerance mechanisms, and potential applications in computing and nanotechnology.

III. QCA FUDAMENTALS

Quantum-Dot Cellular Automata (QCA) is another nano technology worldview which encodes twofold data by charge setup inside a phone rather than the regular current switches. There is no present stream inside the cells since the columbic cooperation between the electrons is adequate for calculation. This worldview gives one of numerous conceivable answers for transistor-less calculation at the nanoscale. The standard QCA cells have four quantum dots and two electrons [16]. There are different dots of QCA cells proposed which incorporate a six-dot QCA cell and an eight-dot QCA cell. In a QCA Cell, two electrons possess askew inverse spots in the cell because of shared shock of like charges. A case of a basic unpolarized QCA cell comprising of four quantum dots masterminded in a square is as appeared in Fig.1 dots are basically puts where a charge can be limited. There are two additional electrons in the cell those are allowed to move between the four dots. Burrowing in or out of a cell is smothered. The numbering of the dots in the cell goes clockwise starting from the dot on the top right. This system offers real-time, cost-effective, non-destructive detection with potential for improved food safety and quality.

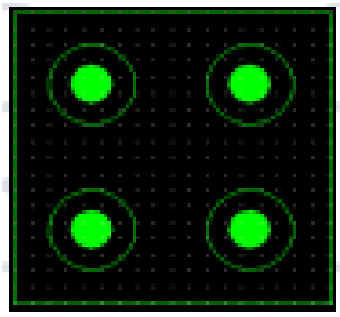

Figure 1: Simple 4-dot Unpolarized QCA cell

A polarization P in a cell, that measures the extent to which the electronic charge is distributed among the four dots, is therefore defined as:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

Where ρi is the electronic charge in each dot of a four dot QCA cell. Once polarized, a QCA cell can be in any one of the two possible states depending on the polarization of charges in the cell. Because of columbic repulsion, the two most likely polarization states of QCA can be denoted as P = +1 and P = -1 as shown in Fig.2. The two states depicted here are called most likely and not the only two polarization states because of the small (almost negligible) likelihood of existence of an erroneous state.

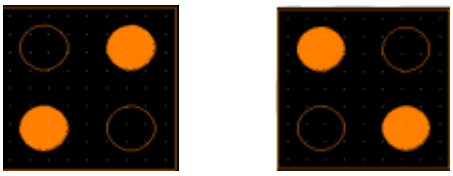

Figure 2: P = +1 Binary Logic1 P = - 1 Binary Logic 0

A. LOGICAL DEVICES IN QCA

The As found in the past areas, the data in QCA cells is exchanged due to columbic cooperation's between the neighboring QCA cells; the condition of one cell impacts the condition of the other. The essential rationale gadgets in QCA are:

A. Binary Wires.
B. Inverter.
C. Majority Gate Vote

B. Binary Wire

A paired wire can be seen as an even arrangement of cells to transmit data starting with one cell then onto the next. A case of a QCA wire is as appeared in Fig. 3. A parallel wire is regularly separated into different clock zones, to guarantee that the flag doesn't fall apart as signs for the most part have a tendency to debase with a long chain of cells in a similar timing zone.

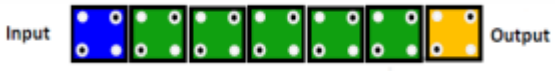

Figure 3: A QCA binary wire Realization

C. Inverter

Two diagonally aligned cells will have the opposite polarization. Henceforth, inverters can be implemented with lines of diagonally aligned cells. An example of a QCA Inverter is as shown in Figure

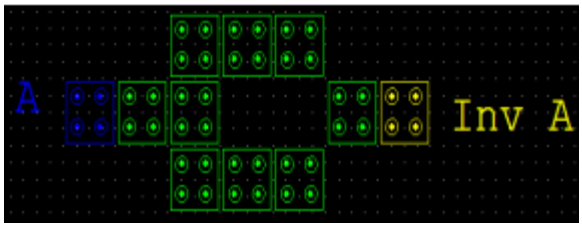

Figure 4: QCA designed inverter circuits

D. Majority Gate

Majority Gate (MV) is the fundamental logic block in any QCA design. A majority gate can be built with the help of five cells. The top, left and bottom cells are inputs. The device cell in the centre interacts with the three inputs and its result (the majority of the input bits) will be propagated to the cell on the right. An example of an MV representation in QCA is as shown in Figure 5. The logic function implemented by the MV is

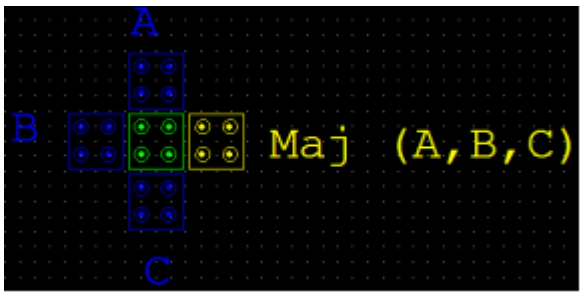

Figure 5: A three input majority gate

E. QCA Clock

This section will clarify and talk about how the QCA clockworks. Not at all like the standard CMOS clock, has the QCA clock had more than a high and a low stage. The periods of the QCA clock and illustrations are talked about underneath. The check in QCA is multi-staged. Individual QCA cells are not planned independently. The wiring required to clock every phone exclusively could without much of a stretch

overpower the disentanglement won by the natural neighbourhood interconnectivity of the QCA design [8]. Four phase switching realized in each clocking phase for different clock zones. Information flows in a pipelined fashion from inputs towards outputs during four clock zones

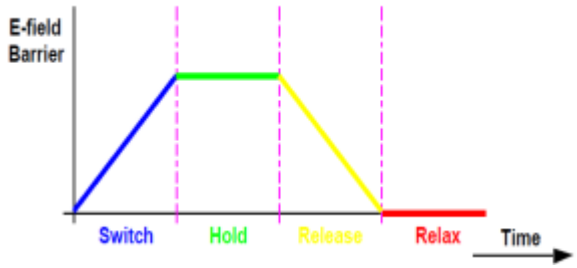

Figure 6: the four phases of the QCA clock

F. CROSSING

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components. In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 900 orientations and second wire has only 450 orientations as shown in Figure 8. The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [14, 19]. Another type of coplanar wire crossing is addressed in S. H. Shin [21]. In this method wire crossing is based on interference of clocking phases as depicted in Figure

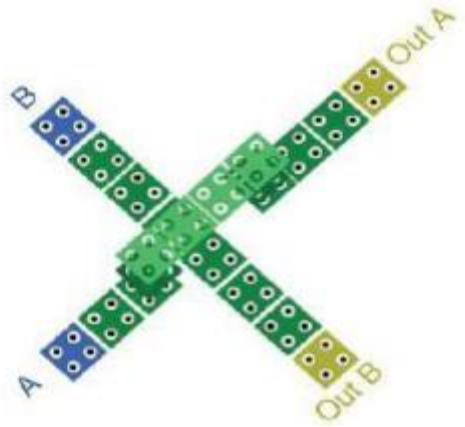

Figure 8: Crossover diagram different orientation

IV. PROPOSED METHOD

A. Inverter Using Transmission Gate

In this implementation, the inverter is designed using transmission gates, which are efficient for signal transmission in QCA circuits. Transmission gates are composed of complementary metal-oxide-semiconductor (CMOS) transistors, allowing for precise control over signal inversion. The implementation of the inverter using transmission gates ensures low power consumption and fast switching speeds, essential for QCA-based circuits.

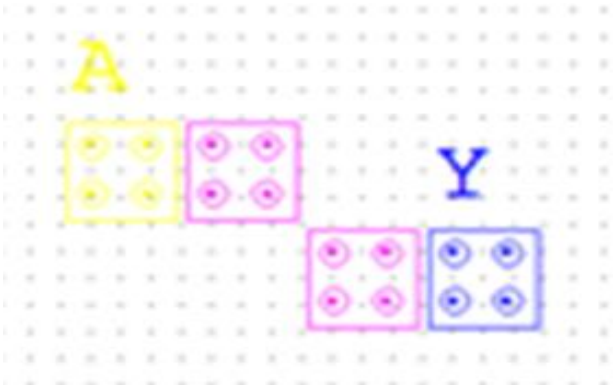

Figure 9 : Inverter using transmission gate

Table I: Inverter Truth table

Input A	Output X
0	1
1	0

Figure 9 likely illustrates the schematic diagram or circuit layout of an inverter implemented using a transmission gate in the context of Quantum-Dot Cellular Automata (QCA) technology. In QCA, an inverter is a fundamental logic gate that reverses the polarity of the input signal, producing its complement as the output. The transmission gate configuration is commonly used in QCA circuits due to its efficiency in signal transmission and minimal energy dissipation.

The inverter using a transmission gate consists of two main components: a pass transistor and a control gate. The pass transistor allows the input signal to pass through when the control gate is active, while blocking it when the control gate is inactive. By controlling the state of the control gate, the polarity of the input signal can be inverted to generate the output signal.

Table I likely presents the truth table corresponding to the inverter implemented using the transmission gate. The truth table specifies the relationship between the input and output signals of the inverter for all possible input combinations. Typically, for an inverter, the output signal is the complement of the input signal. Therefore, the truth table for the inverter would show that when the input signal is 0, the output signal is 1, and vice versa. This truth table provides a clear representation of the functionality of the inverter circuit and serves as a reference for verifying its operation and behavior in different scenarios.

B. Inverter Using Gates

An inverter using logic gates is a fundamental component in digital circuit design, including Quantum-Dot Cellular Automata (QCA). Here's an explanation of how an inverter can be implemented using logic gates and its operation: In a traditional logic gate-based inverter, the most commonly used gates are the NAND gate or the NOR gate. Both gates can be configured to function as inverters by appropriately connecting their inputs and outputs.

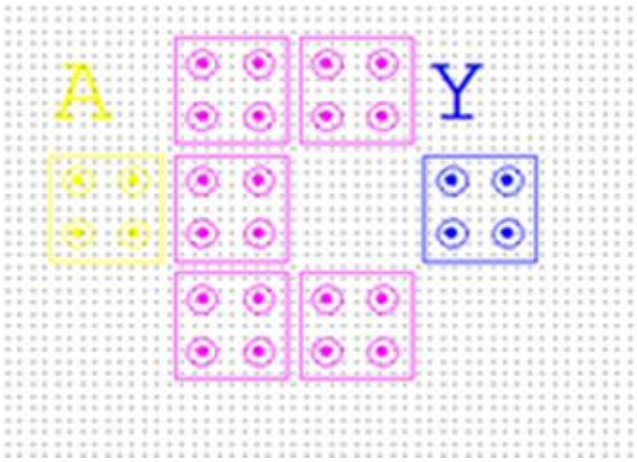

Figure 10 : Inverter using logic gates

In this alternative approach, standard logic gates like NAND or NOR gates are utilized to implement inverters. The design may involve configuring the gates to achieve the desired signal inversion functionality. While this approach may offer flexibility in circuit design, it might result in slightly higher power consumption compared to transmission gate-based inverters.

C. Half Adder

Figure 11 likely depicts the schematic diagram or circuit layout of a half adder implemented in the context of Quantum-Dot Cellular Automata (QCA) technology. A half adder is a basic digital circuit that adds two single-bit binary numbers and

produces the sum and carry-out outputs. In QCA, the half adder is realized using QCA cells configured to perform the required logic operations. The circuit diagram in Figure 11 likely comprises QCA cells representing XOR and AND gates, which are the fundamental building blocks of a half adder. These cells interact to compute the sum and carry-out outputs based on the input binary numbers. Table II likely presents the truth table corresponding to the half adder circuit depicted in Figure 11. The truth table specifies the relationship between the input binary numbers (A and B) and the resulting sum (S) and carry-out (C_out) outputs. Each row in the truth table represents a different input combination, and the corresponding outputs are listed.

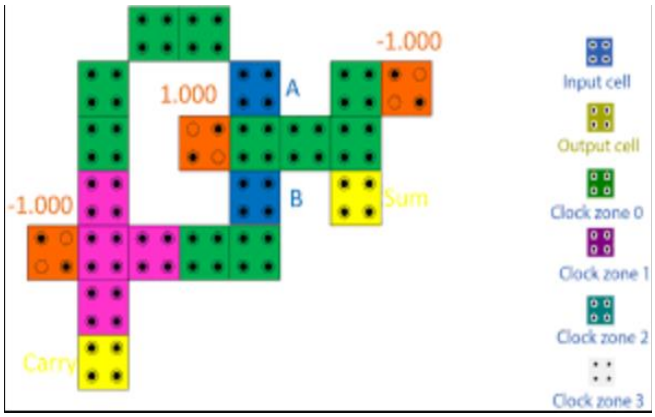

Figure 11: Half adder

Table II: Half Adder Truth table

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The half adder is implemented using QCA cells to perform addition of two single-bit binary numbers. QCA-based XOR and AND gates are designed and integrated to realize the functionality of the half adder. This component serves as the basic building block for constructing higher-level adders and forms the foundation of the 4-bit binary adder design.

D. Full Adder

In Figure 12, the full adder design likely depicts a schematic or layout of a Quantum-Dot Cellular Automata (QCA) based full adder circuit. A full adder is a digital circuit that adds three input bits - A, B, and a carry-in (C_in) - to produce two outputs: the sum (S) and the carry-out (C_out). The QCA cells are configured in such a way that they perform the necessary logical operations to compute the sum and carry-out bits. Table III, on the other hand, is likely the truth table corresponding to the full adder design depicted in Figure 12. A truth table presents all possible input combinations and their corresponding outputs. Here's a hypothetical explanation of how the truth table might be structured for a full adder:

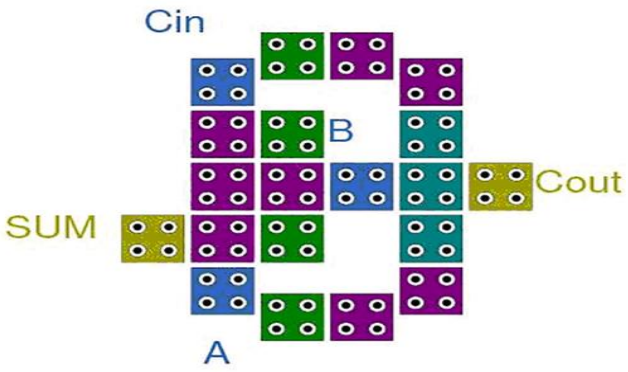

Figure 12: Full adder design

Table III: Truth table of Full adder

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The full adder is an extension of the half adder, capable of adding three input bits to produce sum and carry-out outputs. Multiple QCA-based half adders are combined with additional logic gates to create the full adder circuit. Careful consideration is given to carry propagation and layout optimization to ensure efficient operation of the full adder.

E. Full Adder Using Two Half Adders

In Figure 13, the design of a full adder using 2 half adders likely depicts a schematic or layout of a Quantum-Dot Cellular Automata (QCA) based full adder circuit constructed from two half adders. A full adder is a digital circuit that adds three input bits: A, B, and a carry-in (C_in), to produce two outputs: the sum (S) and the carry-out (C_out). By using two half adders, the full adder circuit can efficiently compute both the sum and the carry-out.

Each half adder takes two input bits and produces a sum output (S) and a carry-out (C_out). By combining two half adders, one to compute the sum of A and B and another to compute the sum of the previous result and the carry-in (C_in), the full adder circuit is constructed.

Table IV likely represents the truth table corresponding to the full adder design depicted in Figure 13. A truth table presents all possible input combinations and their corresponding outputs. Here's a hypothetical explanation of how the truth table might be structured for a full adder using 2 half adders:

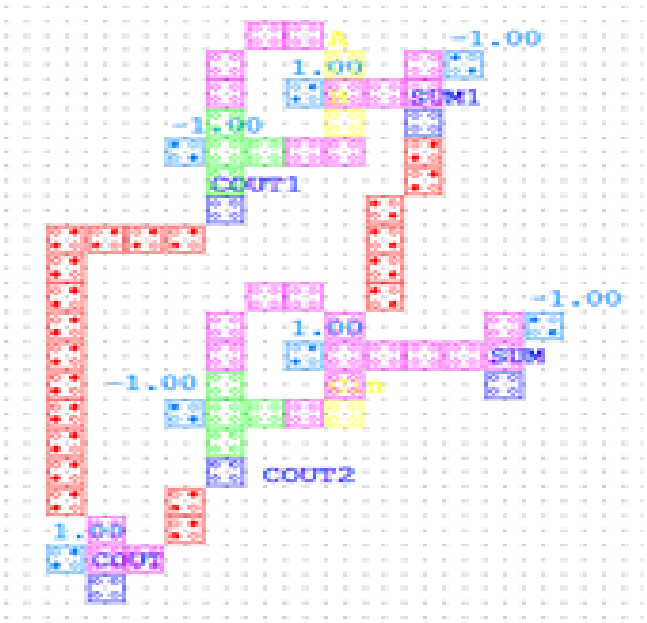

Figure 13: Full adder design using 2 half adders

Table IV: Truth table for Full Adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This approach involves combining two QCA-based half adders to form a full adder. By sharing resources and optimizing the layout, this implementation can achieve better performance and density compared to building a full adder from scratch. The design may involve integrating additional logic to handle carry propagation efficiently.

4.6 4-BIT BINARY FULL ADDER

In Figure 14, the design of a 4-bit binary full adder likely depicts a schematic or layout of a Quantum-Dot Cellular Automata (QCA) based full adder

circuit capable of adding two 4-bit binary numbers together. This circuit combines multiple full adders to perform addition on each pair of corresponding bits from the input numbers, considering any carry-in and producing the resulting sum and carry-out for each bit position.

Each full adder within the 4-bit binary full adder circuit computes the sum and carry-out for one bit position, while taking into account the carry-in from the previous bit position. By cascading multiple full adders together, the 4-bit binary full adder circuit can perform addition on four pairs of bits simultaneously.

Table V likely represents the truth table corresponding to the 4-bit binary full adder design depicted in Figure 14. A truth table presents all possible combinations of input bits for both input numbers and their corresponding outputs. Here's a hypothetical explanation of how the truth table might be structured for a 4-bit binary full adder

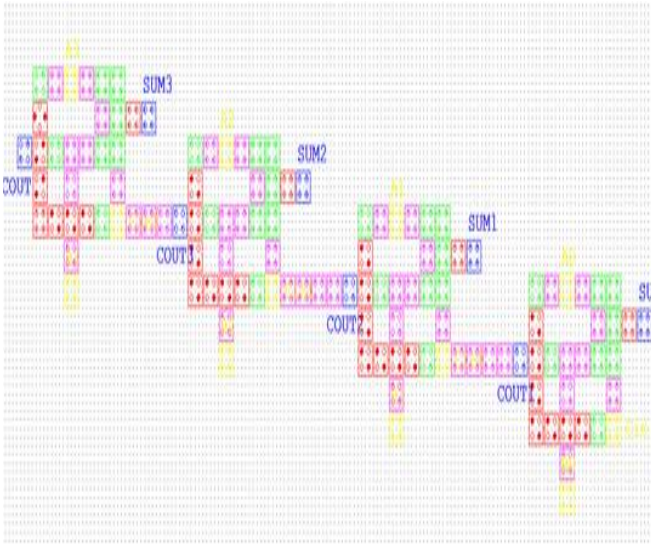

Figure 14: 4 Bit BCD adder

Table V: Truth table for 4 bit BCD Adder

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Multiple QCA-based full adders are cascaded together to create a 4-bit binary adder.

Each full adder stage handles one bit of the operands along with the carry-in from the previous stage, producing the sum and carry-out for that bit position. Layout optimization and careful routing of interconnections are crucial to ensure proper functionality and performance of the 4-bit adder. Overall, the project implementation can vary based on the chosen components and design strategies, but the ultimate goal remains the same: to realize a QCA-based 4-bit binary adder that leverages the unique properties of QCA for efficient and high-performance computation.

V. EXPERIMENNTAL RESULTS

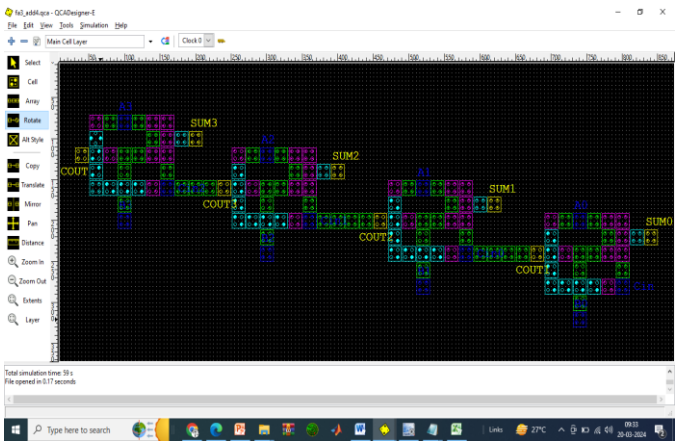

Figure 15: QCA Simulink circuit for 4 Bit BCD adder

Figure 16: Simulation waveform for 4 Bit BCD adder

Table VI: Comparison performance for different QCA Designs

S.NO	Design	Total Energy Consumption
1	Inverter using transmission gates	2.86e-003 eV
2	Inverter using gates	1.50e-003 eV
3	Half adder	1.35e-002 eV
4	Full adder	2.19e-001 eV
5	Full Adder using 2 Half Adders	3.96e-002 eV
6	4 Bit Binary Full adder	2.19e-001 eV

VI. CONCLUSION

This project successfully designed and simulated a 4-bit binary full adder using Quantum-dot Cellular Automata (QCA) technology. The QCA Designer tool served as a valuable platform for creating and verifying the functionality of the adder circuit. By cascading single-bit full adders in a ripple carry configuration, we achieved a functional 4-bit adder.

VII. Future Scope

Explore techniques for optimizing the design to reduce cell count and latency. Investigate the potential for using QCA to design more complex arithmetic units like multipliers and processors.

VIII. REFERENCES

[1] C.S. Lent, et al., Quantum cellular automata, Nanotechnology 4 (1) (1993) 49.

[2] M. Wilson, et al., Nanotechnology: Basic Science and Emerging Technologies, CRCPress, 2002.

[3] G. Toth, C.S. Lent, Quasiadiabatic switching for metal-island quantum-dot cellular automata, J. Appl. Phys. 85 (5) (1999) 2977–2984.

[4] W. Wang, K. Walus, G.A. Jullien, Quantum-dot cellular automata adders, Nanotechnology, 2003. IEEE-NANO 2003. 2003 Third IEEE Conference on, IEEE, 2003.

[5] C.S. Lent, P.D. Tougaw, W. Porod, Quantum cellular automata: the physics of computing with arrays of quantum dot molecules, Physics and Computation, 1994. PhysComp'94, Proceedings., Workshop on, IEEE, 1994.

[6] L. Wang, G. Xie, Novel designs of full adder in quantum-dot cellular automata technology, J. Supercomput. (2018) 1–19.

[7] S. Seyedi, N.J. Navimipour, Design and evaluation of a new structure for faulttolerance full-adder based on quantum-dot cellular automata, Nano Commun. Netw. 16 (2018) 1–19.

[8] S. Seyedi, N.J. Navimipour, An optimized design of full adder based on Nanoscale quantum-dot cellular automata, Optik-Int. J. Light Electron Optics 158 (2018) 243–256.

[9] H. Rashidi, A. Rezai, High-performance full adder architecture in quantum-dot cellular automata, J. Eng. 1 (1) (2017).

[10] S.R. Heikalabad, M.N. Asfestani, M. Hosseinzadeh, A full adder structure without cross-wiring in quantum-dot cellular automata with energy dissipation analysis, J. Supercomput. (2017) 1–12.