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Study of Voltage Reference in Analog Circuit

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ABSTRACT

In this paper, we present the study of voltage reference in analog circuits. A voltage reference is an important part of any analog integrated circuit. Transistors in analog integrated circuits must have stable bias currents in order to have stable transconductances. Stable voltage references are usually required to generate these bias currents and are also used in other parts of analog circuits. For an analog circuit to operate reliably, the reference voltage provided to the circuit must be stable over a wide range of temperatures and power supply voltages. This chapter surveys various voltage reference topologies reported in literature and chooses the one which is most appropriate for our application of a fully implantable device (recording system). Transistor and component sizing is carried out, and simulation and test results are reported.

Keywords : FIRS, Electrical Component, MUX, Noise.

1. VOLTAGE REFERENCE CONCEPTS

An ideal voltage reference circuit will supply a fixed DC voltage of known amplitude that stays constant with changing temperature or external power supply voltage. Several approaches have traditionally been used for accomplishing this, including: using a reverse biased zener diode in breakdown mode, subtracting the threshold voltages of an enhancement transistor and a depletion transistor, and eliminating the negative temperature dependence of a p-n junction with the positive temperature dependence generated by a proportional to absolute temperature (PTAT) circuit. The last approach is the most popular, and is used in all of the circuit topologies considered here, so it will be discussed in this section. A block diagram of standard bandgap voltage reference circuit is shown in Figure 1, with the two voltage components which are added together to form the voltage reference. The first component of the voltage reference is the base-emitter voltage of a forward biased bipolar transistor [1-5].

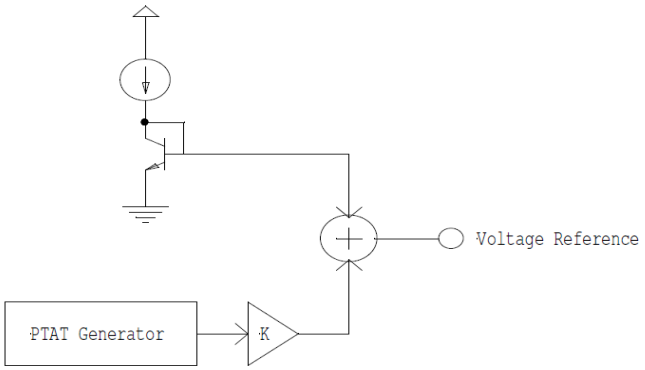

Figure 1 : Bandgap voltage reference block diagram (K is a multiplier for the PTAT component)

The I-V relationship for this voltage is given by:

$$I_C = I_S.e^{q.V_{BE}/K.T} \quad (1)$$

Here I_C is the collector current of the transistor, I_S is the scale current, and V_{BE} is the base-emitter voltage. It can be shown that for constant I_C, V_{BE} has a -2.2 mV/°K temperature dependence at room temperature (25°C).

The second component is the PTAT voltage, which can be formed by subtracting the base-emitter voltages of two base-emitter junctions biased at different current densities. We can show that the result of this subtraction
is

$$\Delta V_{BE} = \frac{k.T}{q} . \ln \left(\frac{J_2}{J_1}\right) \quad (2)$$

which clearly has a positive temperature co-efficient (J_1 and J_2 are the current densities of the base-emitter junctions). The result of adding these components is

$$V_{ref} = V_{BE}^2 + K. \Delta V_{BE} \quad (3)$$

where K is a scaling constant that is adjusted to achieve zero temperature dependence at a specific temperature. This is the basic structure of the majority of the voltage reference circuit topologies that are discussed here. For a more thorough review of bandgap voltage reference concepts. Most of the designs use bipolar transistors available in CMOS processes to realize the PTAT block, although MOS transistors operating in weak inversion and diodes are also used. While this basic design compensates for the linear temperature dependence of a base-emitter voltage, some designs use more complex circuitry to compensate for the quadratic temperature dependence and thereby achieve reduced voltage variations over a larger temperature range [6].

2. VOLTAGE REFERENCE REQUIREMENTS

The most important requirement for a voltage reference in a fully implantable recording system is that it be stable over a wide range of power supply voltages. Assuming the system is powered by an inductive link, the coupling of the link will vary if the internal and external coils shift relative to each other, so variations in the supply voltage received by the voltage reference circuit will be likely. The other standard voltage reference requirement of being stable over a range of temperatures is not as important for a fully implanted system, since the circuit will remain at approximately 37° C (body temperature). Other requirements for the voltage reference are that it be of minimal size and complexity, and that it consume very little power. The area requirement stems from the need to keep the entire implantable unit as small as possible to limit trauma caused by implantation, and the power requirement arises from the need to limit heating effects on the tissue surrounding the implant. Additional requirements for the voltage reference are that it should be possible to fabricate it in a standard CMOS process, and it should not require any special post-processing techniques (i.e., laser trimming, etc.) to achieve the desired results [7].

3. VOLTAGE REFERENCE TOPOLOGIES

The first design considered is unique in that it makes use of MOS transistors operating in weak inversion to realize the PTAT component of the reference [8]. This is possible since the IV characteristics of a MOS transistor in weak inversion is described by

$$I_D = I_{DO}. (W/L).e^{(q.VGS/n.k.T)} \quad (4)$$

where I_D is the drain current of the MOS transistor, I_{D0} is an intrinsic unit current, V_{GS} is the gate source voltage, and n is the slope factor. This is an exponential relationship similar to that of the bipolar transistor that is normally used. One drawback of this design is that the base-emitter voltage component is generated from an *npn* bipolar transistor which requires a p-well process or an additional p-base layer. This additional layer is not available in most standard CMOS processes, so fewer processes can be used for implementation of the circuit. The second design reviewed makes use of lateral bipolar transistors rather than the vertical ones used in most designs [9]. The advantage of using lateral transistors is that they do not need to have the collector tied to the substrate

(as is the case with standard vertical BJT transistors), which allows greater design flexibility. The lateral transistors used in this design can be realized by biasing the gate of a MOS transistor well below its threshold voltage so that an accumulation layer forms (preventing normal MOS transistor operation), and properly biasing the other terminals to obtain a bipolar operating mode. The drawback of this approach is the negative gate voltage required for proper operation. An alternative means of creating a lateral bipolar transistor is to use an additional layer (p-base), however, this layer is not available in most CMOS processes. This design improves on the traditional design by reducing the contribution of the amplifier offset voltage to the final voltage reference. The offset voltage is not PTAT and thus cannot be compensated for, so it is one of the major causes of error in a traditional voltage reference circuit. The third design creates a voltage reference that is floating, instead of being set with respect to the positive or negative supply [10]. As a result, the common mode value of the reference must be set by a common mode feedback circuit (CMFB), so this design would be useful in a system where the voltage reference has to interface with other differential circuit blocks that already have CMFB circuits. The extra circuitry required for the floating reference adds complexity, and since this would not provide an advantage in our application, this design will not be considered further.

The fourth design has been optimized to minimize all sources of error and realize a very precise voltage reference [11]. In addition to the standard PTAT correction voltage, this design makes use of a quadratic ($PTAT^2$) temperature correction voltage to minimize the temperature drift. This design employs a complicated two step trimming procedure where both capacitor arrays and resistor strings are trimmed to achieve 12-bit accuracy in the reference voltage. This circuit has the highest complexity of all of the designs reviewed here. The next design reviewed is similar to the previous one in that it adds an additional voltage component to compensate second order temperature variations not accounted for by the standard PTAT correction term. It differs in that it uses current-mode correction to allow operation with supply voltages down to 1.1 V [12]. A p-base layer is required to create bipolar transistors with collectors not connected to the substrate, and it makes use of a JFET in its start-up circuit (a device that is not available in standard CMOS processes). It also makes use of a complex multi-step trimming procedure to achieve a zero-temperature coefficient at the desired temperature. The sixth design is a low voltage design that uses current-mode operation to allow lower supply voltages [13]. In simulations, the circuit had an output of 0.84V, which is lower than a conventional bandgap reference voltage by 0.46V. This design requires that native NMOS transistors be available, since the threshold voltages of enhancement mode NMOS transistors are too high to achieve the low voltage operation. The last design reviewed uses a simple circuit topology which does not require an opamp (as most traditional designs do), while allowing low supply voltages and providing a good power supply rejection ratio (PSRR) [14].

4. CONCLUSIONS

This design does not make use of any additional layers, and the base-emitter voltages are realized by bipolar transistors that can be implemented in any n-well CMOS process. Some advantages of this design are that it achieves good results without trimming, and the circuit has a low level of complexity.

An additional advantage is that part of the circuit regulates the supply voltage down to a lower controlled voltage, so the output will remain stable for changing power supply voltages. The performance and features of each voltage reference reviewed is summarized in Table 1. The final design will choose for implementation since it come the closest to meeting the requirements outlined and present in next paper.

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