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Study of Analog Circuit Design, Simulation and Experimental Verification of Voltage Reference

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ABSTRACT

In this paper, we present the study of study of analog circuit design, simulation and experimental verification of voltage reference. A voltage reference is an important part of any analog integrated circuit design.

Keywords : FIRS, Electrical Component, MUX, Noise.

1. INTRODUCTION

Voltage reference concept, voltage reference requirement, and voltage reference topologies are explained clearly in our previous paper. In this part of paper, we continued accordingly and design a circuit, simulate the process of voltage reference concept and experimentally verified them. The first component of the voltage reference is the base-emitter voltage of a forward biased bipolar transistor [1-5].

The I-V relationship for this voltage is given by:

$$I_C = I_S . e^{q.V_{BE}/K.T} \quad (1)$$

Here I_C is the collector current of the transistor, I_S is the scale current, and V_{BE} is the base-emitter voltage. It can be shown that for constant I_C, V_{BE} has a -2.2 mV/°K temperature dependence at room temperature (25°C).

The second component is the PTAT voltage, which can be formed by subtracting the base-emitter voltages of two base-emitter junctions biased at different current densities. We can show that the result of this subtraction is

$$\Delta V_{BE} = \frac{k.T}{q} . \ln\left(\frac{J_2}{J_1}\right) \quad (2)$$

which clearly has a positive temperature co-efficient (J_1 and J_2 are the current densities of the base-emitter junctions). The result of adding these components is

$$V_{ref} = V_{BE^2} + K. \Delta V_{BE} \quad (3)$$

where K is a scaling constant that is adjusted to achieve zero temperature dependence at a specific temperature.

2. CIRCUIT DESIGN

This section provides details on the design carried out for the chosen circuit topology. The approach taken for the transistor sizing was to choose a value for the currents in the important circuit branches, then choose resistor sizes and device ratios to achieve a zero

*Temperature coefficients and power supply coefficients cannot be compared directly since different papers used different temperature and voltage ranges in measuring them temperature coefficient at 37°C, and then choose transistor sizes to ensure that all devices are in the active region. The core of the bandgap circuit is shown in Figure 1.

Here N is the ratio of the widths of MOS transistors M_1 and M_3, and M is the ratio of the emitter areas of bipolar transistors Q_2 and Q_1.

Table 1: Comparison of reviewed voltage reference topologies

Design	Implementable in Standard CMOS Process	Post-Processing Required	Complexity	Stability for Changing Power Supply*	Temperature Coefficient*
(10)	No	No	Low	N/A	70 ppm/°C (0°C to 65°C)
(11)	No	Yes	Low	N/A	23 ppm/°C (0°C to 70°C)
(12)	Yes	No	High	N/A	21 ppm/°C (0°C to 100°C)
(13)	Yes	No	High	N/A	13 ppm/°C (0°C to 70°C)
(14)	No	Yes	Moderate	408 ppm/V (1.2V to 10V)	20 ppm/°C (15°C to 90°C)
(15)	No	No	Low	1080 ppm/V (2.2V to 4V)	59 ppm/°C (27°C to 125°C)
(16)	Yes	No	Low	N/A	85 ppm/°C (-40°C to 85°C)

Additional feedback circuitry (not shown in this schematic, see Figure 1 for details) forces the voltage at *Node1* to equal the voltage at *Node2*, in turn forcing the currents in M_1 and M_2 to be equal. Using these conditions, the bandgap voltage V_{BG}, is derived as:

$$V_{BG} = V_{BE2} + N \times \frac{R_1}{R_2} \times \ln [M \times (N+1)] \times V_T \quad (4)$$

Here V_{BE2} is the base-emitter voltage of bipolar transistor Q_2, which has a temperature coefficient of -2.2 mV/°C at 25°C, and V_T is the thermal voltage, which has a temperature coefficient of +0.085 mV/°C. Taking the derivative of (5) with respect to temperature, setting it equal to zero, and substituting in the temperature coefficients, we arrive at the following equation for the transistor sizes and device ratios:

$$N \times \frac{R_1}{R_2} \times \ln [M \times (N+1)] = 25.88 \quad (5)$$

Choosing $M = 9.5$ and $N = 4$ in this equation, we get $R_2/R_1 = 1.78$. So, choosing $R_1 = 10$ kΩ, we calculate that $R_2 = 17.8$ kΩ.

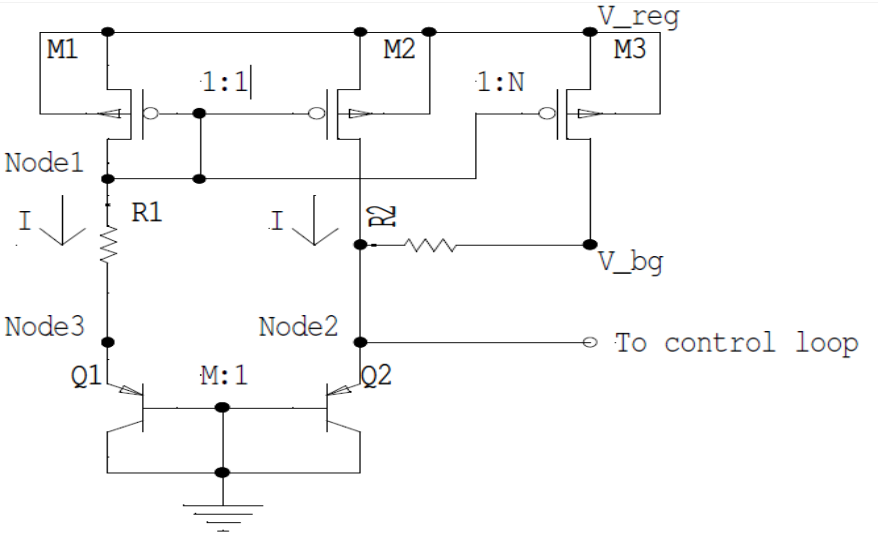

Figure 1: Schematic of bandgap voltage reference circuit core

Figure 1 shows the complete schematic. The next step was to choose a drain current for M_1 and M_2. A current of 10 µA was chosen to minimize power consumption. The next step was to perform steady state calculations for all the nodes of the circuit and adjust sizing and ratios to ensure that all devices were in the active region. The default sizing for transistors was W/L = 19.2 µm/6.4 µm, to provide good matching between devices. The final sizing for all devices is shown on the schematic in Figure 1. Note that some of the device sizes differ from those calculated above, due to optimizing after simulations were run.

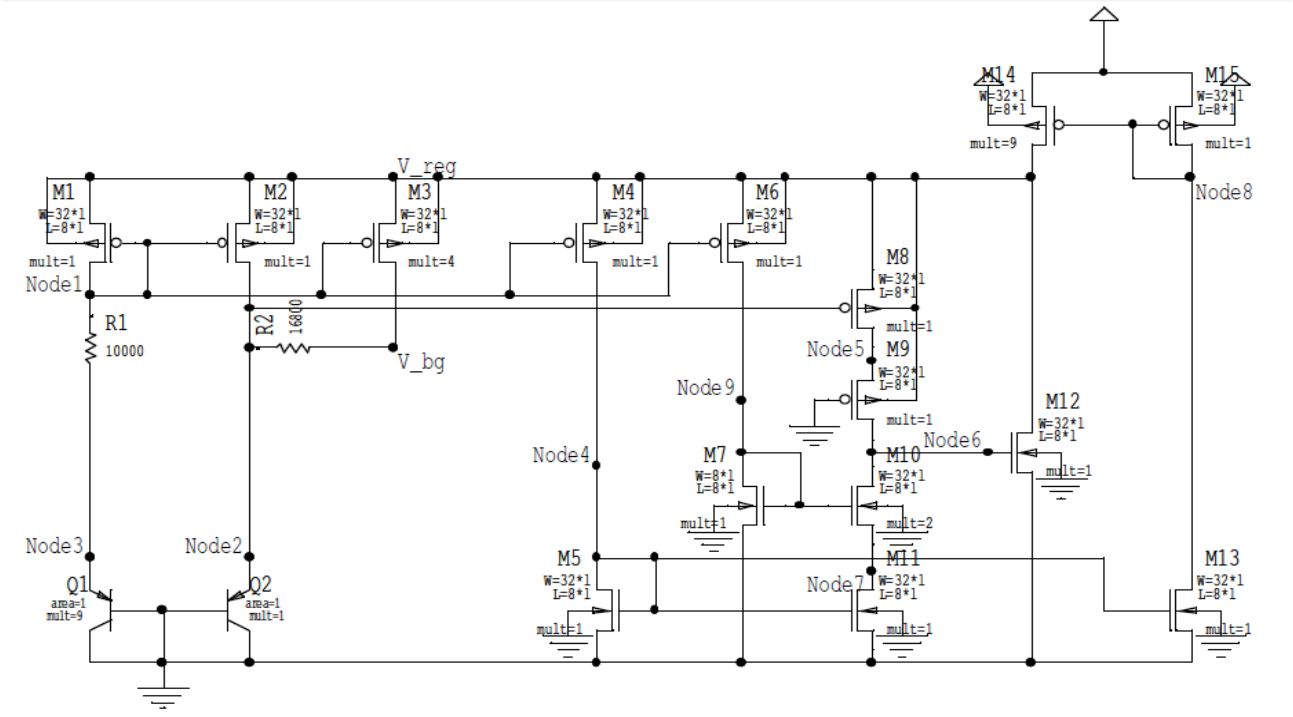

Figure 2: Complete schematic of bandgap voltage reference (l = λ = 0.8µm)

3. SIMULATION RESULTS

Accurate simulation results were difficult to obtain before a chip was fabricated, because an accurate value for the resistance of the poly resistors was not known, and accurate parameters for the bipolar junction transistors (BJTs) were not available. Simulations were carried out using approximate resistance values and BJT parameters, but they did not accurately reflect the test results. After testing and characterizing the chip, actual resistance

values and BJT parameters were extrapolated from the test data, and the circuits were re-simulated. This simulation data matched the measured data very closely and is the data that is reported here as revision 1.

Another version of the chip was then fabricated, using the test and simulation data from the first revision to lay out resistors with more accurate values. This version had large performance improvements over the first revision, and the results for this design are listed as revision 2. Results of the temperature simulations are shown in Figure 8. The resistor ratio R_2/R_1 in the first revision was too high, but test results allowed a more accurate ratio for the second revision. Characterization of the first revision revealed that the value of the resistor R_2 in the first revision was 14 kΩ, which is significantly greater than the target resistance of 6.8 kΩ. These resistor values differ from the calculated values in the previous section, which were estimated using approximate BJT parameters. For the second revision, five voltage reference layouts were created, with target resistances of 6.4, 6.6, 6.8, 7.0, and 7.2 kΩ in an attempt to bracket the desired value of 6.8 kΩ. The temperature simulation for the second revision uses the resistance of 6.8 kΩ, and it can be seen from Figure 8 that the temperature variance is much smaller than for the first revision. Revision one varies by 41 mV over the temperature range simulated (1353 ppm/°C), while revision two varies by 3.6 mV over the temperature range (169 ppm/°C). Power supply simulations were also carried out on the voltage references. Both revisions required a minimum supply voltage of 3 V to produce a stable output voltage. For the supply voltage ranging from 3 V to 10 V, revision 1 varied by 19.5 mV (1873 ppm/V), while revision 2 varied by 2 mV (268 ppm/V), a significant improvement.

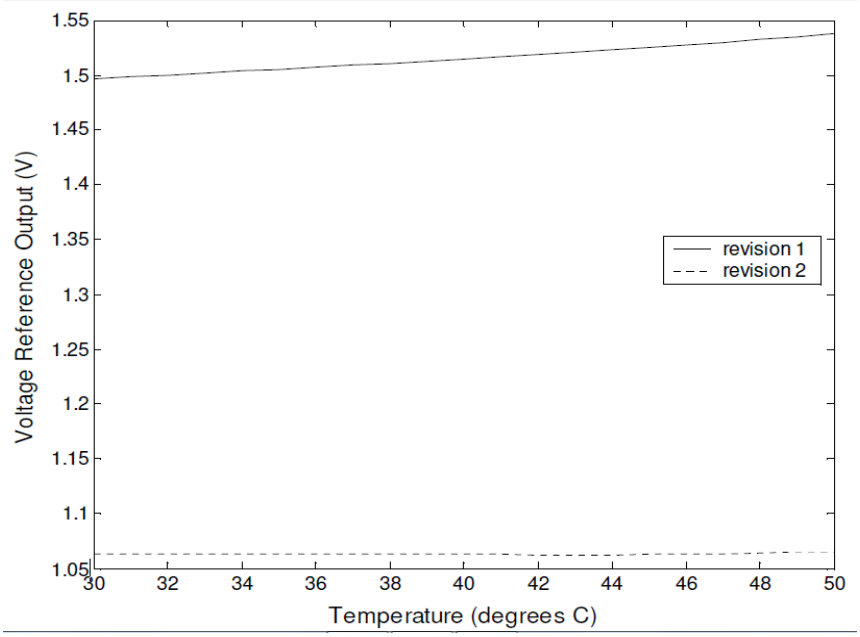

Figure 3: Temperature simulation for voltage references

The power supply rejection characteristics of the voltage references were also simulated. This is an important parameter for a voltage reference in FIRS, since the power is transmitted through an inductive link and it is likely that there will be some variance in the supply voltage. Over the simulated range from 1 kHz to 100 kHz, the power supply rejection ratio (PSRR) of revision 1 varied from -70 dB to -56 dB, while the PSRR for revision 2 showed significant improvement, varying from -83 dB to -62 dB.

4. EXPERIMENTAL RESULTS

A photograph of the test chip including the voltage reference is shown in Figure 4. The voltage reference is contained within the white box in the lower right-hand corner of the chip. The layout for all of the revisions is the same except for the size of R_2.

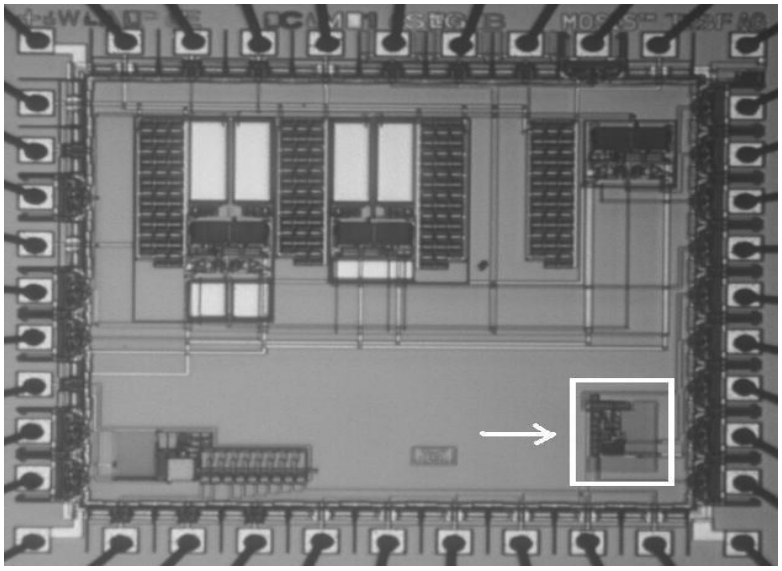

Figure 4: Voltage reference test chip photograph (layout of voltage reference is contained in the white box in the lower right-hand corner)

As mentioned in the previous section, only one version of the voltage reference was fabricated for the first revision, but for the second revision there were five versions fabricated, one with the target resistance, and two for bracketing purposes on either side. Figure 5 shows the test results for the temperature variance of the voltage references. The revision 1 voltage reference had a variation of 38 mV over the temperature range from 30°C to 50°C, for a temperature coefficient of 1278 ppm/°C. The revision 2 voltage references had variations ranging from 2 mV to 3.5 mV, and temperature coefficients ranging from 94 ppm/°C to 165 ppm/°C. The temperature coefficients of each of the versions of the revision 2 voltage reference did not match the simulation results exactly, this is likely due to the ~20% tolerance on poly resistors in this process, which means that the coefficient with the middle resistance of 6.8 kΩ could be as high as 8.2 kΩ or as low as 5.4 kΩ, which is a much greater range than the range of designed resistances. Figure 6 shows the output voltages for each of the voltage references plotted against the power supply voltage.

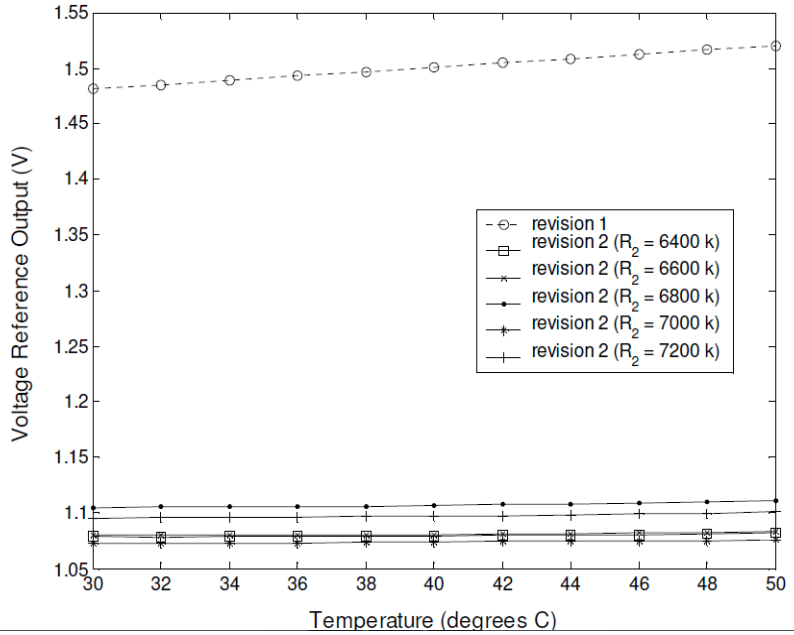

Figure 5: Measured voltage reference output variations with changing temperature

The revision 1 voltage reference has a minimum supply voltage of 3.3 V, while the minimum supply voltage for the revision 2 voltage references varies from 3.4 V to 3.7 V. The variation in the output for supply voltages from 3.8 V to 10 V was 66 mV (7108 ppm/V) for revision 1, and ranged from 48 mV to 55 mV (7138 ppm/V to 7930 ppm/V) for revision 2. The output variations for changing supply voltages were much greater in the experimental results than in the simulated results (see Table 2 for a comparison).

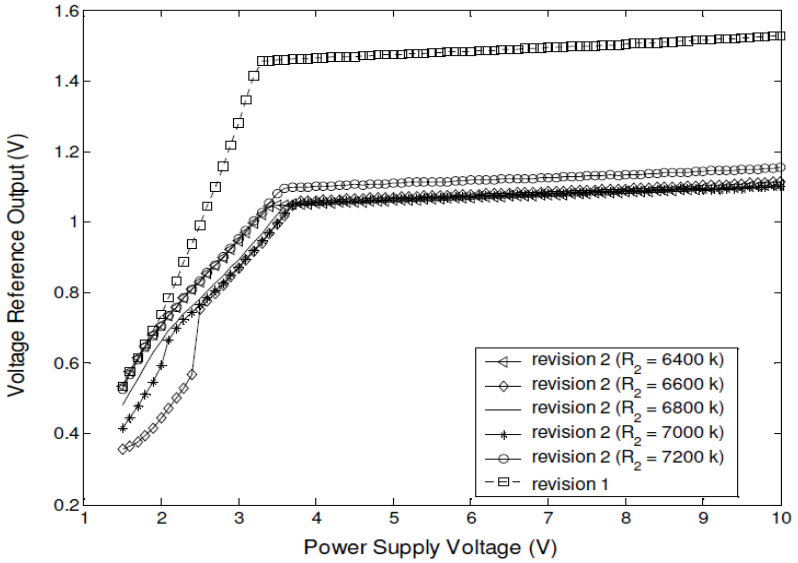

Figure 6: Measured voltage reference output variation for changing power supply

Figure 7 plots the power supply rejection ratio (PSRR) for each of the voltage references at frequencies from 1 kHz to 100 kHz. The revision 1 voltage reference has a PSRR between 62 dB and 46 dB over this range, while the revision 2 voltage references have PSRR varying from 78 dB to 47 dB over this range.

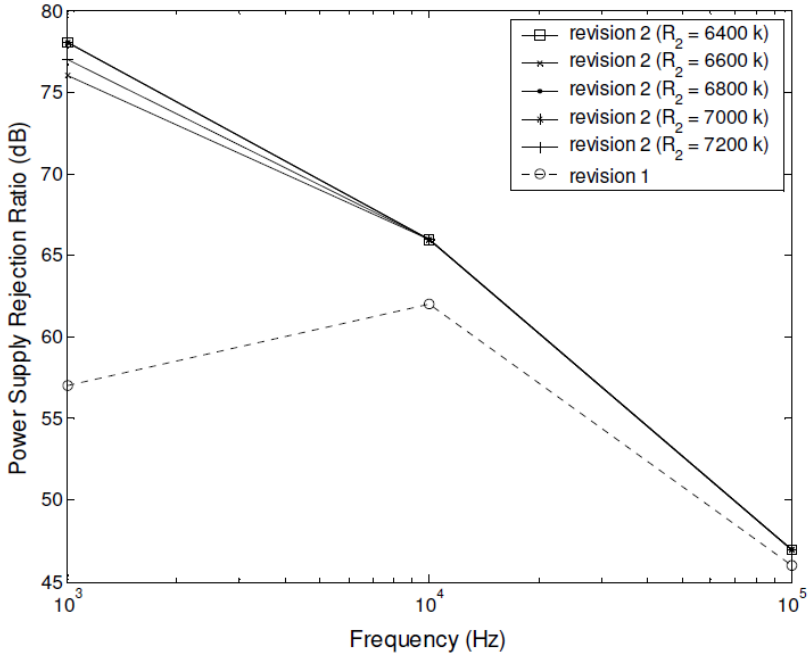

Figure 7: Power supply rejection ratios for voltage references

Experimental and simulated results for the voltage references are summarized in Table 2.

Table 2: Simulated and experimental results for voltage references

Parameter	Revision 1		Revision2	
	Simulation	Experimental	Simulation	Experimental
Power Supply Range	3 to 10 V	3.3 to 10 V	3 to 10 V	3.4 to 10 V
Power Dissipation (5 V supply)	660 µW	N/A	555 µA	N/A
Area	N/A	0.060 mm^2	N/A	0.044 mm^2
Mean V_{BG}	1.515 V	1.499 V	1.063 V	1.067 V
Temperature Coefficient for 30°C - 50°C	1353 ppm/°C	1278 ppm/°C	169 ppm/°C	94 ppm/°C
Power Supply Coefficient for 3 V – 10 V	1873 ppm/V	7108 ppm/V	268 ppm/V	7138 ppm/V
PSRR				
At 1 KHz	-70 dB	-57 dB	-83 dB	-78 dB
At 10 KHz	-70 dB	-62 dB	-80 dB	-66 dB
At 100 KHz	-57 dB	-46 dB	-62 dB	-47 dB

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