© 2019 IJSRST | Volume 6 | Issue 1 | Print ISSN: 2395-6011 | Online ISSN: 2395-602X
Themed Section: Science and Technology
DOI : https://doi.org/10.32628/IJSRST196128

High gain and Low power Up conversion Mixer for Wireless LAN Applications

Ananda M*[1], Dr. A B Kalpana[2]

*[1]ECE Department, PES University-EC Campus, Bangalore, Karnataka, India
[2]ECE Department, Bangalore Institute of Technology, Bangalore, Karnataka, India

ABSTRACT

This work aims an efficient RF Up-Conversion Mixer at Intermediate frequency of 100MHz and Local oscillator frequency of 2.3GHz. The proposed RF Up-Conversion Mixer exhibited better performance in terms of parameter like conversion gain and power consumption. The Simulation of Up-Conversion Mixer shows that the results of voltage conversion gain with LO power at 0dB is 5dB, at 5dB is 4.9dB, and at 10dB is 4.7dB. The power consumption of proposed design is 6mW. The 1dB compression point is -5.43dBm and third order intercept point is 10.53dBm.

Keywords: RF, Up-Conversion, ISM, MIMO-OFDM, Intercept Point.

I. INTRODUCTION

In MIMO-OFDM RF Transceiver for WLAN systems, the high frequency analog signal is passed to Up-Conversion Mixer where Intermediate frequency signal is mixed with Local oscillator [17] signal to give a Radio frequency. Up conversion mixer plays an important role in translating Intermediate frequency signals to RF frequency signal. For RF Transceiver system to achieve low power and high gain mixer design play important role. Hence double balanced active Gilbert mixer is widely used for MIMO-OFDM RF Transceiver system.

A mixer in ideal from is a multiplier circuit [1] [17] and is represented usually with multiplier symbol as shown in Fig 1. This mixer is called Ideal because it can act as both Up-conversion or Down conversion. If the Mixer mixes the Radio frequency signal with local oscillator to give Intermediate frequency then it Down conversion mixer and will be included in Receiver and if the Mixer mixes the Intermediate frequency signal with Local oscillator signal to give Radio frequency then it is Up-Conversion mixer and will be included in Transmitter as shown in Figure 1.

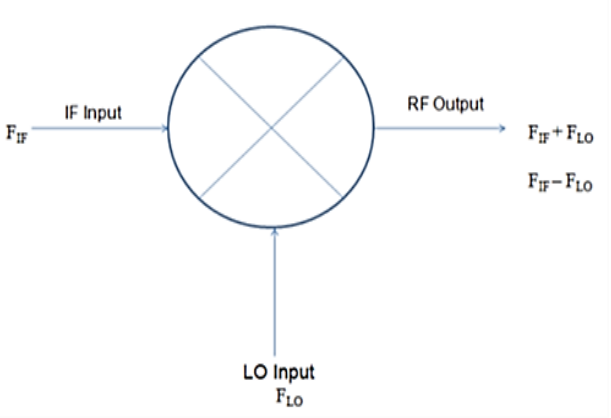

Figure 1 : Mixer (Ideal from)

In MIMO-OFDM RF transmitter The Up-conversion mixer decides [17] the overall performance of the transmitter. Presently with the advent of new

Wireless LAN devices, the speed of WLAN service has to be increased and therefore the frequency band of 2.4GHz is set free for Industry, Scientific and Medicine (ISM).

The work aims at design of High gain, low power Up-conversion mixer in 180nm technology. To achieve this, the following parameters are analyzed,

1. Voltage conversion gain,
   $G = (2/\pi)$ (gm Rload) ……(1)
2. 1 dB Compression point.
3. Intermodulation performance.

II. DESIGN METHODOLOGY

The topologies used in the design of mixer is discussed as follows.

A. Basic Double Balanced Mixer cell (Gilbert Mixer)

In Figure 2 the transconductance stages are transistor M1 and M2 it is also called as Driver stage. Switching stages consists of transistor M3, M4, M5, M6. Resistive load RL is called as transresistance stage it is used for broadband operation. The size of the transistor M1 and M2 should be small compare to that of the transistor M3, M4, M5, M6 to obtain perfect switching. Double balanced mixer is formed by two single balanced mixers. Transistor M1, M3, M4 form a one single balanced mixer and transistor M2, M5 and M6 form another single balanced mixer. Transistor M1 and M2 is provided with Intermediate frequency signal which is differential. Transistor M3, M4, M5 and M6 provided with Local oscillator signal which is differential. VIF+ and VIF- denote the differential phased of IF inputs. Each half circuit commutates the IF current to its RF output, if VLO+ is large transistor M3 and M5 turns on and if VLO- is small enough transistors M4 and M6 turns off. Now transistor M3 and M5 are closed switch so that M1 transistor is connected to RL. The output is taken as a Radio frequency VRF+.

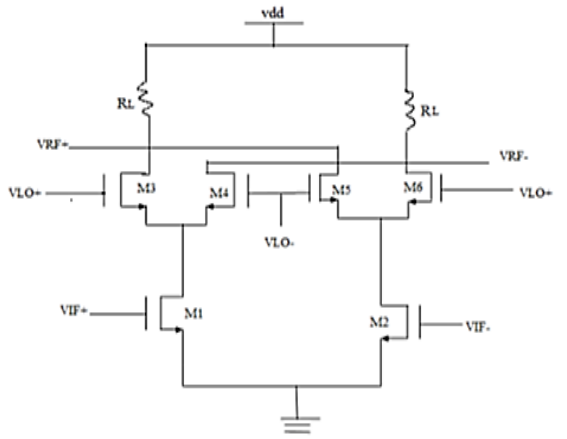

Figure 2 : Gilbert mixer (Double balanced).

If VLO- is large transistor M4 and M6 turns on and if VLO+ is small enough transistors M3 and M5 turns off. Now transistor M4 and M6 are closed switch so that M1 transistor is connected to RL and M2 is connected to RL. The output is taken as an Radio frequency VRF-. This is also a differential amplifier configuration but with an output interchange with respect to other output. In other words, the output is same as before just it is multiplied by a factor -1. The purpose of gilbert cell is to multiply square wave with +1 or -1 at LO frequency by the time domain input IF signal is called as Mixing [2].

B. Basic Double Balanced Mixer cell (Gilbert Mixer)

In an IC chip as there are number of Amplifier stages, the biasing of transistors can be done by using constant source. A constant [17] DC current produced at one position is duplicated to various stages of amplifier and this process is called current steering as shown in Figure 3 [3][4].

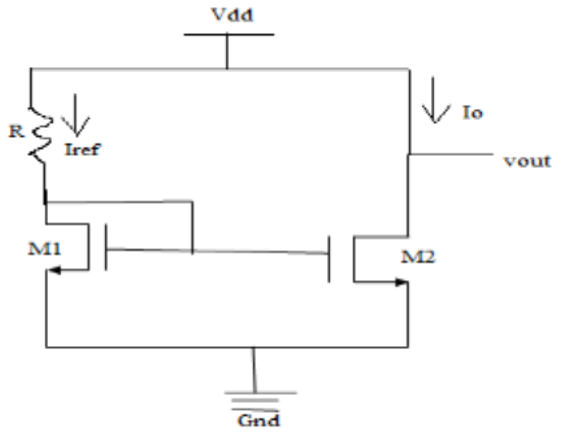

Figure 3 : Current mirror circuit

From Figure 3 the nmos transistors M1 and M2 form the "current mirror". The saturation current equation for transistor M1 is given by (2) and (3).

$$I_D = I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_G - V_{Tn})^2 \quad \text{.....(2)}$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn} - V_{Tn}\right)^2 \quad \text{.....(3)}$$

$$I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{REF} \quad \text{.....(4)}$$

From current mirror circuit [4] [17] since drain of transistor M1 is shorted to its gate, the transistor M1 operates in saturation region and as the gate of transistor M1 and M2 is also shorted. The ratio of I_{out} and I_{REF} is given by the ratio of device dimensions equation (4), a quality that can be controlled with reasonable accuracy.

III.DESIGN OF PROPOSED UP CONVERSION MIXER

The design of up-conversion mixer consists of the Current mirror, Current-Bleeding, IF stage, switch stage and load. Constant current source is used to bias the transistor. The IF stage is known as driver stage where it converts the voltage in to current and the differential input is given to the IF stage and it is given to switching stage. The differential input is given to the switching stage. The [17] Load stage is called as trans inductance where current converted in to voltage.

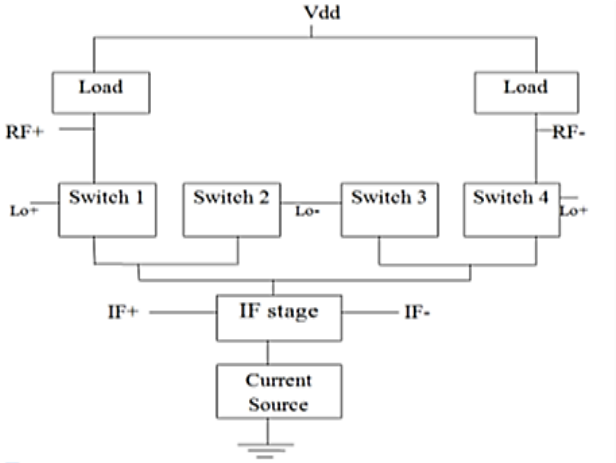

Figure 4 : Block diagram of Up conversion mixer

IV. DESIGN OF PROPOSED UP CONVERSION MIXER

Mixer design Figure 5 consists of Current Mirror, Current-Bleeding and [17] Double balanced mixer. Current mirror is mainly used to biases the transistor and the current mirror transistor are M1-M3 and M4-M6. Resistance R is used to block AC signal and it passes DC and its value depends on the voltage of current mirror. Transistors M7-M10 works as ideal switches, the current-bleeding sources are used and the switching transistors are biased in the saturation region. The bleeding current can be tuned through the transistors M11 and M12. Capacitors are used to block DC signal.

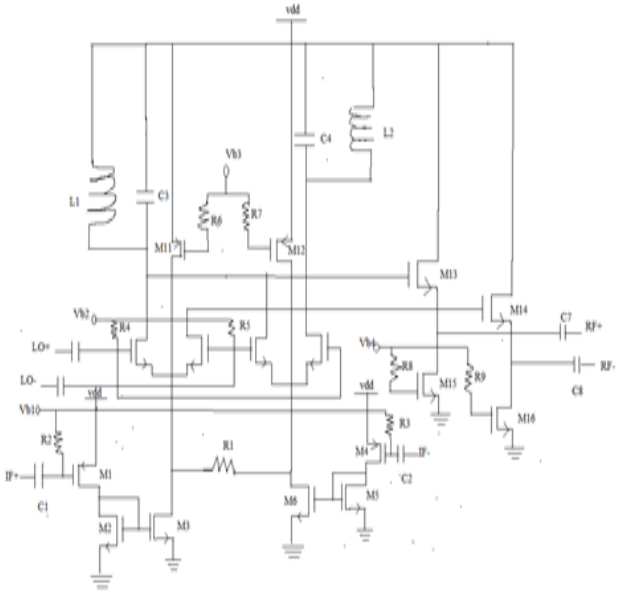

Figure 5 : Schematic of Proposed Up-conversion mixer

V. DESIGN AND IMPLEMENTATION OF UP-CONVERSION MIXER

Determine the W/L ratio of proposed system Up-Conversion Mixer is done in 180nm technology. For 180nm technology the standard [5][17] value for threshold voltages is 0.5V-0.6V and the gate to source voltage is 0.6V-0.8V.

In current mirror circuit the transistor operates in saturation region therefore the drain current equation is given by

$$ID = ½ \mu n Cox(W/L) (Vgs - Vth)2 \quad \text{.....(5)}$$

The output power can be calculated as

P = Vdd ID

6m = 1.8 ID

$$ID=3.3m \quad \text{..... (6)}$$

μn cox for nmos transistor of Current mirror and IF stage is given by 519μ ……...(7)

substitute equation (6) and (7) in (5)

$$ID = ½ \mu n Cox (W/L) (Vgs - Vth)2$$

$$2.2mA = ½ *519\mu*(W/180nm)*(0.79-0.7)\ 2 \quad W \approx 320\mu m \quad (8)$$

For IF[17] stage transistor and current mirror the width is taken as approximately 320μm

The current starts diving at LO stage equally therefore current is given by 2.2m and substitute in equation (5)

$$ID = ½ \mu n Cox (W/L) (Vgs - Vth)2$$

$$1.7mA = ½ *519\mu*(W/180nm) *(0.79-0.7)2$$

$$W \approx 160\mu m \quad \text{..... (9)}$$

For LO stage transistor the width is taken as approximately 160μm

VI. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

The Schematic design of Proposed Up conversion mixer shown in Figure 6 and Figure.7, shows the design under test of proposed Up-Conversion Mixer. The supply voltage is 1.8V. Three ports [17] are used IF port, LO port and RF port. Balun is used in simulation where it converts the differential inputs and outputs of mixer to single ended source and load impedance. Device which achieves balanced to unbalanced transformation is called as Balun.

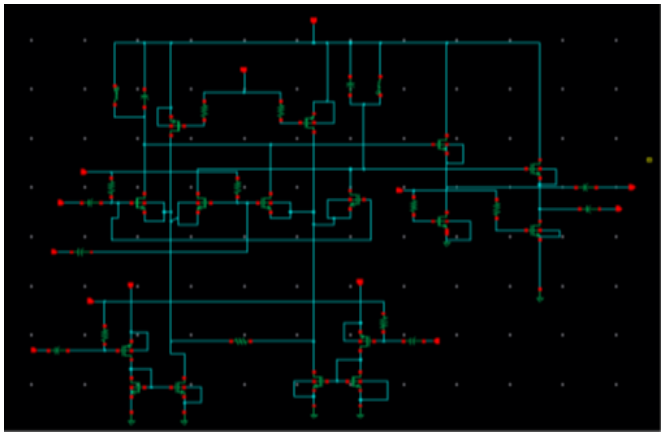

Figure 6 : Schematic design of Up conversion mixer

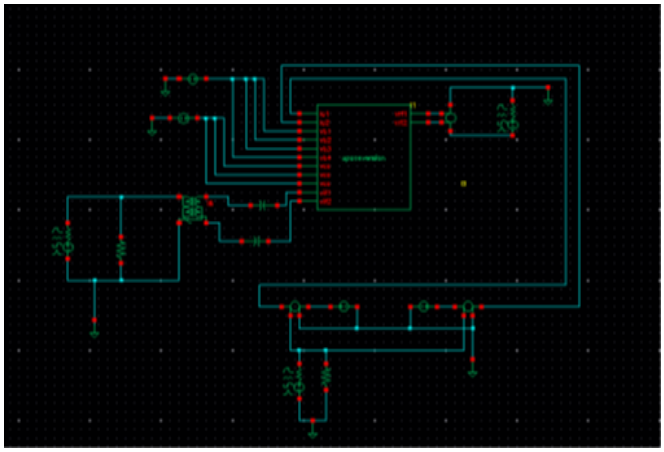

Figure 7 : Design under test of proposed Up-Conversion Mixer

The power conversion gain [17]and voltage conversion gain for the proposed-Up conversion mixer is obtained by performing the PAC analysis and QPSS analysis. The results are validated on Cadence Virtuoso IC 613[5][6] at 180nm Technology. Here load impedance and mixer's input impedance are both equal to the source impedance and therefore, the voltage and power conversion gain are the same. In this paper, LO and IF frequency is set to 2.3GHz and 100MHz respectively.

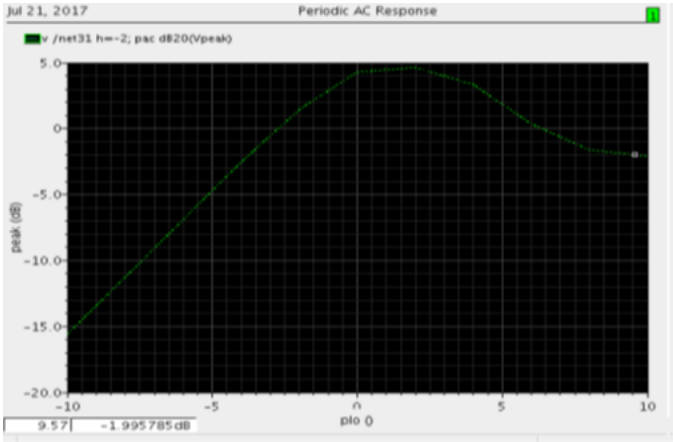

Figure 8 : Voltage conversion gain @10dB

Figure 8 shows the voltage conversion gains at 10dB. And voltage conversion gain with LO power at 0dB is 5dB, at 5dB is 4.9dB, and at 10dB is 4.7dB.

1 dB Compression point is the point at which device shows the Non-linear characteristics from Linear. 1 dB Compression point of proposed Up-Conversion Mixer is given in the Figure 9: 1dB conversion compression point of proposed system is -5.43.

The Third intercept point [17] is same as 1 dB Compression point in which two small different frequencies is applied to the input and the output power versus input powers are plotted. These two curves will linearly increase to meet is called third order intercept point, Figure 10. Shows the IIP3 of proposed Up conversion mixer.

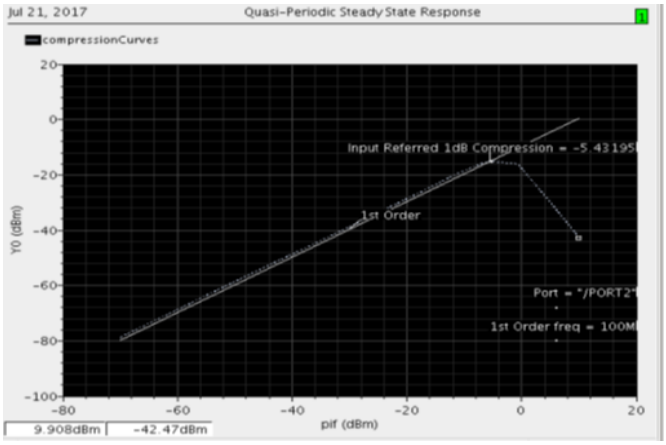

Figure 9 : 1dB compression point

The third order intercept point [17] of proposed Up-Conversion mixer is given in Fig 10. the IIP3 of proposed system is 10.533. The transient analysis of proposed Up-Conversion mixer is shown in Figure 11.

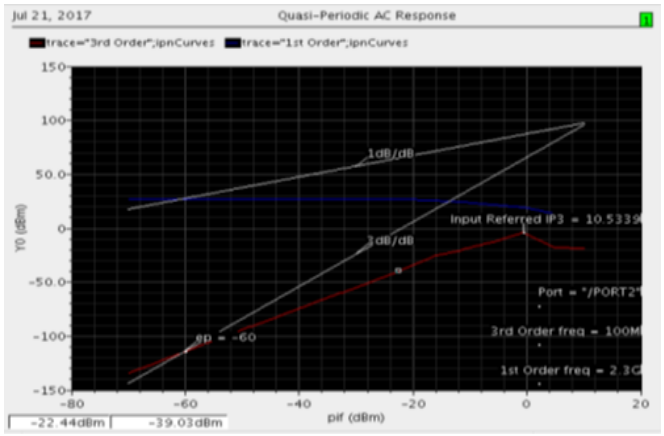

Figure 10 : IIP3 using QPSS and QPAC.

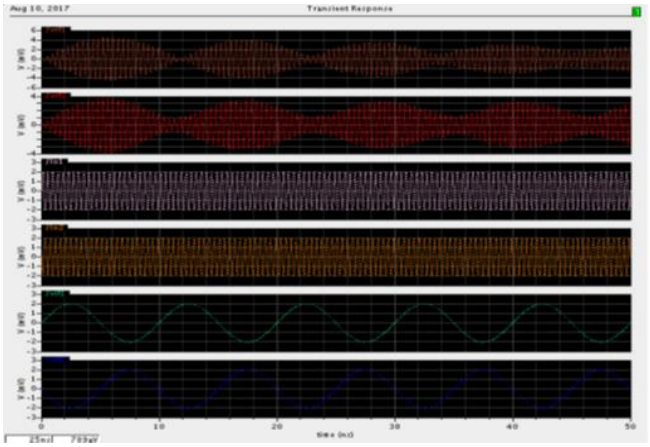

Figure 11: Envelop transient response of proposed mixer.

Power Spectrum gives a good estimate of the total power consumption. Most of the power is in the main output harmonics. The power dissipation is P= 1.8V X 2.92mA = 6mA. The power spectrum of proposed mixer is shown in Figure 12.

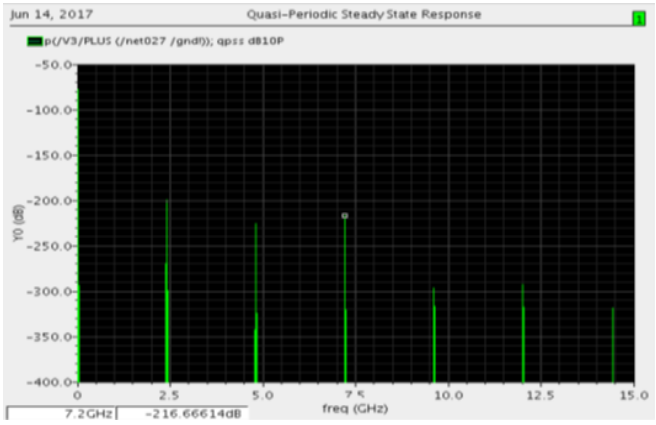

Figure 12: Power Spectrum of proposed mixer

TABLE I

PERFORMANCE COMPARISON

Year	2009	2012	2013	2014	2015	2017-2018
Reference	[12]	[13]	[14]	[15]	[16]	This work
Technology	0.18 µm	0.18µm	0.18 µm	0.18 µm	0.18µm	0.18µm
LO	0	2	0	4	0dB	0 dBm
power	dBm	dBm	dBm	dBm	m	
Conversion gain	2.5 dB	7.1 dB	7.5 dB	5 dB	28.4 dB	5 dB
IIP3	6.5 dBm	7.3 dBm	-5 dBm	9 dBm	24.71 dBm	-10.53 dBm
1 dB compression pt	-	-	-	-	32.04 dBm	5.43dBm
Supply voltage	1V	1.2V	1.8 V	1.5 V	3.3V	1.8V
Power supply	39mW	4.5mW	8.1 mW	8.2 mW	8.66 mW	6mW

IV. CONCLUSION

In proposed system theoretical and [17] practical values of the IF frequency is 100M, LO frequency is 2.3G and supply voltage 1.8V. The power consumption of simulated result is 6mW but theoretical value is 6.1mW. 1dB compression point and IIP3 is -5.433 and 10.533 respectively.

V. ACKNOWLEDGEMENT

I would like thank the institute PES University-EC Campus for providing me with a conducive environment and BIT for research facilities that helped me in completing the work on time. I also thank my PhD guide Dr. A B Kalpana, Associate Professor, BIT, who has been very supportive in all possible ways to make this successful piece of work.

VI. REFERENCES

[1] Rajendra D Khanphade, Santosh B. Patil, "A 2.4GHz Double balanced Differential Input Differential Output Low Power High gain

Gilbert Cell Down Conversion Mixer in TSMC 180nm CMOS RF process," IEEE sponsored 2nd International Conference of Electronics and Communication System, pp. 1187-1193, 2015.

[2] Payam Gh, Afshar, Mahrokh Maghsoodi, Reza E Atani and Mehregan Mahdevi, "A 3.5 GHz Low Noise Figure Mixer with High Conversion Gain for Wimax Systems", Volume 3, Issue 5, May 2013.

[3] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mc Graw-Hill edition, pp100-126, 2002.

[4] Adel S Sedra, Kenneth C Smith, "Microelectronics Circuits", sixth Edition, Oxford university Press, pp587-590, 2004.

[5] http:/wwww.cadence.com/

[6] http:/www.ncjrs.gov/pdf_files/nij/191160.pdf

[7] Behzad Razavi, "RF Transmitter Architectures and circuits", IEEE Custom Integrated Circuits Conference, pp 197-204, 1999.

[8] Behzad Razavi- "RF Microelectronics", Prentice hall Inc. 2nd Edition, 1998.

[9] Bosco Leung, "VLSI for Wireless Communication", Prentice Hall Electronics and VLSI series.

[10] Jacob Phil, Kare Tais and Erik Bruun, "Direct Down conversion with Switching CMOS Mixer",IEEE ISCAS, pp.117-120, 2001.

[11] Douglas A Pucknell and Kamran Eshraghian, "The Design of CMOS Radio Frequency Integrated Circuits", New York Cambridge University Press, pp25-55, 2008.

[12] Arif A. Siddiqi and Tad Kwasniewski, "2.4GHz RF Up-Conversion Mixers in standard CMOS technology", International Symposium on Circuits and System, 2009.

[13] Rajendra D. Kanphade and Santosh B. patil "A 2.4GHz Double Balanced Differential Input Differential Output Low Power High Gain Gilbert Cell Up-Conversion Mixer in TSMC 180nm CMOS RF Process", 2015 IEEE.

[14] S.A.Z Murad, R.K Pokharel, M.A. Abdelghany and S.A.Z Murad "High Linearity 5.2 GHz CMOS Up-Conversion Mixer Using Derivative Superposition Method", 2010 IEEE .

[15] Jeng-Han Tsai, Wu-Hsuan Lin, and Chuan-Jung Huang "Design of 15-34 GHz Low-Power Up-Conversion Ring Mixer Using 180nm CMOS Technology", 2016 IEEE.

[16] Darshak Bhatt Jayanta Mukherjee Jean-Michel Redoute "A High Isolation Linear Folded Mixer for Wi-Fi Applications", 2014 IEEE.

[17] Ananda M, Dr A B Kalpana, Design of High gain Low power down conversion Mixer used for wireless LAN applications, IEEE-International Conference on Innovative Mechanisms for Industry Applications (ICIMIA-2017) conducted by DSCE, Bengaluru from 21st to 23rd February 2017.

Cite this article as : Ananda M, Dr. A B Kalpana, "High gain and Low power Up conversion Mixer for Wireless LAN Applications", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 6 Issue 1, pp. 179-185, January-February 2019. Available at doi : https://doi.org/10.32628/IJSRST196128

Journal URL : http://ijsrst.com/IJSRST196128