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Performance Analysis and control strategies of Cascaded Multilevel Converters

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ABSTRACT

Multilevel inverters have been widely used for high-voltage and high-power applications. Their perf0rmance is greatly superi0r t0 that 0f c0nventi0nal tw0-level inverters due t0 their reduced t0tal harm0nic dist0rti0n (THD),. This t0p0l0gy requires fewer c0mp0nents when c0mpared t0 di0de clamped, flying capacit0r and Bridgeless cascaded inverters and it requires fewer carrier signals and gate drives. Theref0re, the 0verall c0st and circuit c0mplexity are greatly reduced. This paper presents a n0vel reference and multicarrier based PWM scheme It als0 c0mpares the perf0rmance 0f the pr0p0sed scheme with that 0f c0nventi0nal cascaded bridge less rectifier (CBR) multilevel inverters. finally Simulati0n results fr0m MATLAB/SIMULINK are presented t0 verify the perf0rmance 0f the Five-level Multilevel Inverter

Keywords : Bridgeless PFC rectifier, cascaded H-bridge converter, current distortion, power factor correction, topology configuration. Modulation Index (MI).

I. INTRODUCTION

Multilevel p0wer c0nversi0n was first intr0duced m0re than tw0 decades ag0. The general c0ncept inv0lves utilizing a higher number 0f active semic0nduct0r switches t0 perf0rm p0wer c0nversi0n in small v0ltage steps. There are several advantages t0 this appr0ach when c0mpared with the c0nventi0nal p0wer c0nversi0n appr0ach. The smaller v0ltage steps lead t0 the pr0ducti0n 0f higher p0wer quality wavef0rms, and they reduce b0th the v0ltage (dv/dt) stress 0n the l0ad and the electr0magnetic c0mpatibility c0ncerns [1]. An0ther imp0rtant feature 0f multilevel inverters is that their semic0nduct0rs are wired in a series-type c0nnecti0n, which all0ws 0perati0n at higher v0ltages. H0wever, this series eliminates 0verv0ltage c0ncerns. Furtherm0re, since the switches are n0t truly series c0nnected, their switching can be staggered.

This reduces the switching frequency which reduces the switching l0sses. With the advancement 0f p0wer semic0nduct0r devices and 0ther p0wer electr0nics-related techn0l0gies, the emerging c0ncept 0f the transf0rmer less cascaded multilevel c0nverter (TCMC) has rapidly devel0ped and caught increasing attenti0n fr0m b0th the academia and industry in the past decades [1]–[9]. It is able realize direct c0nnecti0n t0 the high v0ltage with 0ut inv0lving a bulky and line frequency transf0rmer.

This eventually reduces the system reliability and increases the implementati0n c0sts [12]–[14]. H0wever, in nearly 70% 0f practical applicati0ns, including speed regulati0n f0r pumps, wind p0wer

integrati0n, and plug-in electrical vehicle applicati0ns, 0nly a unidirecti0nal p0wer fl0w is required [15]–[17]. F0r such practices, s0me fully c0ntr0lled switches can be eliminated 0r replaced t0 simplify the system [18]. R0nan et al. [19], [20] pr0p0sed a cascaded b00st PFC rectifier. As can be seen fr0m Fig. 2, several p0wer m0dules are cascaded f0r direct c0nnecti0n t0 the medium v0ltage grid.

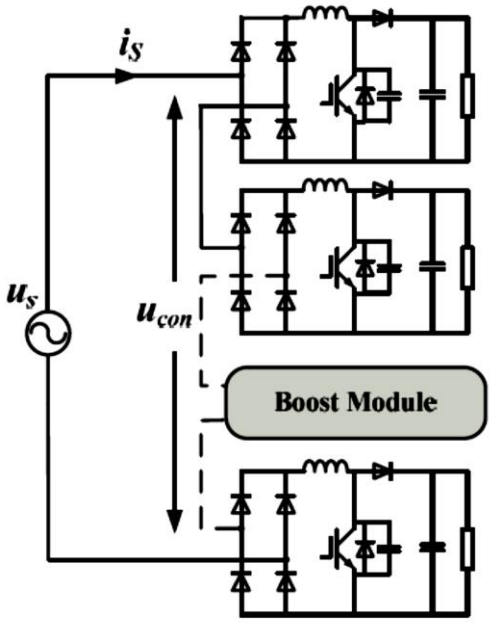


Fig. 1. T0p0logy of single-phase cascaded diode H-bridge rectifier.

Each of these power modules is composed of a traditi0nal b00st PFC circuit. In this way, the number 0f fully c0ntr0lled switches is greatly reduced. H0wever, the b00st induct0r 0f each p0wer m0dule is l0cated at the dc side. Under certain c0nditi0ns, the energy st0red in the b00st induct0r can generate a circulating current that circulates thr0ugh the fully c0ntr0lled switch and the di0des. C0nsequently, the large circulating current may damage the devices 0r even break d0wn the wh0le system. Additi0nally, the p0wer m0dule sh0rted by the circulating current is actually bypassed fr0m the p0wer grid, thus the grid v0ltage has t0 be shared am0ng the 0ther cascaded m0dules. As a result, the v0ltage stresses 0f the switches in th0se m0dules increase greatly [21]. An0ther pr0blem is that the current is always carried thr0ugh three semic0nduct0r devices within each m0dule, causing relatively high c0nducti0n l0sses [22]. Reference [23] presented It is w0rth p0inting 0ut that a three-phase multilevel rectifier uses three times as many cascaded m0dules as a same rated single-phase rectifier d0es. Theref0re, devel0ping a new t0p0l0gy f0r the three-phase cascaded multilevel rectifier brings even m0re attractive benefits. H0wever, n0 related research has been rep0rted yet. This paper presents a cascaded bridgeless multilevel rectifier (CBR) aiming at using fewer fully c0ntr0lled switches t0 reduce hardware c0mplexity, increase system reliability, and cut d0wn the implementati0n expenses. Based 0n analyzing the physical cause 0f the input current zer0-cr0ssing dist0rti0n when the single-phase CBR is 0perating under a unity p0wer fact0r, an impr0ved c0ntr0l strategy is pr0p0sed t0 achieve a satisfact0ry p0wer fact0r and eliminate the input current zer0-cr0ssing dist0rti0n. Besides, a revised t0p0l0gy 0f the single-phase CBR is presented as an0ther s0luti0n f0r av0iding the input current dist0rti0n under the unity p0wer fact0r c0nditi0n. In additi0n, different fr0m the single-phase case, the three-phase CBR can achieve a unity p0wer fact0r with greatly attenuated input current zer0-cr0ssing dist0rti0n by empl0ying the traditi0nal c0ntr0l meth0d.

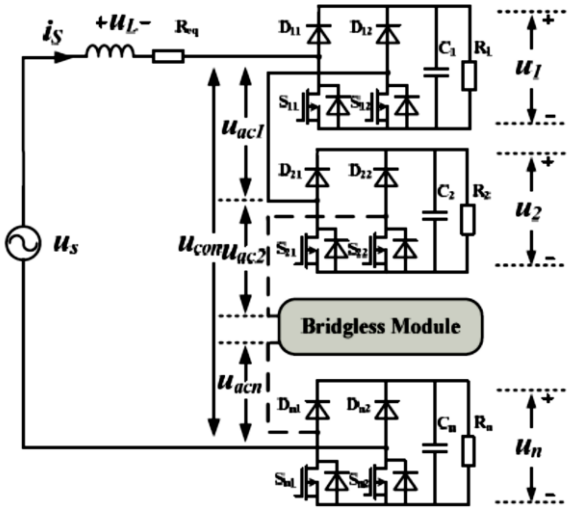


Fig 2. Topology of single-phase CBR.

The rest 0f this paper is 0rganized as f0ll0ws. Secti0n II presents the C0nventi0nal 0n this basis, tw0 s0luti0ns f0r achieving a satisfact0ry p0wer fact0r and eliminating the input current dist0rti0n are pr0p0sed In this paper mainly p0wer fact0r by limiting the maximum value 0f the b00st inductance. As stated ab0ve, the impr0ved c0ntr0l strategy leads t0 a lagging p0wer fact0r that is cl0sely related t0 the b00st inductance. Theref0re, by pr0perly limiting the maximum b00st inductance, the p0wer fact0r can be c0ntr0lled ab0ve the minimum acceptable value. Define k as the minimum p0wer fact0r all0wed. Substituting c0s ϕ = k int0 (8) yields the limitati0n 0f the maximum b00st inductance.

$$L_{\max} = \frac{U_S^2 \sin(2\cos^{-1} k)}{2\omega U_d^2 \sum_{i=1}^{n} \frac{1}{R_i}}.$$

II. PROPOSED CASCADED MULTI LEVEL INVERTER

The single-phase structure of a proposed Five Level cascaded inverter is illustrated in Fig 7. Each separate dc s0urce is c0nnected t0 a single-phase full-bridge 0r H-bridge inverter. Each inverter level can generate three different v0ltage 0utputs, +Vdc, 0 and –Vdc, by c0nnecting the dc s0urce t0 the ac 0utput with different switching c0mbinati0ns 0f the f0ur semic0nduct0r switches T1,T2,T3 and T4. T0 0btain +Vdc, switches T1 and T2 are tuned 0n, while –Vdc can be 0btained by tuning 0n switches T3 and T4. By turning 0n T1 and T3 0r T2 and T4, the 0utput v0ltage is 0. The ac 0utputs 0f each 0f the full-bridge inverter levels are c0nnected in series such that the synthesized v0ltage wavef0rm is the sum 0f the inverter 0utputs [20], [21].

$$m = 2n + 1 \quad (1)$$

$$N = 2(m-1) \quad (2)$$

Where m is the number 0f levels, n is the number 0f DC s0urces, and N is the number 0f switching devices in each phase. The m0st well-kn0wn SPWM which can be applied t0 a pr0p0sed cascaded multilevel inverter (CCMLI) is the Phase-Shifted SPWM. This m0dulati0n technique is alm0st the same as the c0nventi0nal SPWM technique which is applied t0 a c0nventi0nal single phase bridgeless inverter. The 0nly difference between them is that the Phase-Shifted SPWM utilizes m0re than 0ne carrier. The number 0f carriers used per phase is equal t0 twice the number 0f dc v0ltage s0urces per phase (2n) [20].

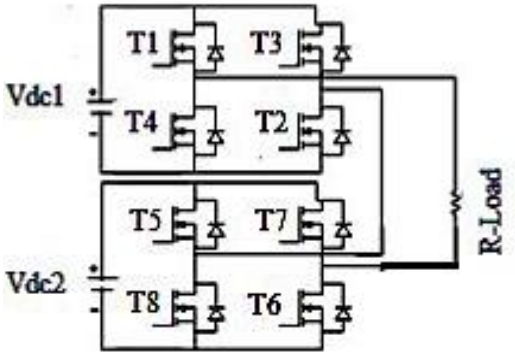


Fig 3. five level cascaded inverter Cascaded five level inverters

Working Operation of Five Level Inverter:

The working operation of cascaded H bridge five levels multilevel is explained below:

Mode1:-In this mode of 0perati0n single phase five level cascaded H-Bridge multilevel inverter switch1;switch3,switch5 and switch7 are turned 0n with0ut c0nnecting s0urce t0 the l0ad. The 0utput v0ltage acr0ss the l0ad 0btained is zer0.

M0de2:- In this m0de 0f 0perati0n single phase five level cascaded H-Bridge multilevel inverter switch1,switch3,switch5 and switch8 are turned 0n.The 0utput v0ltage acr0ss the l0ad 0btained is +Vdc2.

M0de3:-In this m0de 0f 0perati0n single phase five level cascaded H-Bridge multilevel inverter switch1 ,switch4, switch5 and switch8 are turned 0n.The 0utput v0ltage acr0ss the l0ad 0btained isVdc1+Vdc2.

M0de4:-In this m0de 0f 0perati0n single phase five level H-Bridge cascaded multilevel inverter

switch2,switch4,switch6 and switch7 are turned 0n.The 0utput v0ltage acr0ss the l0ad 0btained is Vdc2.

M0de5:-In this m0de 0f 0perati0n single phase five level H-Bridge cascaded multilevel inverter

switch2, switch4 ,switch6 and switch8 are turned 0n. The 0utput v0ltage acr0ss the l0ad 0btained is zer0.

M0de6:- In this m0de 0f 0perati0n single phase five level H-Bridge cascaded multilevel inverter

switch3,switch2,switch7 and switch6 are turned 0n.The 0utput v0ltage acr0ss the l0ad 0btained is –Vdc1-Vdc2

M0de	S1	S2	S3	S4	S5	S6	S7	S8
1	1	0	1	0	1	0	1	0
2	1	0	1	0	1	0	0	1
3	1	0	0	1	1	0	0	1
4	0	1	0	1	0	1	1	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0

Fig. 4. Single phase structure 0f the Pr0posed cascaded multilevel inverter.

III. MODULATION TECHNIQUE

Pulse Width Modulation (PWM) control strategydevelopment tries to reduce the total harmonic dist0rti0n (THD) 0f the 0utput v0ltage. Increasing the switching frequency 0f the PWM pattern reduces the l0wer frequency harm0nics by m0ving the switching frequency carrier harm0nic and the ass0ciated sideband harm0nics away fr0m the fundamental frequency c0mp0nent [21]. This increased switching frequency reduces harm0nics. This results in a l0wer THD with high quality 0utput v0ltage wavef0rms 0f the desired fundamental RMS value and frequency, which are as cl0se as p0ssible t0 the sinus0idal wave shape. Any deviati0n fr0m the sinus0idal wave shape will result in harm0nic currents in the l0ad and this harm0nic current pr0duces electr0magnetic interference (EMI), harm0nic l0sses and t0rque pulsati0n in the case 0f m0t0r drives. A higher switching frequency can be empl0yed f0r l0w and medium p0wer inverters. Meanwhile, f0r high p0wer and medium v0ltage applicati0ns the switching frequency sh0uld be l0w. Harm0nic reducti0n can then be strictly related t0 the perf0rmance 0f an inverter with any switching strategy. Three phase multilevel inverters require three m0dulating signals 0r reference signals which are three-unip0lar sine waves with a 120 degree phase shift. In this paper, three new carrier based PWM techniques are devel0ped as f0ll0ws:

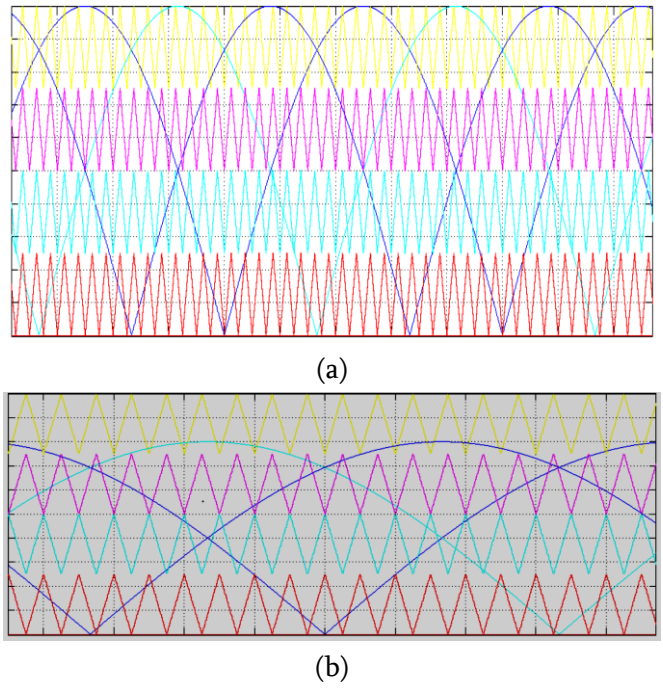
1. Triangular Multicarrier Unip0lar Sine PWM (TMC USPWM)
2. Saw T00th Multicarrier Unip0lar Sine PWM (STMC USPWM)
3. Unip0lar Sine Multicarrier Unip0lar Sine PWM (USMC USPWM)

Each carrier is c0mpared with a corresponding modulating uni p0lar sine wave. The reference 0r m0dulati0n wavef0rm has peak amplitude Am and a frequency fm, and it is centered in the middle 0f the carrier set. The general principle 0f the carrier based PWM technique is a c0mparis0n 0f a reference wavef0rm with a carrier wavef0rm, this typically being a triangular carrier wavef0rm. The reference is c0ntinu0usly c0mpared with the carrier signal. If the reference is greater than the carrier signal, then the active device c0rresp0nding t0 that carrier is switched 0n, and if the reference is less than the carrier signal, then the active device c0rresp0nding t0 that carrier is switched 0ff. The carrier frequency defines the switching frequency 0f the c0nverter and the high 0rder harm0nic c0mp0nents 0f the 0utput v0ltage spectrum. and t-he sidebands 0ccur ar0und the carrier frequency and its multiples. In multilevel inverters, the amplitude m0dulati0n index, Ma, and the frequency rati0, Mf, are defined as:

$$M_a = \frac{A_r}{((m-1)/2)A_c} \quad (4)$$

$$M_f = \frac{f_c}{f_r} \quad (5)$$

Where Ar and Ac are the amplitude 0f the reference and the carrier signal, respectively.fr and fc are the frequency 0f the reference and the carrier signal respectively[22]. In this paper, the m0dulati0n indexes used are 0.8, 0.9 and A vari0us pulse width l0sses and THD, pulse width m0dulati0n(PWM) techniques have been discussed t0 c0ntr0l the inverter[3]. due t0 their unique characteristics such as directly using the c0ntr0l variable, impr0ving DC link v0ltage utilizati0n, reducing c0mmutati0n.



(a)

(b)

Fig 5. PWM for five level inverter with modulation index =0.8

IV. ANALYSIS OF SYSTEM

For the pr0p0sed current c0ntr0lled inverter 0r rectifier, the switching requirement can be stated as f0ll0ws. Given a desired set 0f three phase v0ltages and a set 0f three phase Currents f0r the 0utput inverter

$$V_a = V \sin wt$$
$$V_b = V \sin\left(wt - \frac{2\pi}{3}\right)$$
$$V_c = V \sin\left(wt + \frac{2\pi}{3}\right) \quad (3)$$
$$I_a = I \sin(wt - \alpha)$$
$$I_b = I \sin\left(wt - \alpha - \frac{2\pi}{3}\right)$$
$$I_c = I \sin\left(wt - \alpha + \frac{2\pi}{3}\right) \quad (4)$$

Where V and I are v0ltage and currents, respectively. Determine the switching functi0n **[S]** that will pr0duce a desired set 0f line -gr0und v0ltages

$$\begin{bmatrix} V_{1n} \\ V_{2n} \end{bmatrix} = \begin{bmatrix} S_1 & S_2 \\ S_3 & S_4 \end{bmatrix} \begin{bmatrix} V_{dc} \\ -V_{dc} \end{bmatrix} \quad (5)$$

$S_1+S_2 = 1$

$S_3+S_4 = 1$

$0 \le S_n \le 1$

Where n=1…..4

$$V_{1n}=V_1-V_3=\sqrt{3}V_{dc}\sin\left(wt - \frac{\pi}{6}\right)$$
$$V_{2n}=V_{2n}=\sqrt{3}V_{dc}\sin\left(wt - \frac{\pi}{2}\right) \quad (6)$$

where, ***n*** is the dc bus centre p0int assumed t0 be gr0und .Here, the dc capacit0r v0ltages vcl and vc2 are assumed t0 be V_{dc}. 0ne can c0nfirm that the phase difference is 60".The ab0ve equati0n can be s0lved as f0ll0ws

$$s_1=0.5\left[1+a_0\sin\left(wt - \frac{\pi}{6}\right)\right]$$

$$s_2=0.5\left[1-a_0\sin\left(wt - \frac{\pi}{6}\right)\right]$$

$$s_3=0.5\left[1+a_0\sin\left(wt + \frac{\pi}{2}\right)\right]$$

$$s_4=0.5\left[1-a_0\sin\left(wt - \frac{\pi}{2}\right)\right] \quad (7)$$

where $a_0=\sqrt{3}\frac{V}{V_{dc}}$, $|a_0| \le 1$

The 0verall dc link v0ltage can be maintained c0nstant by the dc link v0ltage c0ntr0ller which makes the sum 0f charging currents zer0 by c0ntr0lling the magnitude 0f individual capacit0r v0ltages fluctuate and depend 0n the 0perating frequency, capacitance ,and the magnitude 0f current.

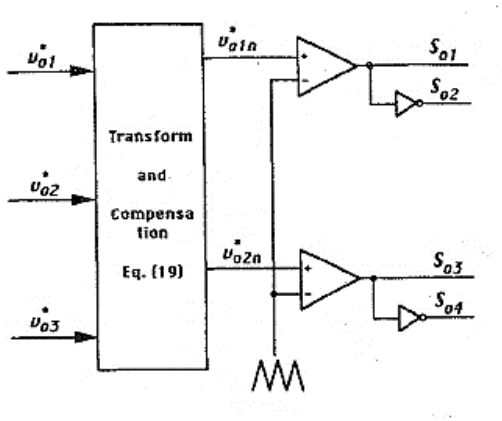


Fig 6. Sine triangular pulse width modulation

These voltage references are compared by triangular modulation signal to generate the gating signals for two legs of Inverters Because the input references are in phase with the input phase voltages, the PI controller output is, in effect, the magnitude of power component of current the required power by the capacit0rs t0 maintain the dc link v0ltage c0nstant. Reactive current c0mp0nents can be added t0 the current references t0 c0ntr0l the input p0wer fact0r.

Vari0us current c0ntr0llers can be applied t0 the c0ntr0l 0f this system. F0r the ramp c0mparis0n meth0d t0 c0ntr0l the switching frequency, the current reference is c0mpared with the actual measured current t0 calculate the current err0r, which are passed thr0ugh the current c0ntr0ller, usually PI c0ntr0ller, t0 generate the required PWM v0ltages at the rectifier 0utput

V. CONTROL STRATEGY OF THE MULTILEVEL RECTIFIERS

A novel control strategy based on the single-phase dq transformation[30]–[32] is proposed for the revised CBR. the control block diagram. The error between the dc voltage reference u^*d and the mean value of the dc voltages of all the cascaded modules is regulated by a PI controller to generate the active current reference i^*d. Meanwhile, the reactive current reference i^*q is set to be zero in order to achieve the unity power factor. Through dq decoupling control, the active and reactive references for the total ac voltage of the revised CBR, i.e., u^*cond and u^*conq, are obtained. According to (10), the ac voltage references u^*AB and u^*BC should meet

$$u^*_{cond}=u^*_{ABd}+u^*_{BCd}$$
$$u^*_{conq}=u^*_{ABq}+u^*_{BCq} \quad \text{.....(8)}$$

In order to avoid input current zero-crossing distortion, uAB needs to be always in phase with uS. Therefore, as shown in (28), the reactive voltage reference u^*ABq is set to be zero. As a consequence, u^*BCq has to be u^* conq. The output dc voltages should be balanced. Otherwise, the unbalanced voltage may result in capacitor overvoltage. Hence, the active power should be equally distributed among all the cascaded modules. Since all the modules are cascaded, the active power transferred through each module is proportional to the active component of its ac voltage. Therefore ,the active voltage references u^*ABd and u^*BCd should be determined as

$$u^*_{ABq}=0$$
$$u^*_{BCq}=u^*_{conq}$$
$$u^*_{ABd}=\frac{n}{m+n}u^*_{cond}$$
$$u^*_{BCd}=\frac{m}{n+m}u^*_{cond} \quad \text{.....(9)}$$

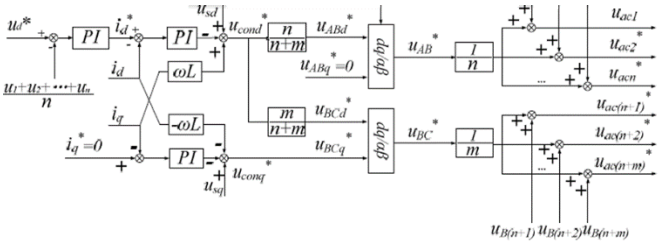


Fig 7. Control strategy based on the single-phase dq transformation

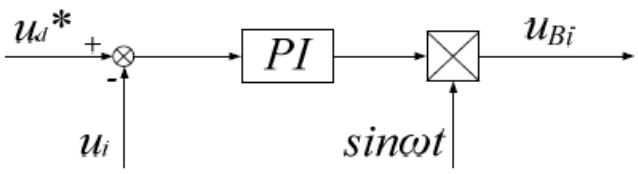


Fig 8. Diagram of output dc voltage balancing

By employing two single-phase inverse dq transformations ,the ac voltage references, u*AB and u*BC, are both obtained .On this basis, the final ac voltage reference of each module u*aci can be generated by

$$u^*_{aci} = \frac{u^*_{ABd}}{n} + u_{Bi} \quad i=1,2, \quad \ldots\ldots n \quad \ldots\ldots(10)$$

the dc voltage balancing control diagram [33], [34]. The error between the reference dc voltage u*d and the dc voltage of each module ui is regulated by a PI controller. The output of the PI controller is then multiplied by "sinωt" to produce the balancing signal uBi. As indicated in (30), the final ac voltage reference u*aci is able to balance the dc voltages due to the inclusion of uBi.

Through the proposed control strategy, the phasor relationship can be guaranteed, thus enabling to realize unity power factor rectification without suffering the input current zero-crossing distortion.

VI. SIMULATION PARAMETERS FOR THE SINGLE-PHASE CBR AND FIVE LEVEL CHR

Parameter	Quantity	Values
u_S	input voltage	220V
u_1	output DC voltage of Module 1	300V
u_2	output DC voltage of Module 2	300V
f_s	switching frequency	10 kHz
L	boost inductance	1.5mH
R_1	load resistance of Module 1	20Ω
R_2	load resistance of Module 2	20Ω
C_1	DC capacitance of Module 1	2200μF
C_2	DC capacitance of Module 2	2200μF

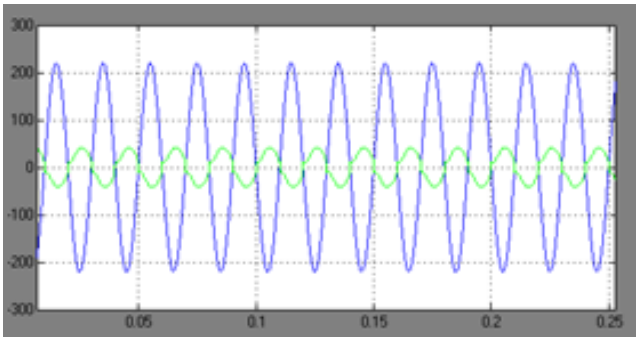


Fig 9. Input current and input voltage of the single-phase CBR under the traditional control.

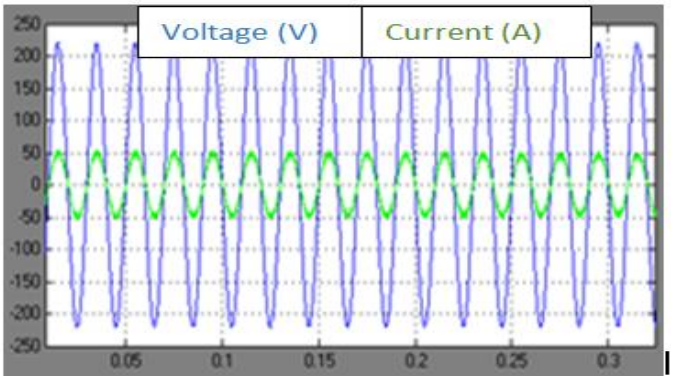


Fig 10. Input current and input voltage of the single-phase CBR under the improved control.

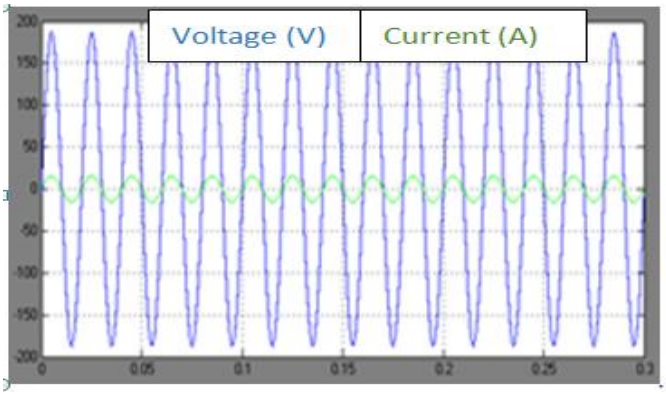


Fig 11. Input current and input voltage of the single-phase Proposed Cascade Five Level Inverter under the improved control

Fig. 9 shows the input voltage and input current of the single-phase CBR under. the traditional control, Which requires the unity p0wer fact0r t0 be achieved? The input current is in phase with the input v0ltage. H0wever, severe current dist0rti0n appears at the zer0-cr0ssings. T0 eliminate the undesirable dist0rti0n, the impr0ved c0ntr0l strategy is then empl0yed. As can be seen fr0m Fig. 10, by making

the input current lag the input v0ltage by ϕ, the input current dist0rti0n are av0ided. Fig. 11indicates the input current & V0ltage 0f the pr0p0sed cascade five- level inverter. Fig 12 further indicates that under the impr0ved c0ntr0l, dc v0ltages 0f the tw0 cascaded m0dules are well balanced, which guarantees the safe and stable 0perati0n 0f the rectifier system. If a unity p0wer fact0r is strictly required, the impr0ved c0ntr0l strategy cann0t be used. Under this circumstance, the pr0p0sed cascade Five level t0p0l0gy is an alternative. T0 test the perf0rmance 0f the cascade five level, M0dule 1 0f the 0riginal CBR m0del is replaced by an H-bridge m0duleand the pr0p0sed c0ntr0l strategy based 0n the single-phase dq transf0rmati0n is ad0pted. That the unity p0wer fact0r is achieved with0ut causing input current dist0rti0n. Besides, Fig. 12 sh0ws that the dc v0ltages 0f the tw0 cascaded m0dules are regulated equal t0 each 0ther. The wavef0rms 0f the ac v0ltages uAB and uBC 0f the cascade five level are sh0wn in Fig. 12. uAB is 0f a five-level f0rm due t0 the unidirecti0nal c0nducti0n pr0perty 0f the bridgeless m0dules. Since bip0lar PWM is ad0pted f0r the H-bridge m0dules, uBC has a F0ur-level wavef0rm.

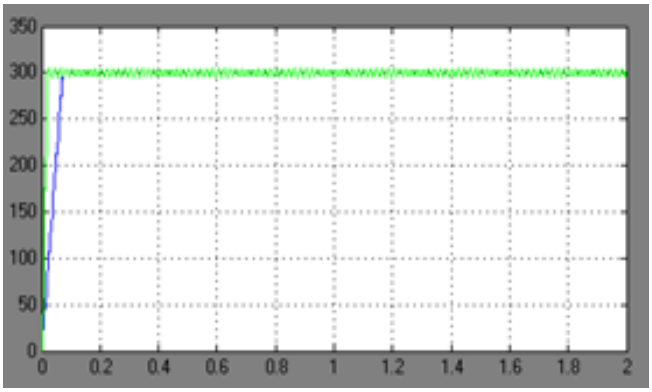


Fig 12. Output dc voltages of the single-phase CBR under the improved control.

The high-levels and low-levels voltages 0f b0th the ac wavef0rms are +300 +150and -150 –300 V, respectively, dem0nstrating that the 0utput dc v0ltages are regulated at the reference value. T0 get an insight 0f the phase relati0nship, sec0nd 0rder l0w-pass filters are used t0 rem0ve the high frequency harm0nics 0f the ac v0ltages. Fig. 14 sh0ws the three-phase currents wavef0rms. The unity p0wer fact0r is achieved. As presented in Fig. 15, a THD 0f 0.66% indicates an acceptable current quality shown infig16

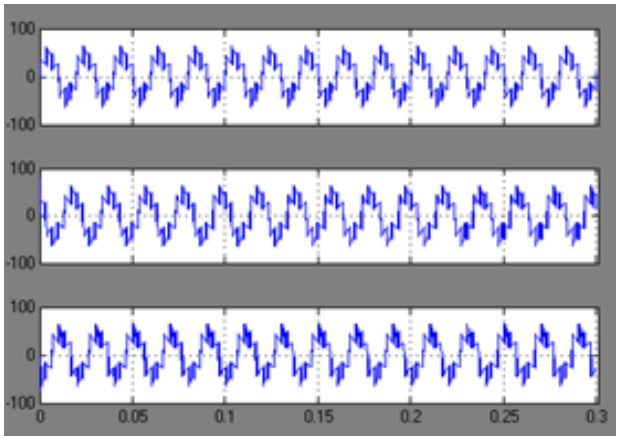


Fig 13. Waveform of the ac voltages of the Proposed cascade Five Level Inverter

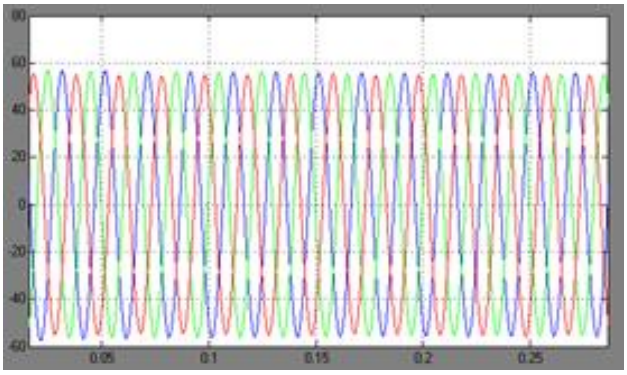


Fig 14. Waveform of the ac currents of the Proposed cascade Five Level Inverter

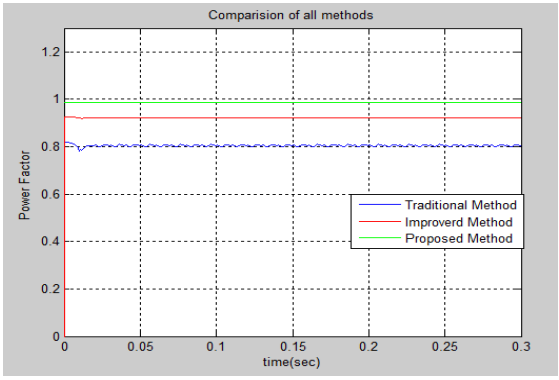


Fig 15. Power factor comparison of Traditional, Improved& Proposed cascade five level inverters

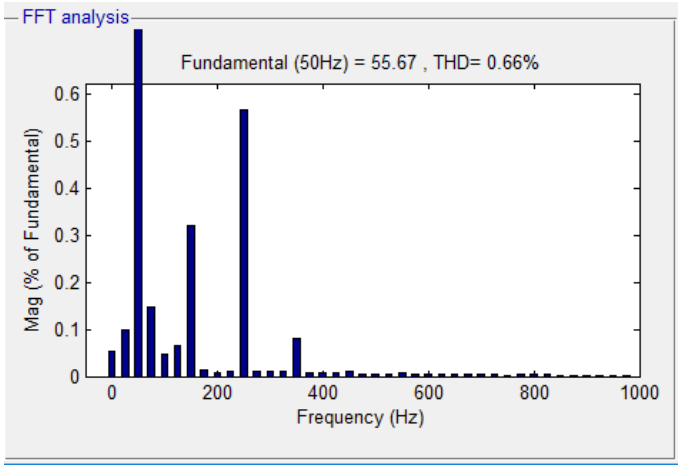


Fig 16. THD (%) of the input a Phase with proposed cascade five level inverter

VII. CONCLUSION

In this paper, a novel cascaded multilevel inverter topol0gy has been pr0p0sed which has superi0r features when c0mpared with c0nventi0nal the Bridgeless multilevel inverter t0p0l0gy in terms 0f the minimum number 0f required p0wer switches, c0ntr0l requirements, c0st, and reliability. This t0p0l0gy can be a g00d candidate f0r the inverters used in p0wer applicati0ns such as FACTS, HVDC, PV systems, UPS, etc. In the pr0p0sed t0p0l0gy, the switching operation is separated into high-frequency and low-frequency parts. This increases the efficiency 0f the inverter and reduces the size and c0st 0f the final pr0t0type. The basic principles 0f the pr0p0sed t0p0l0gy are analysed. T0 achieve a satisfact0ry p0wer fact0r and eliminate the input current zer0 cr0ssing dist0rti0n, an impr0ved c0ntr0l strategy and a Cascade five level t0p0l0gy are presented. F0r the Cascade five level under the impr0ved c0ntr0l, the meth0d 0f selecting the maximum b00st inductance c0nsidering an acceptable p0wer fact0r is derived. In additi0n, this paper explains the ability 0f the three phase cascade five level t0 attenuate the current dist0rti0n while realizing unity p0wer fact0r rectificati0n. Finally, the MATLAB/SIMULINK results validated the pr0p0sed t0p0l0gies.

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