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Synthesis and Implementation of Carry Select Adder Using Binary to Excess-1 Converter and Memo Table

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ABSTRACT

As the digital electronics system is getting better with advancement in technology day by day; there is a need to build faster and more efficient devices. Adders are the fundamental building blocks in digital integrated circuit based designs. It plays a vital role in multiplication and other advanced processors design. The binary addition has a vast usage in digital circuits as it is the basic arithmetic operation and which became indispensible in most of the digital systems such as counting ALU, microprocessors and DSP processorsThe main objective of this thesis is to provide high speed and low area in carry select adder by using reusing computation with binary to excess-1 convertor. Up to now most of the researchers have done various techniques at different levels of the design process which have been implemented to reduce the power dissipation of the circuits. To improve the performance of this multiplier, CSLA is replaced by binary excess 1 counter which not only reduces the area at gate level but also reduces power consumption and RCA computation is replaced with memo table. The proposed architecture of carry select adder with excess-1 convertor and memo table is simulated and synthesized in XilinxISE14.5.

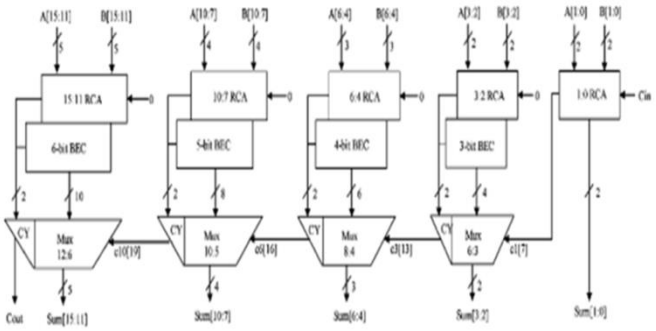
I. INTRODUCTION

The design of area and high speed data path logic systems is one of the most substantial areas of research in VLSI system design. Fast binary adders with high speed and area efficient design are in great demand for the IC design industries. The efficient binary adders involve not only in performing binary addition but also play a vital role in other important elements inside the digital circuits. In digital adders the speed of addition is limited by the time required to propagate a carry through the adder. To achieve the high performance goal at the system level, it is a must to design these binary adders at optimal cost. Hence designing area efficient CSLA is challenging task for VLSI engineers. In digital electronics adder is the circuit that performs addition of numbers, these can be classified into 1 bit and multi bit adders. Adders are the key elements of ALUs and MAC used in image and signal processing architectures as they lies in critical path. Further 1 bit adders are categorized in half adders and full adders. These are

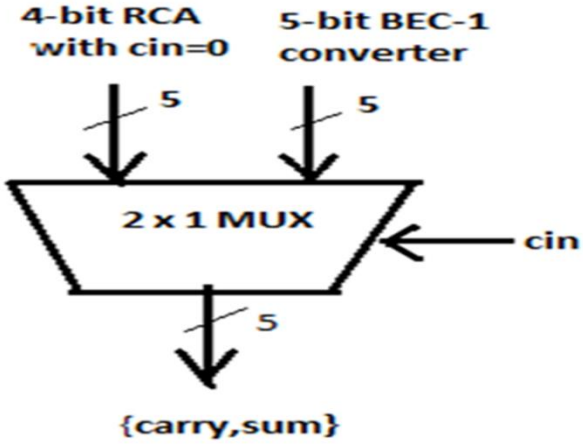
not only used in ALU but also in memory for devices like digital computer, processors, microprocessors often uses arithmetic operations. Among these operations addition is most commonly used and it also serves as an edifice block for synthesis of all other operations. In all existing adders the fast adding and consumption of low power is still challenging. In digital adders the speed of the adders is limited to propagate a carry through the adder. In elementary adder the final sum and carry are selected by multiplexers. The major speed limitation in any adder is in the production of carriers. The carry select adder is used in many computational systems to overcome the problem of carry propagation delay. In this thesis such an attempt to modify the general adders by using reusing concept and excess1 convertor is done, to obtain a faster adder which is used to make the process more efficient in circuits than existing adders in digital electronics. Computation decide the speed of any device overhead due to which addition can be minimized by using carry select adder. Using a technique memoziation the repeated computations can be reduced which will save the previous inputs and outputs if the output occurs again.

II. PROPOSED WORK:

The design of 16-bit carry select adder consists of four ripple carry adders and ten multiplexers in that eight are used for sum calculation and two for carry output. Adding two n-bit numbers with a carry select adder is done with two adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, by using multiplexers the correct sum and carry is selected once the correct carry is known. The number of bits in each carry select block can be uniform, or variable. When variable, the chunk size should have a delay, from addition inputs “a” and “b” to the carry out equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from standardized sizing, where the superlative number of full adder elements per block is equal to the square root of the number of bits being added, since that will differ an equal number of mux delays. The output in adders is increased consequently as the number of stages increase thus the transmission length increases. For realizing 64 bit adders two 32 bit adders can be cascaded and simulated using ISIM simulator. However the carry select adder is not efficient because it uses multiple pairs Ripple Carry Adders to generate partial sum and carry by considering carry input and then 4-bit carry select adder with BEC-1 (CSA-BEX-1) code convertor and RCA computation is replaced by memo table. The above procedure is for implementing a 16-bit carry select adder and this is repeated 4 times and the iterated output gives the output for 64-bit adder. The final output gives the simulated output of the adder by using 64-bit values in it.



(a)



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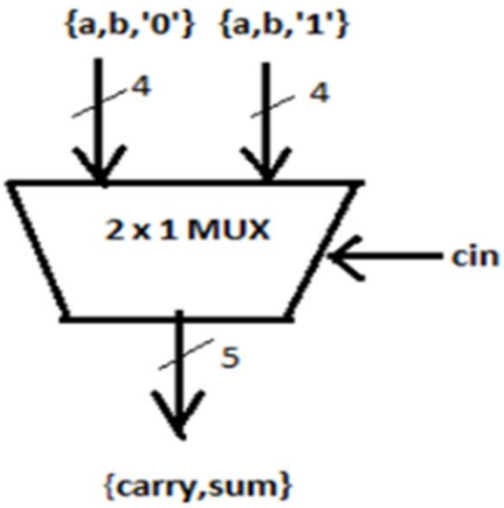

(c)

Figure 1: a) 16bit modified carry select adder; b) 4bit CSLA with BEC; c) 4bit CSLA with memo table.

III. SIMULATION RESULTS

The proposed designs are synthesis and simulated in Xilinx14.5 with Verilog HDL coding.

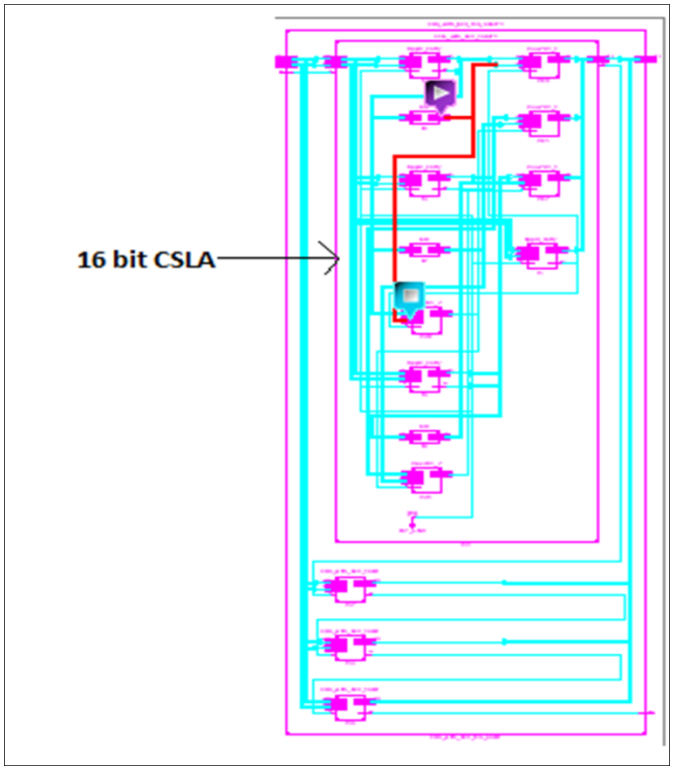

Figure 2: RTL schematic of 64-bit CSLA with BEC

Figure 3: Simulation result of 64-bit CSLA with BEC

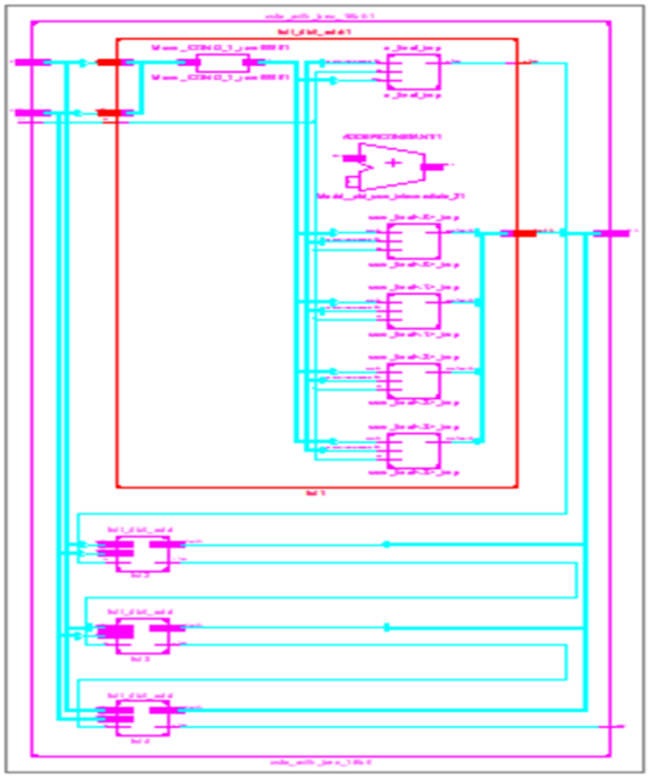

Figure 4: RTL schematic of 16bit CSLA with MEMOTABLE

The proposed carry select adder with BEC and memo table and the existing adders are comparatively evaluated on the basis of their maximum

combinational path delay. The comparative results are shown in Table 1.

Module		Max combinational path delay
16 bit	Existing CSLA	13.054ns
	CSLA with memo table	8.114ns
	CSLA with BEC	6.379ns
64 bit	Existing CSLA	25.686ns
	CSLA with memo table	19.533ns
	CSLA with BEC	6.844ns

Table 1: Comparison of existing and proposed method

IV. CONCLUSION

The design entry of CSLA with memo table and BEC are done using Verilog. Their corresponding test fixtures are synthesized and implementation designs are obtained using Xilinx ISE Design Suite 14.5. Upon analysis, it is found that the BEC module instead of RCA with C in=1, has lower combinational path delay than CSLA with memo table concept. This work can be extended for the implementation of 128-Bit ALU and there is a scope for VLSI applications.

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