International Conference on Advances in Materials, Computing and Communication Technologies
In Association with International Journal of Scientific Research in Science and Technology
Volume 9 | Issue 1 | Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)

Design of Energy Recovery Flip Flop Using Soft Error Robust Algorithm for Low Power Resonant Clocking Applications

Jeya Pradha K[1], Dr. S. P. Valan Arasu[2]

[1]PG Scholar, Department of ECE, Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, Tamil Nadu, India

[2]Associate Professor, Department of ECE, Dr.Sivanthi Aditanar College of Engineering, Tiruchendur, Tamil Nadu, India

ABSTRACT

The development of a high-performance processor has become a major concern as the semiconductor industry has advanced. One of the most important aspects of almost any optical signal processing program is flip flop. The Soft Error Robust Algorithm is used to model the low-power Energy Recovery Flip Flop in this project. To achieve low power dissipation, the SCCER Flip Flop's basic building block is constructed using the SVL algorithm. The Energy Recovery Flip Flop saves a lot of power while the Flip Flops are idle, and there's no visible overhead compared to the original flip flop. Compared to D-Flip Flop using SVL algorithm, SCCER Flip Flop saves 34.2% of power using SVL algorithm. Thus the simulation results have shown that the proposed Energy Recovery Flip Flop using Soft Error Robust offers low power consumption and can be well suited for Low Power Resonant Clocking applications. Simulation is performed using the Tanner EDA tool in 180nm technology and the results indicate a major improvement in Low power consumption.

Keywords: SCCER Flip Flop, CMOS process technology, SVL algorithm, Soft Error Robust

I. INTRODUCTION

Flip-flops are important components in modern electronics devices used in computers, networking, and a number of other uses. Data is stored using flip-flops and latches. A flip-flop is a computer that stores a single bit (binary digit) of data in one of two states: "one" and "zero". In electronics, such data storage can be used for state storage, and such a circuit is known as sequential logic. As a consequence, among the different methods of implementation, there are various techniques designed to resolve issues such as power consumption reduction, clock delivery, area, and cost Flip-flops may be edge-triggered or level-triggered (asynchronous, translucent, or opaque) (synchronous or clocked).The term "flip-flop" has long been used to refer to both level- and edge-triggered circuits that use gates to store a single bit of data. A level-sensitive flip-flop is referred to as a translucent latch in this language, whereas an edge-triggered flip-flop is merely referred to as a flip-flop. The expression "flip-flop" refers to a computer that

holds a single bit of data in any terminology. To eliminate ambiguity, the words "edge-triggered" and "level-triggered" may be used.

II. REVIEW OF LOW POWER CONSUMING FLIP FLOPS

According to Moore's Law, as the feature size of CMOS technology shrinks, designers are able to fit more transistors into the same integrated circuit. Power usage and timing concerns have been a major problem in the contemporary semiconductor industry as a result of the widespread use of mobile devices. When the number of transistors increases, so does the amount of switching and, as a result, the amount of power dissipated. One of the major packaging problems in this era is heat, which is one of the primary reasons for stressing the need for low-power design methodologies and practices.

2.1 SINGLE ENDED CONDITIONAL CAPTURING ENERGY RECOVERY FLIP FLOP

Single Ended Conditional Capturing Energy Recovery flip flop (SCCER) is a single ended version of the DCCER flip flop. The assessment course on the right hand side is static and does not require conditional capturing. Charge sharing is minimized when MN3 is stacked over MN4.The power consumed during sleep (clock gated) mode for 50 percent data switching operation has been shown. As the clock gating is added to the flip-flop during the idle state, significant power savings are observed. As compared to the power consumption without clock gating, power savings of over 1000 times can be seen during the idle state.

2.2 CONDITIONAL DATA MAPPING FLIP FLOP

Conditional Data Mapping Flip-Flops (CDMFFs) are a class of low-cost, high-performance flip-flops that reduce dynamic power by mapping their inputs to a configuration that avoids redundant internal transitions. At data operation, d-CDMFF consumes less than half of the minimum power in the differential category. The use of conditional circuitry in the data path, which provides more power reduction as data operation is reduced, contributes to CDMFFs' excellent power reduction capability. The CDMFF has the disadvantage of being 34% larger than the SCCER Flip Flop.

2.3 STATIC DIFFERENTIAL ENERGY RECOVERY FLIP FLOP

An energy recovery clock is used to run the SDER flip-flop. Evaluation happens as the clock voltage approaches the clock transistor's (MN1) threshold voltage. At the start of the evaluation, a small voltage difference between the Fixed and RESET nodes resulted from the discrepancy between the differential data inputs (D and DB).The cross coupled inverter amplifies the original minor voltage difference, causing the SET or RESET switches to go low. The set/reset latch (cross coupled NAND gates) captures this state transformation and holds it for the remainder of the loop before the next assessment. At low data switching operations where the data does not change constantly, which results in significant power usage.

2.4 CATHODE VOLTAGE SWITCH LOGIC

The modern CVSL flip-flop is great in terms of silicon region gained and number of transistors used, since it uses only 8 transistors, compared to 14 transistors in Yuan's flip-flop and 18 in a traditional structure. This flip-flop configuration is created by changing the Yuan flip-first flop's stage as follows, the input stage's third clocked transistors are replaced with clock operated n-type pass transistors. When the clock is at 0, no floating nodes are left to be pulled up by the Pl-P2 transistor. The inverter and N3-N4 transistors,

which hold the internal nodes of the flip-flop at zero potential, are removed from the first stage, while the transistor (NC1) is inserted. Both flip-flops have similar delay characteristics, but the latest CVSL flip-flop has uniform and lower power consumption characteristics with respect to load and frequency. Thus, presented the new CVSL Flip-Flop as a better alternative to the conventional flip-flop.

III. FLIP FLOP DESIGN USING ENERGY RECOVERY LOGIC

To minimize power dissipation, a Flip Flop was constructed using Single Ended Conditional Capturing Energy Recovery Logic (SCCER) and the Self Voltage Level (SVL) algorithm. To reduce the propagation delay of the Flip Flops, SCCER FF with the SVL algorithm was used. In nanoscale ASICs and systems-on-chips with improved functionality and die sizes, an energy recovery or resonant clocking scheme is very appealing for saving clock capacity .Because of Moore's rule, which reduces node capacitance and supply voltage, nanoscale integrated circuits are more susceptible to radiation-induced single case upsets (SEUs) or soft errors. Soft error stable flip-flops built on Quatro latches that can operate with an energy recovery sinusoidal clock at ultra-low power. The suggested conditional-pass Quatro (CPQ) and true single phase clock energy recovery (TSPCER) FFs are built on a Quatro latch, which is a special soft error resilient latch. Ultra Low Power Resonant clocking technique and soft error robust logic has been designed using CMOS process technology to reduce the power dissipation and propagation delay.

3.1 SELF VOLTAGE LEVEL ALGORITHM

The SVL technique is used to minimize leakage capacity in clocked systems such as flip flops when they are in standby mode, i.e. when the clock is zero. The SVL process uses PMOS and NMOS transistors to simulate a pull-up or pull-down mechanism. The gate of a pull-up transistor is attached to the complement of the clock signal, while the gate of a pull-down transistor is connected to the clock. The supply voltage to the D flip flop is regulated by a clock signal in this technique to minimize leakage capacity .As a result, the term "self voltage standard" is appropriate.
When clock = 1, clock bar=0, and Psw1 is turned on, Nsw1 is turned off. Vdd would be connected to the clocked circuit. The circuit is in standby mode when clock = 0 and does not need additional power to stay in standby mode .As a result, the clocked circuit leakage capacity is minimized in standby mode (i.e. when clock = 0).

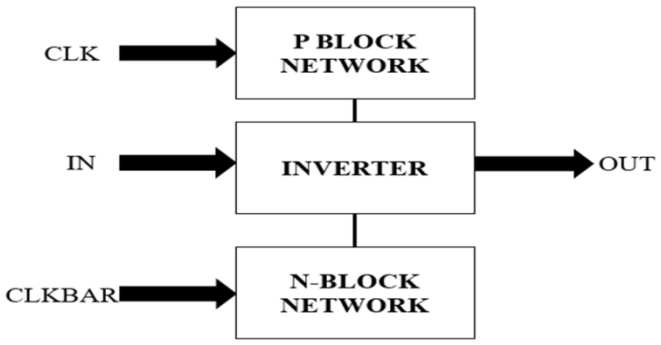

FIGURE 3.1 Block Diagram of SVL Algorithm

3.2 SCCER FLIP FLOP USING SVL ALGORITHM

SVL Algorithm is used to reduce leakage power in clocked systems like flip flops during standby mode of operation.
SCCER flip flop is connected with complement of clock signal and pull down transistors gate terminal is connected with clock. This technique to reduce leakage power uses a clock signal as the control signal to control supply voltage. The circuit is in standby mode when clock = 0 and does not need additional power to stay in standby mode. Hence even if we reduce the supply voltage during standby mode it will work perfectly fine and power consumption will be reduced, especially the leakage power that flows when transistors are in off state will be reduced. As clock = 0, Nsw2 is turned off. When used as a pull down, the PMOS transistor gives a poor logic '0', i.e. it provides Vth at the output. Since Psw2 is a PMOS

transistor with a pull-down connection rather than a ground connection, it will have a finite voltage at the node's "true ground."

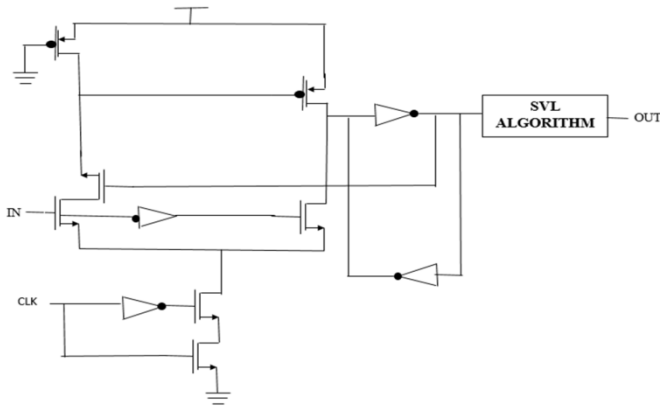

FIGURE 3.2 Block Diagram of SCCER Technique with SVL algorithm

3.3 LEAKAGE CONTROLLED TRANSISTOR TECHNIQUE

The Leakage Regulated Transistor suggested a new strategy for reducing power leakage in VLSI circuits using CMOS technology. The integration of Sleepy stacked with the LECTOR technique is proposed as a new improved leakage power reduction technique. For power consumption reduction, the current method utilizes a mixture of Pull up and Pull down logic architecture. The two transistors are added in logic circuit based on the two SCCER flip flop design network circuit. This transistor design will provide the path resistance for the ground to supply connection. The circuit's leakage current will be held to a minimum with this resistance. The sleepy signal is fed into Vcc through a parallel link with a Pull up and Pull down logic circuit, where the sleepy signal waveform is delivered to both transistors. The engineered circuit would work successfully in both active and standby modes. Increase the resistance in the direction from the source to the ground as well. It is introduced using SCCER FF Logic, which decreases power usage by allowing transistors to swing between secure voltage values to avoid unnecessary power consumption.

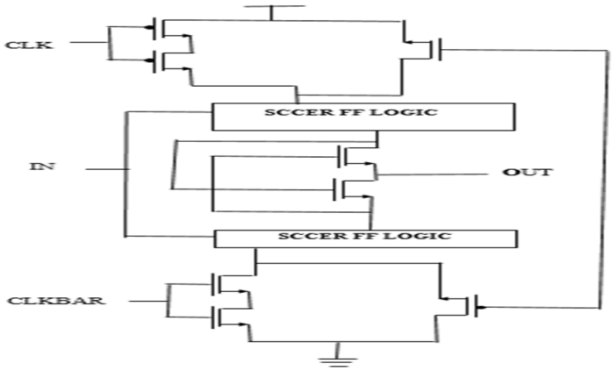

FIGURE 3.3 Block Diagram of LECTOR Technique

3.4 EFFICIENT CHARGE RECOVERY LOGIC TECHNIQUE

Along with SCCER logic, effective charge recovery logic (ECRL) is proposed as a candidate for low-energy adiabatic logic circuits. The energy recovery mechanism is demonstrated using an ECRL (Efficient Charge Recovery Logic inverter) and SCCER with SVL logic inverter. Holds clk=1 in the initial condition, and Mn1 is conducting (Q=0). Over conductive transistor Mp2, the output Q matches the deviation of PC as it increases from 0 to Vdd.

As the PC hits the Vdd value, it holds Q=1 and Q=0, which are true logic states at the next stage's inputs. For a practical loading and service frequency spectrum, the suggested rationale indicates a four to six times power reduction.A supply clock generation circuit based on inductors is proposed.The circuits are made with 1.0-micron CMOS technology and a 0.2-volt threshold voltage.

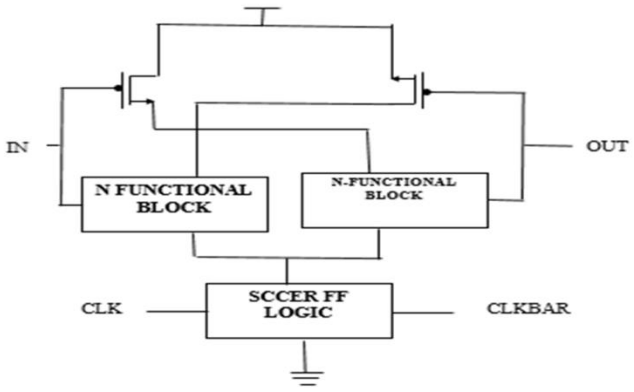

FIGURE 3.4 Block Diagram of ECRL Technique

3.5 EMBEDDED LOGIC FLIP FLOP

The proposed Embedded Logic Flip Flop architecture allows logic functions to be embedded within the flip-flop. The ELFF's operation can be broken down into two phases: assessment and pre-charge. During the assessment process, the CLK is high, but during the pre-charge phase, it is low .During the assessment process, the actual latching happens while the CLK and CLKB are at a 1–1 overlap state. For the remainder of the evaluation process, the first cross-coupled inverter holds the node X1 at a low stage. As a result, the PMOS transistor PM1 keeps the node X2 elevated during the evaluation cycle. The circuit reaches the pre-charge process when the CLK becomes low. Then, by PM0, the node X1 is pulled high, shifting the condition of the first cross-coupled inverter. The ELFF has an asynchronous performance reset that enables counters and registers to be easily enforced. When compared to the current DDFF-ELM structure, ELFF has improved power dissipation and delay efficiency.

As opposed to current logic flip-flop architectures, the ELFF outperforms them by 20%.

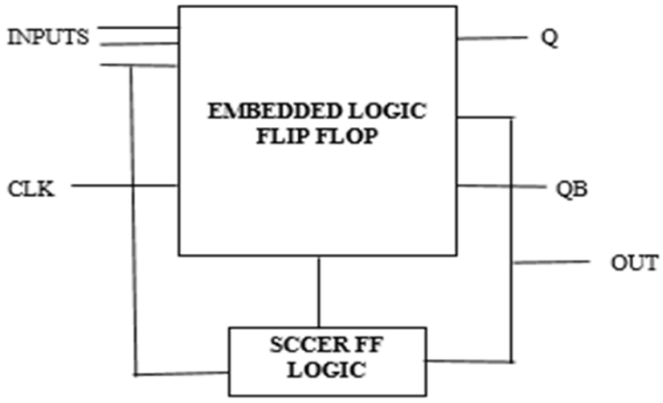

FIGURE 3.5 Block Diagram of ELFF Technique

3.6 MCML TECHNIQUE

A current mode logic clutch with a sample and keep state at each of the clock signal's logic stages.The transistor pairs N1 and N2 are used to sense information in the tracking mode, while transistor pairs N3 and N4 are used to store the details. The circuit runs in monitoring mode while the clock at the Gate of N5 is high; however, when the clock is low, N6 switches on to trigger the hold pair transistor. Present Mode MOS for both traditional and proposed D-latches, logic techniques and SCCER flip flops include clock to output delay and data to output delay as a function of data to clock delay. It is worth noting that the proposed design's clock to output delay increases linearly with data to clock delay, and the value is lower than the traditional one. The data to output delay, on the other hand, is observed to be almost independent of the data to clock gap and to be much smaller than the traditional latch. This brings us to the end of our strategy for achieving a higher data volume.

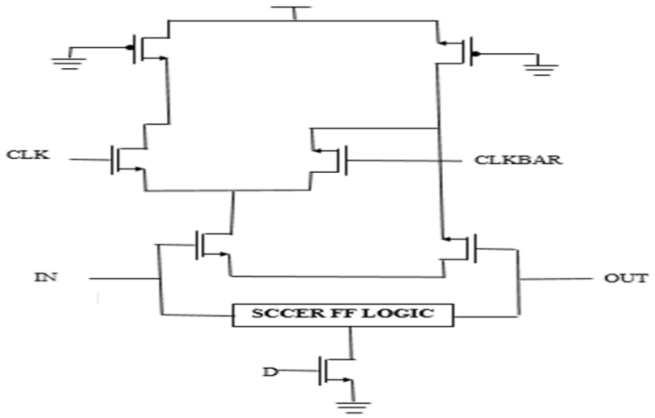

FIGURE 4.6 Block Diagram of MCML Technique

3.7 CONDITIONAL PASS QUATRO FLIP FLOP

The Conditional Pass Quatro has an input transfer unit, Storage unit, and output stage. During the Clk and Clkb signal overlap, the input stage delay factor opens a small transparency window that allows data and its complement to transfer and be written to the storage cell. In this case, the MCML technique is the holding unit.The output stage is made up of a two-transistor, two-input inverter that allows the SET to spread to the output while masking it.To transfer logic "1" or "0" data to the output, the input stage delay factor (three inverters) produces a small time window using Clk and Clkb signals at the rising edge of the Clk signal. When the storage cell at the 0 → 1

transition of the input Clk signal. If the FF is storing a "1", the voltages at internal nodes A, B, C, and D are "0", "1", "0", and "1". For a stored value of "0", the node voltages are "1", "0", "1", and "0".

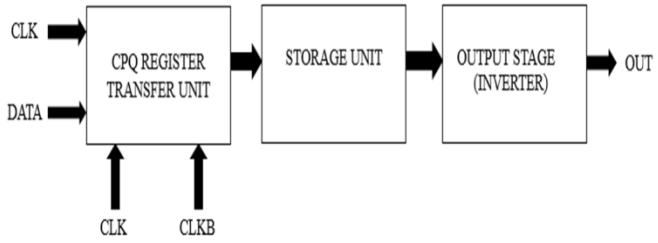

FIGURE 4.7 Block Diagram of CPQ Flip Flop

3.8 TSPC ENERGY RECOVERY FLIP-FLOP

Soft error stable True Single Phase Clock Energy Recovery (TSPCER)A new TSPC register switch unit, a single node SEU hardened Quatro cell, and a two-input, two-output stage inverter are all included in the FF. The register stage is in precharge mode when Clk="0." Node "X" precharged/discharged to complement of data during the precharge process, while node "Y" precharged to "1."The transfer unit is in the assessment process at the rising edge of Clk. If data = "1," node "X" = "0," node "Y" = "1," node "B" pulled down to low at the rising edge of the Clk signal at the start of the evaluation process. Nodes (B, D) = "0" drive the output inverter, resulting in a large output.

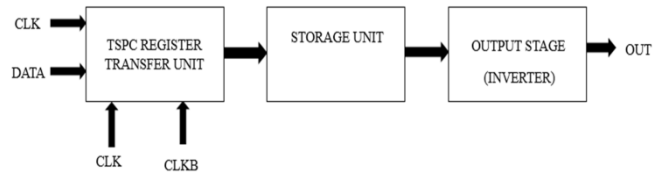

FIGURE 4.8 Block Diagram of TSPCER Flip Flop

IV. RESULTS AND DISCUSSION

The Flip Flops are designed based on CMOS process technology as shown in Table 4.1.The performance parameters such as power, delay and PDP (Power Delay Product) of Flip Flops are also analyzed.

Table 4.1 Performance comparison of Flip Flops

EXISTING LOGIC	POWER(µw)	DELAY(s)	PDP
SCCER FF	12.27	1.65	20.2455
CDMFF	16.86	2.19	36.9234
SDER FF	12.86	1.17	15.0462
CVSL FF	14.29	1.89	27.0081

Table 4.2 Performance comparison of SVL Logic

PROPOSED LOGIC	POWER(µw)	DELAY(s)	PDP
SCCER FF using SVL Algorithm	4.15	3.65	15.1475
CDMFF using SVL Algorithm	20.3	1.73	35.119
SDER using SVL Algorithm	18.6	1.21	22.506
CVSL using SVL Algorithm	25.1	1.74	43.674

The above Table 4.2 shows the performance comparison of various Flip Flops in terms of power and delay. The SCCER FF using SVL Algorithm shows significant improvement in power and delay of about 34.12% and 13.91 % respectively.

Table 4.3 Performance comparison of Low Power Design Techniques

PROPOSED LOGIC	POWER(µw)	DELAY(s)	PDP
LECTOR	4.15	2.03	8.4245
ECRL	5.56	6.62	36.80
MCML	3.79	1.49	5.6471
ELFF	5.19	2.07	10.74

The above Table 4.3 shows the performance comparison of various Low Power Design Techniques in terms of power and delay.

Table 4.4 Performance comparison of Low Power Resonant Clocking

PROPOSED LOGIC	POWER(µw)	DELAY(s)	PDP
CPQ FF	23.26	2.40	55.824
TSPCER FF	20.07	2.00	40.14

The above Table 4.4 shows the performance comparison of various Low Power Resonant Clocking in terms of power and delay.

V. SIMULATION RESULTS

5.1 SINGLE ENDED CONDITIONAL CAPTURING ENERGY RECOVERY FLIP FLOP (SCCER)

The schematic of SCCER flip flop is shown in Fig. 5.1.In this flip flop, 8-bit IN and CLK are given as input and the corresponding 8-bit output is obtained.

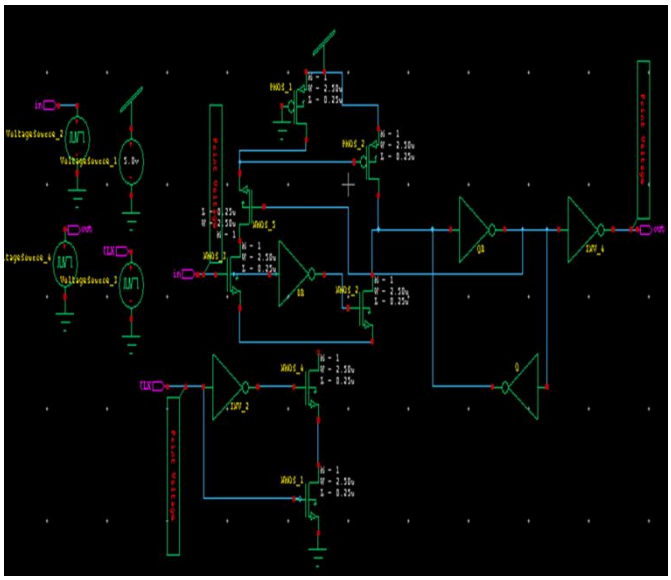

FIGURE 5.1 Schematic of SCCER Flip Flop

Figure 5.2 shows the power and delay analysis of the SCCER flip flop. The total power consumption is 12.27µw.The delay of the SCCER flip flop is 1.65s.

```
Power Results

VVoltageSource_1 from time 1e-009 to 1e-007
Average power consumed -> 4.801493e-002 watts
Max power 2.383247e-001 at time 2.1e-008
Min power 1.859443e-002 at time 4.0875e-008

VVoltageSource_2 from time 1e-009 to 1e-007
Average power consumed -> 1.227949e-007 watts
Max power 1.392673e-004 at time 3.1e-008
Min power 0.000000e+000 at time 2.1e-008

Measurement result summary
Parsing                         0.01 seconds
Setup                           0.04 seconds
DC operating point              0.07 seconds
Transient Analysis              0.73 seconds
Overhead                        0.79 seconds

Total                           1.65 seconds
```

FIGURE 5.2 Power and delay analysis for SCCER Flip Flop

5.2 SCCER FLIP FLOP USING SVL ALGORITHM

The schematic of SCCER flip flop using SVL algorithm is shown in Fig. 5.3.In this flip flop, 8-bit IN, CLK and CLKBAR are given as input and the corresponding 8-bit output is obtained.

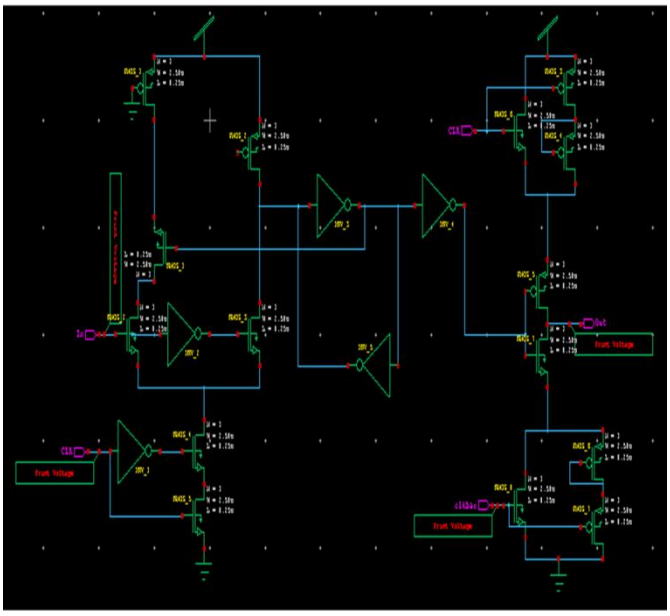

FIGURE 5.3 Schematic of SCCER Flip Flop using SVL Algorithm

Figure 5.4 shows the power and delay analysis of the SCCER Flip Flop using SVL Algorithm. The total power consumption is 4.18µw.The delay of SCCER Flip Flop using SVL Algorithm is 3.65s.

```
VVoltageSource_5 from time 1e-009 to 1e-007
Average power consumed -> 4.183044e-006 watts
Max power 2.188053e-004 at time 6.1e-008
Min power 0.000000e+000 at time 1.1e-008

Measurement result summary
Parsing                          0.01 seconds
Setup                            0.02 seconds
DC operating point               2.04 seconds
Transient Analysis               2.75 seconds
-----------------------------------------------
Total                            3.65 seconds
```

FIGURE 5.4 Power and delay analysis for SCCER flip flop using SVL algorithm.

5.3 MOS CURRENT MODE LOGIC

The schematic of MOS Current Mode Logic is shown in Fig. 5.5.In this flip flop, 8-bit IN, CLK and CLKBAR are given as input and the corresponding 8-bit output is obtained.

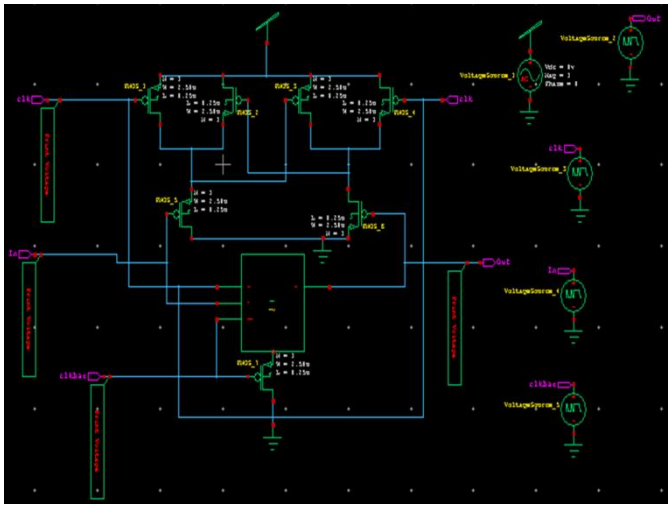

FIGURE 5.5 Schematic of MOS Current Mode Logic.

Figure 5.6 shows the power and delay analysis of MOS Current Mode Logic. The total power consumption is 3.79µw.The delay of MOS Current Mode Logic is 1.49s.

```
VVoltageSource_4 from time 1e-009 to 1e-007
Average power consumed -> 3.797409e-006 watts
Max power 1.858238e-004 at time 6.1e-008
Min power 0.000000e+000 at time 1e-009

VVoltageSource_5 from time 1e-009 to 1e-007
Average power consumed -> 6.589340e-006 watts
Max power 4.789938e-004 at time 5.1e-008
Min power 0.000000e+000 at time 1e-009

Measurement result summary
Parsing                          0.02 seconds
Setup                            0.07 seconds
DC operating point               0.10 seconds
Transient Analysis               0.66 seconds
Overhead                         0.65 seconds
-----------------------------------------------
Total                            1.49 seconds
```

FIGURE 5.6 Power and delay analysis for MOS Current Mode Logic.

The output waveform of MOS Current Mode Logic is shown in Figure 5.7.

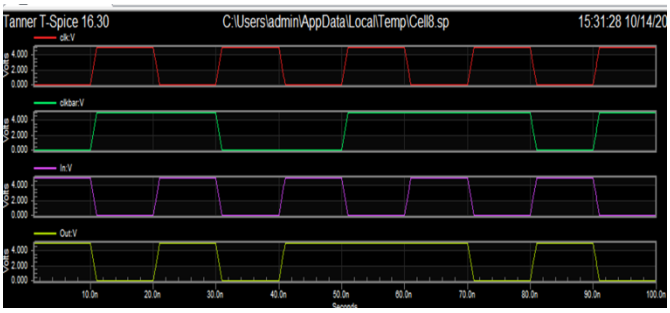

FIGURE 5.7 Simulation waveform for MOS Current Mode Logic.

5.4 TRUE SINGLE PHASE CLOCK ENERGY RECOVERY (TSPCER) FF

The schematic of True Single Phase Clock Energy Recovery (TSPCER) FF is shown in Fig. 5.8.In this flip flop, 8-bit IN, CLK and CLKBAR are given as input and the corresponding 8-bit output is obtained.

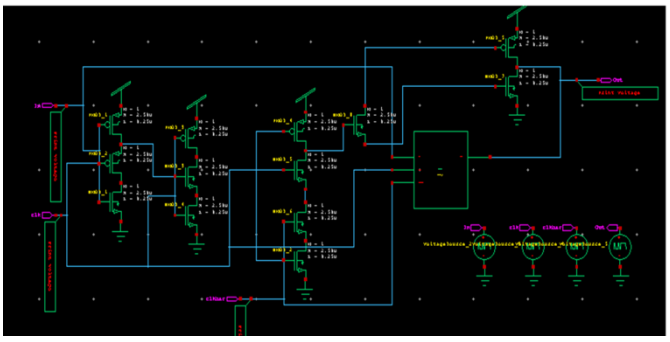

FIGURE 5.8 Schematic of True Single Phase Clock Energy Recovery (TSPCER) FF.

Figure 5.9 shows the power and delay analysis of. The total power True Single Phase Clock Energy Recovery (TSPCER) FF consumption of is 20.07μw. The delay of True Single Phase Clock Energy Recovery (TSPCER) FF Flip Flop is 2.00s.

```
Power Results
VVoltageSource_3 from time 1e-009 to 1e-007
Average power consumed -> 2.007958e-007 watts
Max power 3.234334e-003 at time 1.1e-008
Min power 0.000000e+000 at time 1e-009


Parsing                          0.13 seconds
Setup                            0.35 seconds
DC operating point               0.03 seconds
Transient Analysis               0.59 seconds
Overhead                         0.90 seconds
-----------------------------------------
Total                            2.00 seconds
```

FIGURE 5.9 Power and delay analysis for True Single Phase Clock Energy Recovery (TSPCER) FF.

VI. CONCLUSION

The proposed Energy Recovery Flip Flop using Soft Error Robust model having Low power was designed. SCCER Flip Flop using SVL algorithm is designed and implemented based on circuit techniques to achieve a low power. SCCER Flip Flop using SVL algorithm saves 34.12% of power and 13.91% of delay as compared to that of D-Flip Flop logic using SVL algorithm. LECTOR technique was designed using the SCCER Flip Flop as its building block and stacking transistor has been applied to achieve this. LECTOR technique along with SCCER Flip Flop using SVL algorithm saves 26% of power as compared to that of LECTOR technique using pull up and pull down logic. ECRL technique along with SCCER Flip Flop using SVL algorithm saves 11% of power compared to that of ECRL technique using N- functional block. MCML technique along with SCCER Flip Flop using SVL algorithm saves 20% of power compared to that of Current Mode Logic. ELFF technique along with SCCER Flip Flop using SVL algorithm saves 25% of power compared to that of ELFF using NMOS logic. CPQ Flip Flop using MCML technique saves 52.91% of power as compared to that of CPQ Flip Flop using Quatro Latch. TSPCER Flip Flop using MCML technique saves 31.03% as compared to that of TSPCER Flip Flop using Quatro latch. Thus, it has been observed from the simulation results that the proposed TSPCER Flip Flop provide low power consumption and can be well suited for resonant clocking application.

VII. REFERENCES

[1]. Arkadiy Morgenshtein, Alexander Fish and Israel A. Wagner (2004),' AN EFFICIENT IMPLEMENTATION OF D-FLIP-FLOP USING THE GDI TECHNIQUE' 0-7803-8251-X/04/$1.00 ©2004 IEEE.

[2]. Ayesha Firdous, M.Anand and B.Rajan (2017),' Design and Implementation of Enhanced Leakage Power Reduction Technique in CMOS VLSI Circuits' International Journal of Applied Engineering Research ISSN 0973-4562 Volume.

[3]. Heng You, Jia Yuan, Weidi Tang, Zenghui Yu and Shushan Qiao,' A Low-Power High-Speed Sense-Amplifier-Based Flip-Flop in 55 nm MTCMOS' Electronics 2020, 9, 802; doi: 10.3390/electronics9050802.

[4]. Madhu Shakya, Shweta Agrawal (2018),' Design Low Power CMOS D-Flip Flop using modified SVL Techniques' International Journal of Research and Analytical Reviews (IJRAR).

[5]. Madhusudan Maiti, Anupama Paul, Suraj Kumar Saw, Alak Majumder (2020),' A Dynamic Current Mode D-Flip Flop for High Speed Application' DOI: 10.1109/IEMENTech48150.2019.8981081@2020 IEEE.

[6]. Mashkoor Alam, Rajendra Prasad (2013),' A Noble Design of Energy Recovery Flip-Flops' Journal of Engineering Research and Applications.

[7]. R.Sivakumar, D.Jothi (2014),' Recent Trends in Low Power VLSI Design', International Journal of Computer and Electrical Engineering.

[8]. Riadul Islam, 'Low-Power Resonant Clocking Using Soft Error Robust Energy Recovery Flip-Flops' Received: 3 January 2018 / Accepted: 12 June 2018 © Springer Science Business Media, LLC, part of Springer Nature 2018.

[9]. Sudheer A, Ajith Ravindran (2014),' Design and Implementation of Embedded Logic Flip-Flop for Low Power Applications' International Conference on Information and Communication Technologies (ICICT 2014).

[10]. Yash Vardhan, Dhruv Nair, M. Vinoth Kumar(2017),' Design and analysis of flip flop for low power VLSI applications' - A Review International Journal for Research Trends and Innovation.