International Conference on Advances in Materials, Computing and Communication Technologies
In Association withInternational Journal of Scientific Research in Science and Technology
Volume 9 | Issue 1 | Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)

Scaling Theory Model for Ferroelectric Surrounding Gate TFET Using Negative Capacitance

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ABSTRACT

In this paper, an analytical model for modified Ferroelectric Surrounding Gate Tunnel FET with gate stack engineering and different gate metals has been developed. Furthermore, taking advantage of Gate stack engineering's scaling advantages and dual material engineering's high degree performance, the two have been combined in a novel structure known as Surrounding Gate (SG) Tunnel FET with stacked oxide SiO2/high-k and dual material (DM). By solving 2D Poisson's equation with matching device boundary conditions, the two-dimensional (2D) potential at the surface and electric field mathematical models for the DMSG TFET are constructed. A mathematical expression for the band-to-band (BTB) Tunnelling generation rate is obtained using Kane's formula, and then used to compute the drain current. The impact on the proposed device performance due to the variation of different device parameters has also been studied. The mathematical results have been verified using the simulated results obtained from ANSYS, a 3-D device simulator. In addition, the modelled TFET is implemented by using inverter circuit.

Keywords: Tunnel field effect transistor (TFET), Stacked Gate, Analytical Modelling, Poisson equation, Surface potential, Electric field.

I. INTRODUCTION

The evolution of tunnel field effect transistors (TEFTs) which is commonly known as TFET or surface tunnel transistors (STTs) is the consequences of such innovative research. MOSFET as a switching device was being employed extensively until and unless TFET came into existence. TFET works on band-to-band Tunnelling mechanism and not only has it provided sub-threshold slope less than 60 mV/decade, but also shows promising result for low power application. Previous work on analytical Modeling of TFET using double gate TFET in indicated or evinced improved result for ON current while OFF current remains in fempto or pico ampere range. Double gate TFET is dependent on drain potential and these new findings is investigated earlier. High gate dielectric and thin film structure boost ON current and the significance of using both in DG TFET is shown in previous work. An Ultra-thin silicon body over

insulator tunneling field effect transistor structure. Now here in order to boost this ON current to a greater extent surrounding gate TFET using cylindrical structure is prepared and assumed ON current to be improvable.

Few developments are proposed to hold up the scaling law proposed with the aid of Gordon Moore as Tunnel FET (TFET) is one of the most trusted devices to substitute a MOSFET for nano-scale regime. Moreover, the unique properties of Tunnel FET such as low leakage current (IOFF), sub-60 mV/decade sub-threshold swing (SS), high-quality immunity towards short channel effects and its compatibility with the CMOS process make it an appropriate substitute for ultra low power applications. However, the ON-current (ION) in TFET is restricted due to the band to band tunneling (BTBT) phenomenon, making it unsuited to meet the increased demand for high speed with low power consumption applications. Many thoughts have been proposed to improve the ION current of TFET. This includes a variety of TFET device structures with more than one gate SS such as double, triple, all round gates, junction less TFETs etc. are being proposed and investigated. However, for correct evaluation and investigation of structural and electrical characteristics of TFET, an analytical model study is extremely essential.

In this work, the scaling advantages of gate dielectric engineering and dual material surrounding gate (SG)-TFET are incorporated into a novel structure called dual Material Surrounding Gate (DMSG) Tunnel FET with stacked high-k/SiO2 oxide layer has been proposed to improve the ON current ratio. High-k dielectrics oxides are used for decreasing gate oxide leakage current and SiO2 interfacial layer is used between high-k dielectric and silicon channel to reduce the phonon scattering and improve carrier mobility. Hence, analytical potential, electric field model are derived in this paper. The parabolic approximation technique is used to work out the 2D Poisson's equation with suitable boundary conditions. Then on the basis of the Kane's model and electric field expression, the drain current of proposed device is obtained. Finally the performance of the device structure has been compared with Surrounding gate TFET in terms of ION current.

II. FERRO ELECTRIC TUNNEL FET

Cylindrical gate tunnels-FET (CG-TFET) are extremely promising devices in the area ofhigh-speed integrated circuits for optical communication systems and in analog microwavecircuits for mobile communication systems and play an important role in defense applications.Ferroelectric cylindrical gate tunnels, in particular, are emerging as excellent candidates for potential use at microwave frequencies due to the material properties of Ferroelectric such asthe high maximum electron velocity, saturation speed and thermal stability. It has been shownthat the proposed model correctly predicts the potential distribution and electric field along the channel.

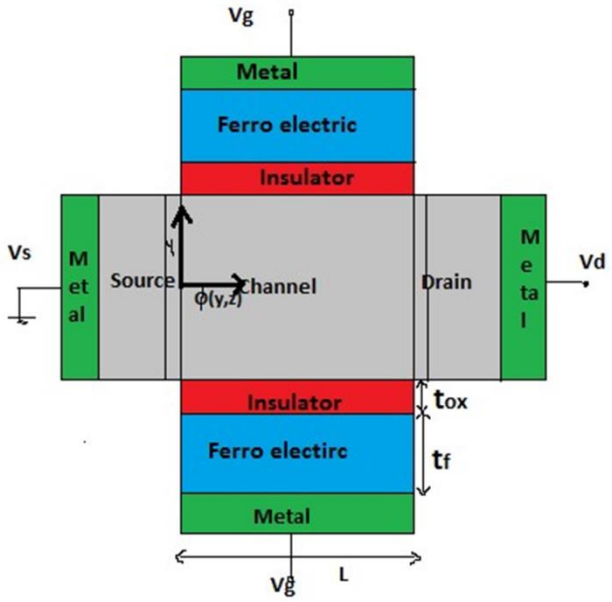

Figure.2.1 Cross Sectional view of Ferro electric TFET

The introduction of ferroelectric material into the device improves the performance ofthe device by showing a progressive increase in surface potential at the metal interface. In addition, the analytical

modeling of the threshold voltage, electric field and drain current isperformed for the Ferroelectric cylindrical gate tunnel of FET by using the Negative capacitance.In the proposed model, the effect of important parameters such as the thickness of the barrierlayer and its doping on the threshold voltage was also included. The model also extends to findan expression for the electric field and discharge the current in the submicron regime.

III. NEGATIVE CAPACITANCE CG-TFET

The effects of short channel (SCE) in small geometry transistors have received considerable attention in recent years due to the drive towards smaller devices for faster and denser integrated circuits. The solution of Poisson's 2-D equation for NC CG-TFET was obtained using several approaches. However, the continuous scaling of the devices is leading the NCCG-TFET to the regime of short channels (for lower supply voltage and high speed operations) and lower width (for lower power consumption and higher density) NC CG-TFET. These devices, called NC CG-TFET with reduced geometry. However, since the size of the device is reduced toeless than one micron, it becomes more difficult to develop a numerical model for it.

By reducing the size of the device, two-dimensional and three-dimensional electrostatic effects tend to degrade the device's performance in terms of threshold voltage, a key parameter in the design of NC CG-TFET circuits. Although the modeling of the SCE device is quite mature, the modeling of NC CG-TFET with reduced geometry has not been done so far, although the effects of reduced width become predominant when the width of the device is reduced. This is because the three-dimensional nature of the problem makes the analysis very difficult and slow. Therefore, a precise 2D analytical model is required to predict the current ON/OFF ratio of reduced Ferroelectric Negative capacitance CG-TFET geometry that simultaneously incorporates both SCE and reduced width effects. In this paper, a simple and accurate threshold voltage is introduced, as well as an analytical model of the drainage current for geometric NC CG-TFETs, using the standard variable separation method to solve the Poisson 2-D equation. This also provides the 2D potential and the electric field analysis and drain current analysis of the proposed model.

IV. DEVICE STRUCTURE

Negative Capacitance Cylindrical tunnel FETs (NC CGTFET) are extremely promising devices in the area of high-speed integrated circuits for optical communication systems and in analog microwave circuits for mobile communication systems. Negative Capacitance CGTFETs,in particular, are emerging as excellent candidates for potential use in microwave frequencies due to the properties of the ferroelectric material, such as the high maximum electron velocity, saturation velocity and thermal stability. It is a trend in composite semiconductor technology to continually develop faster, smaller and high power consumption devices for the same level of integration. Improving device integration technology requires a rapid resizing of device dimensions.

The proposed system employs both the gate dielectric engineering as well as dual material gate engineering techniques. The cross-sectional view of the proposed device is shown in Fig 2.1, which consists of two gate materials of different work functions with gate stack. The source and drain regions are very highly doped p+ and n+ respectively. The center channel region is intrinsic material which is made up of a lightly doped n-type material. In this structure, the gate electrode is made of two materials M1 and M2 of different work functions. These two different materials are deposited over respective gate lengths L1 and L2.

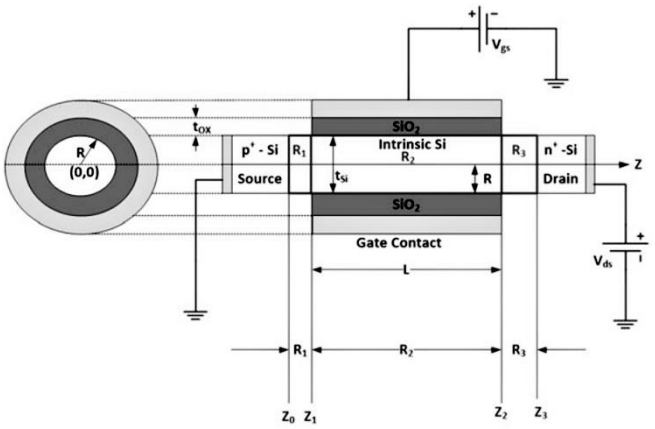

Figure.4.1 Schematic cross section of the surrounding gate n-channel tunnel FET

V. MODEL FORMULATION

Modeling of Surface potential

The surface potential∅(r,z)is solved by the 2-D Poisson equation in the cylindricalcoordinate system

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\emptyset(r,z)\right)+\frac{\partial^2}{\partial z^2}\emptyset(r,z)=\frac{qN_c}{\varepsilon_{si}}$$

∅(r,z)is 2-D surface potential; r is radial direction, z is distance along the channel, εsi ispermittivity of silicon.

ni -intrinsic carrier concentration-quasi potential, Vt-thermal voltage.

The Channel Surface potential is given by

$$\emptyset_s(r,z)=\emptyset_s(r=R,z)$$

The Surface Potential at the source end is given by

$$\emptyset(r,z=0)=\frac{\emptyset_s(z)}{z}=0=V_{bi}$$

The Surface potential at the drain end is given by

$$\emptyset(r,z=L)=\emptyset_s(z)/z=L=V_{bi}+V_{ds}$$

First boundary conditions

$$c_{11}(z)=0$$
$$c_{12}(z)=0$$

$$c_{21}(z)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{GS1}-\emptyset_{s1}(z)}{2Rt_{ox}}$$
$$c_{22}(z)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V_{GS2}-\emptyset_{s2}(z)}{2Rt_{ox}}$$

The charge–voltage characteristic of the ferroelectric material is expressed by using the LK equation.

$$G_f=u_0K+v_0K^3+w_0K^5$$

Here K is the charge per unit area of the ferroelectric layer, Gf voltage across the ferroelectriclayer, u0,v0,w0 co-efficient of ferroelectric material.

Modeling of Electric Field and Subthreshold Swing

The electric field along the channel E can be written as,

$$E=\frac{d}{dr}\emptyset(r,z)/r=0=0$$

Electric field at the silicon and stacked oxide interface is given by

$$\frac{d\emptyset(r,z)}{dr}/r=R=\frac{\varepsilon_{ox}}{\varepsilon_{si}R}\left(\frac{(\varphi_G-\emptyset_s(z))}{\ln\left(1+\frac{t_{ox}}{R}\right)}\right)$$

$$t_{ox}=t_{ox}+\frac{\varepsilon_{ox}t_{hk}}{\varepsilon_{hk}}$$

Simple scaling equations can be obtained as

$$\frac{d^2\emptyset_{deff}(z)}{dz^2}+\frac{V_{Gs}-V_{bi}-\emptyset_{deff}(z)}{\frac{1+B-Cd^2_{eff}}{4C}}=\frac{q_{Nc}}{\varepsilon_{si}}\frac{1+A}{1-B+Cd^2_{eff}}$$

$$\lambda_4=\sqrt{\frac{\varepsilon_{si}t_{ox}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{2R}-\frac{\varepsilon_{si}}{t_{si}t_{ox}}d^2_{eff}\right)}$$

In this λ4 is the Sub-threshold swing and scaling factor for High k/SiO2 stacked Dual material surrounding gate TFET's including effective conducting path effect.

Modeling of Drain Current

This section developed the mathematical expression for the drain current (Id) of theFerroelectric CG TFET being studied. First, we will find the minimum tunnel length, animportant parameter to develop the drain current model. The length of the tunnel is the lengthbetween two equi-energtic points: one in the valance band and the other in the conduction band of the tunnel junction, where the BTBT takes place.

$$I_{DS}=qS_{TL}W_{ch}X\bar{A}_E^{2.5}\exp\left(-\frac{Y}{\bar{E}}\right)$$

$$S_{TL}=\frac{t_0}{\lambda}\ln\frac{\left[(V_s-\phi_0(t_0)/\cos\lambda)\right]+\sqrt{\left[(V_s-\phi_0(t_0)/\cos\lambda)\right]^2-4ab}}{2a}$$

Where Wch is the channel width of the proposed device. A and Y are the tunneling parameters,A=4*10^14cm-12 and Y=1.9*10^7 V/cm

and E is the average electric field . STL is the shortesttunneling length.

Using the Kane's model for the BTBT generation rate of carriers, the current of the proposed device is calculated analytically.

CIRCUIT IMPLEMENTATION

NC FERRO ELECTRIC TFET INVERTER

A TFET inverter or NOT gate inverts the input and is similar to CMOS-based inverters. It consist of a p-type device as the pull-up network and an N-type device as the pull-down network. For an inverter, when the input VIN is 0V, the PTFET is switched-on, the NTFET is switched-off and the output VOUT is driven to VDD through the PTFET, thus inverting a logic 0 to a logic 1.When the input VIN is 0.6V, the PTFET is switched-off, the NTFET is switched-on and the output is discharged to the value at Gnd (0).

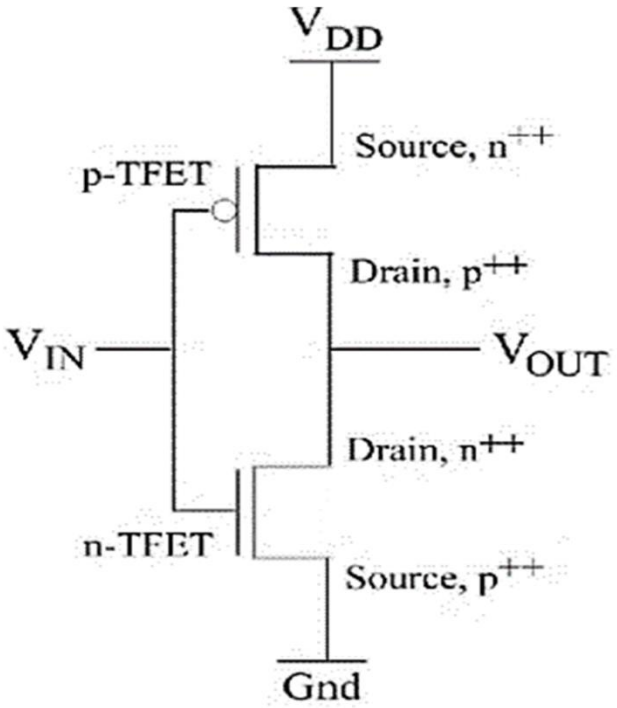

Figure 5.1 Circuit Diagram of NC Ferro Electric TFET

The circuits were designed in ANSYS (HFSS) designer tool., design parameters were set in the ISE,and the simulation was performed using Xilinx Simulator tool. It is to be noted that there is no body terminal for TFET devices. Therefore, factors such as body effect or variable threshold voltage are not considered.

Schematic Diagram

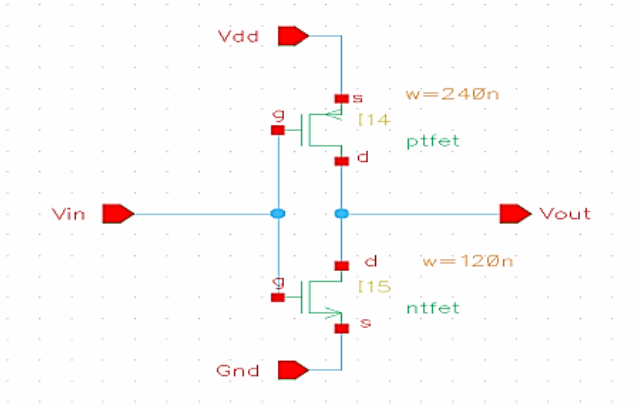

Figure 5.2 Schematic Diagram

Fig 5.2 shows the schematic diagram of NC Ferro Electric TFET inverter.The supply voltage (Vdd) is set to 1V and Vss is connected to ground.

The Transient response is shown

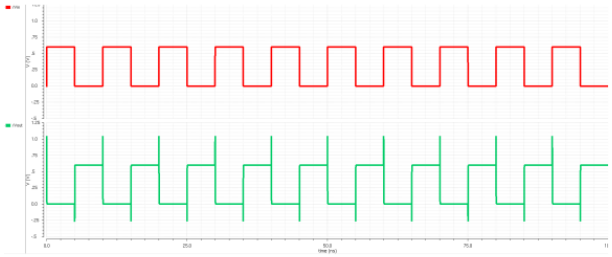

Figure 5.3 TFET inverter Transient Response

Power Analysis

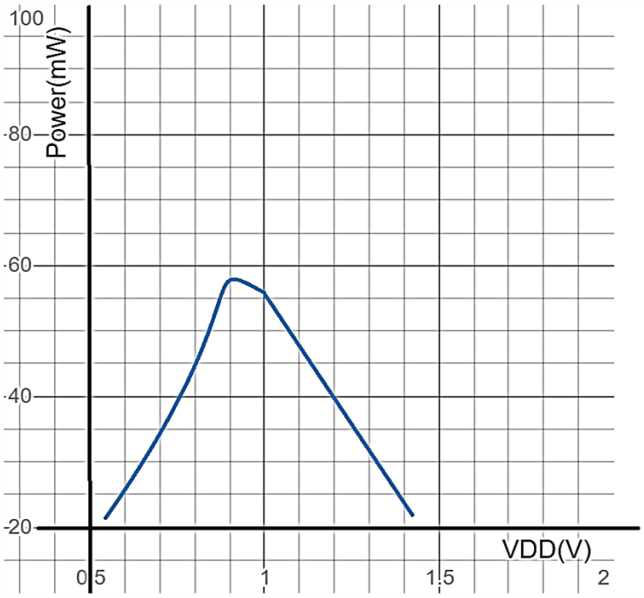

Figure 5.4 Power of NC Ferro electric TFET

The power analysis for NC Ferro electric TFET is 50 Micro Watt as shown in figure.

VI. SIMULATION RESULTS AND DISCUSSION

Table 6.1 Device parameters for simulation

PARAMETERS	VALUE
Silicon film radius (tsi)	6nm
Oxide thickness(tox)	1nm
Ferroelectric thickness(tf)	2nm
Channel length(L)	60nm
Source/drain extension length	20nm
Source doping	1020/cm3
Channel doping	1016/cm3
Drain doping	5*1018/cm3

Surface Potential Analysis

The accuracy of the proposed model is validated by comparison. The results with the ANSYS simulation data. Study the electrical behavior of NC CG TFET, models like Recombination, Concentration and Lombardi dependent on theelectric field, narrowing of the band non-local model and BTBT were used in the ANSYS simulation tool. the surface potential of the new device along the channel improved surface potential is observed due to the polarization effect while polarization as the gate voltage isapply the movement of charges along the channel increases and the proposed NC CG TFET isgive a better performance compared with the conventional CG TFET are shown in Figure 6 .1.

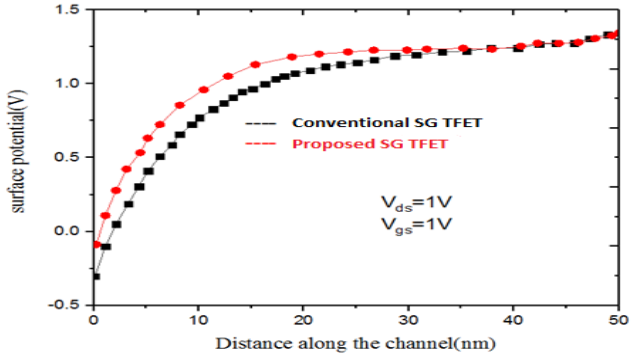

Figure.6.1Comparison surface potential for proposed NC GC TFET and conventional model CG TFET

Electric field analysis

Figure 6.2 shows the electric field analysis X-axis is referred distance along the channel and inY-axis referred lateral electric field .It can be found that NC CG TFET yields 26.5% improvementin the lateral electric field at the tunnel junction as compared with the conventional DGTFET. The tunneling energy barrier width is reduced by the high electric field as well as the on current can be obtained.

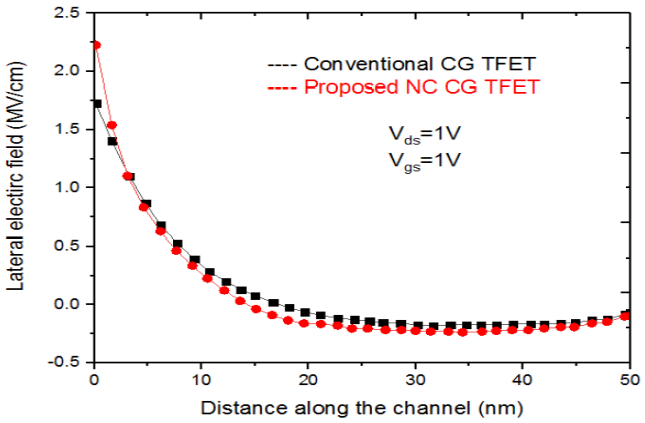

Figure.6.2 Lateral electric field for the Proposed and conventional CG TFET

Drain Current Analysis

Fig.6.3 shows the comparison between Drain current as a function of the Gate voltage VGS for Proposed and conventional TFETs. indicates that NC CG TFET provides higher IDS as compared to CG TFET devices, owing to its higher carrier transport efficiency attributed by the increase inthe average Electric Field produced by the gate-material engineering. The peak in the electricfield profile leads to a rapid acceleration to the carriers at the interface of metals, resulting inenhanced carrier transport efficiency to supply more and more carriers to reach the drainterminal. However, it is worth mentioning that an increase in the drain current causes anincrease in the sub-threshold leakage current and a decrease in the sub-threshold swing, whichneeds to be minimized for ultra low power device applications at Vgs = Vds = 1 V.

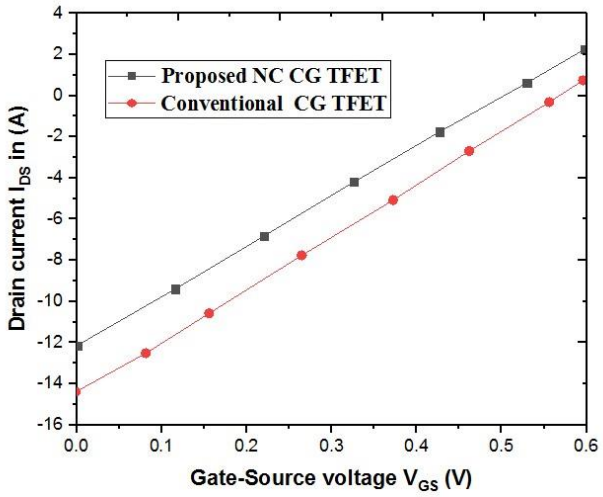

Figure.6.3 Drain current performance for proposed and conventional TFET

Threshold voltage analysis

Fig 6.4 show that the threshold voltage (VTh) variation as a function of channel radius for NC CG TFET and CG TFET. it is evident that NC CG TFET provides higher efficacy to VTh roll-off ascompared to CG TFET for increase in channel radius with a fixed channel length. Fig 6.4 revealsthat as the Si channel thickness increases for both NC CG TFET and CG TFET devices, thegate loses its control over the channel carriers while the drain gains more control on the sameleading to decrease in the threshold voltage. Therefore, in order to achieve a small reduction ofthreshold voltage with gate length downscaling, the Si channel thickness needs to be optimizedto a small value.

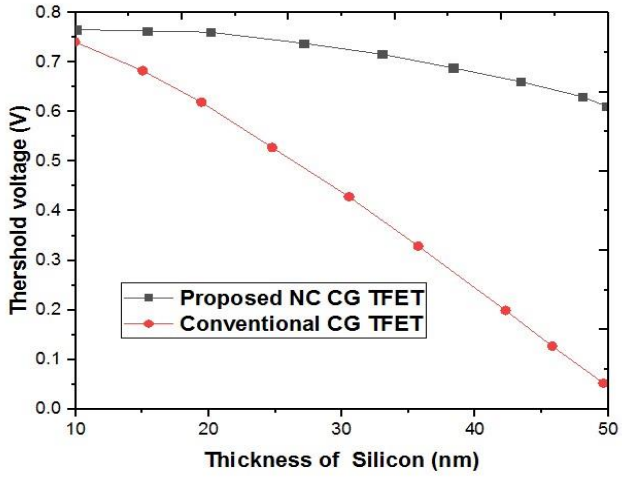

Figure.6.4 Threshold voltage analysis

Sub threshold swing

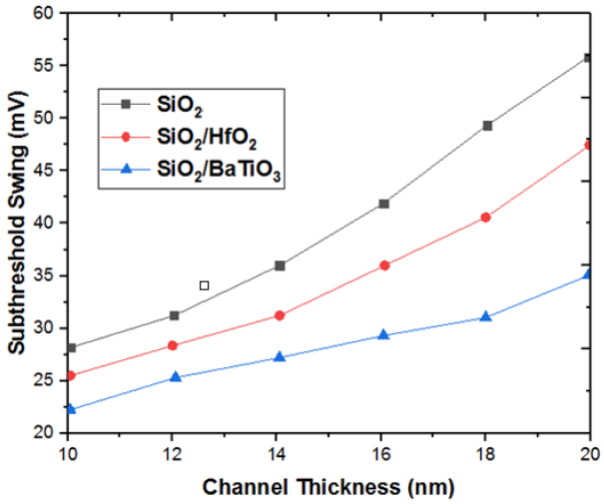

Figure.6.5 Subthreshold swing versus channel thickness at fixed Vgs=Vds=1

Fig 6.5 shows variation of sub-threshold swing (SS) with channel thickness for NC CG TFET. From the figure, it is observed that SS increases with channel thickness and decreases Si channel ofNC CG TFET structures. It is basically due to drain current increases. It gives lowering the Tunneling volume with channel thickness.

VII. CONCLUSION

This work presents the analytical surface modeling for Negative capacitance cylindrical gate TFET, including the effect of mobile charge carriers in this effect is used to analyze the device performances, such as surface potential ,electric field, threshold voltage and subthreshold swing. The On state current of Negative capacitance cylindrical gate TFET increases and ferroelectric layer increases due to the reduced shortest tunneling length.. The surface potential model is used to model the minimum tunnel length Finally, the ID is improved. NC CG TFET is developed. The surface potential ,electric field and drain current are studied. The results of the model are validated by comparing with ANSYS simulation data.Then the cicruit is implemented with NC Ferro Electric TFET.By using Xilinx Software Power has been analysed.

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