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Low Power Design of MIPS RISC Processor

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ABSTRACT

The aim of the paper is to design a reversible control unit for 32 bit RISC processor using VHDL code. RISC or Reduced Instruction Set Computer is a design philosophy that has become a mainstream in scientific and engineering applications. Increasing performance and gate capacity of recent FPGA devices permits complex logic systems to be implemented on a single programmable device. Low power design of MIPS processor involves the use of reversible logic based design. The circuit of control unit is synthesized using Xilinx ISE. The parameters such as power and delay are estimated. The work is proceeded with the reversible logic based implementation.

Key words: MIPS, reversible logic, VHDL, control unit, datapath unit.

I. INTRODUCTION

The need for low power design for control unit and data path design of a MIPS RISC processor is an increasing demand in many applications. By Moore's law, the number of transistors is doubled every 18 months. But the exponential increase in transistor count can increase the heat dissipation. Minimizing heat dissipation lead to development of reversible logics which can yield no information loss due to one to one mapping between input and output. The conventional logic gates are irreversible and have information loss, leading to heat dissipation.

Any Microprocessor and Microcontroller are designed by utilizing the two computing architectures, which are Complex Instruction Set Computing (CISC) and Reduced Instruction Set Computing architectures (RISC). The CISC processor architecture depends on Instruction Set architecture. The CISC processor utilizes the more number of operands and addressing modes in its instruction set. The RISC processor uses a less number of directions compared with the CISC processor. Comparing to CISC, RISC CPU have more advantages, such as faster speed, simplified structure, and easier implementation and so on. RISC CPU is extensive use in embedded system. The MIPS processor structure depends on the RISC processor. The processor utilizes the 5 pipeline stages, which are Instruction Fetch (IF), Instruction Decoder (ID), Execute (EX), Memory Access (MEM) and Write Back (WB). The MIPS single-cycle processor plays out all the pipeline stages in one clock cycle. This work involves the design of a reversible MIPS processor. The design includes a reversible control unit and a reversible data path unit.

II. LITERATURE REVIEW

Galrani Tina, R.D [1] designed to performance Improvement of MIPS Architecture by Adding New Features. The main features of RISC processor are the instruction set can be improved to speed instruction execution. No microcode is needed for single cycle execution. All instructions are fixed bit in length. This simplifies the instruction fetch mechanism since the location of instruction boundaries is not a function of the instruction type. .The RISC approach allows 32 bit processing power to be offered at much lower cost than was possible with a CISC, because of the smaller die size required to implement the processor.

T.Subhaahini, M.Kamaraju, K.Babulu [2] designed the single cycle Risc Micro Architecture Processor Using Clock Gating Technique. RISC based architectures are widely used to achieve low power. This work presents designing of single cycle RISC micro-architecture processor using clock gating technique. The single cycle processor performs the tasks of instruction fetch, instruction decode, execution, memory access and write-back all in one clock cycle. The RISC processor is designed for both single cycle and multi cycles by using the concept of MIPS. he main features of RISC processor are the instruction set can be improved to speed instruction execution. No microcode is needed for single cycle execution.

Preetam Bhole, Hari Krishna Moorthy[3] designed FPGA implementation of low power 32-bit RISC processor. The RISC 32 - bit processor architecture using Clock gating technique to perform the logical memory and branching the instruction. The different blocks are using to fetch, decode, execute, and memory read/write to execute four stage pipelining. The Harvard architecture used which contains memory space for data and program. To reduce the power of RISC core, clock gating technique is used in the architectural level as an effective low power method.

Vishala A.Tyamanavar, Jayashr C.Nidagundi [4] designed FPGA implementation of a 32 – bit MIPS processor. The most important feature of the RISC processor is that this processor is very simple and support load/store architecture. The important components of this processor include the Arithmetic Logic Unit, Shifter, Rotator and Control unit. The RISC processor is designed for both single cycle and multi cycles by using the concept of MIPS.

Sarika U. Kadam, S.D. Mali [5] proposed a 16-bit RISC processor using a parallel programming language called VHDL. It is simulated and synthesized using Xilinx ISE 13.1i. Pipelining is used to make processor faster. In Pipelining instruction cycle is divided into parts so that more than one instruction can be operated in parallel. Number of instructions is designed for this processor. When the proposed work compared with previous processors, it can be seen that proposed processor has less delay.

Pranjali S. Kelgaonkar, ShilpaKodgire [6] implemented the design of 32 bit MIPS RISC Processor. The purpose of RISC microprocessor is to execute a minuscule batch of instructions, with the intention of proliferating the celerity of the processor. A Reduced Instruction Set compiler (RISC) is a microprocessor that had been designed to perform a small set of instructions, with the aim of increasing the overall speed of the processor. The RISC processor is designed based on MIPS instruction set. MIPS-based RISC architecture having operations like addition, subtraction, etc.

Mohit N. Topiwala, N. Saraswathi [7], proposed 32-bit MIPS based RISC processor is implemented successfully with pipeline functionalities. Every instruction is executed in one clock cycle with 5-stage pipelining. This design shows the implementation of MIPS based CPU capable of handling various R -type, J-type and I-type of instruction and each of these categories has a different format. These instructions are verified successfully through testbench. Designing Forwarding unit and hazard detection unit to overcome the data dependencies was critical task and

it was implemented successfully. The design is implemented using VerilogHDL and synthesized using Cadence RTL complier using typical libraries of TSMC 0.18 urn technology. Design of MIPS processor is optimized both in timing and area. Also complete ASIC flow till RTL to GDS II have done using Cadence SoC Encounter, and analyzed the complete physical design flow.

Mrs. Rupali S. Balpande and Mrs. Rashmi S. Keote [8] have designed FPGA based instruction Fetch and Decode Module of 32-bit (MIPS) processor. Through analysis of function and theory of RISC CPU instruction decoder module, they designed instruction decoder (ID) module of 32-bit CPU by pipelining.

Soumya Murthy and Usha Verma [9] proposed FPGA based 32 Bit RISC Core using DLX Architecture for power optimization. By using fetch, decode, ALU, comparator, GPR memory, execute, pipelined RISC processor core is developed using DLX architecture. Using low power technique, the processor is designed to reduce power consumption of the core.

V.N.Sireesha and D.Hari Hara santhosh [10]designed FPGA implementation of a MIPS risc processor. The RISC processors the instructions can be executed with the help of stages by using clock cycles. The instruction can be divided into four stages i.e. fetch, decode, execute and write back. The most important feature of the RISC processor is that this processor is very simple and support load/store architecture. The important components of this processor include the Arithmetic Logic Unit, Shifter, Rotator and control unit.The RISC processor is designed for both single cycle and multi cycles by using the concept of MIPS.

III. MIPS DESIGN

MIPS (Microprocessor without Interlocking Pipelining Stages) is a RISC processor that can execute an entire instruction in one cycle. The cycle time is limited by the slowest instructions. The RISC processor architecture consists of Arithmetic Logic Unit (ALU), Control Unit (CU), Barrel Shifter, Booth's Multiplier, Register File and Accumulator. RISC processor is designed with load/store architecture, meaning that all operations are performed on operands held in the processor registers and the main memory can only be accessed through the load and store instructions.

One shared memory for instructions (program) and data with one data bus and one address bus between processor and memory . Instruction and data are fetched in sequential order so that the latency incurred between the machine cycles can be reduced. For increasing the speed of operation RISC processor is designed with five stage pipelining. The pipelining stages are Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Data Memory (MEM), and Write Back (WB).

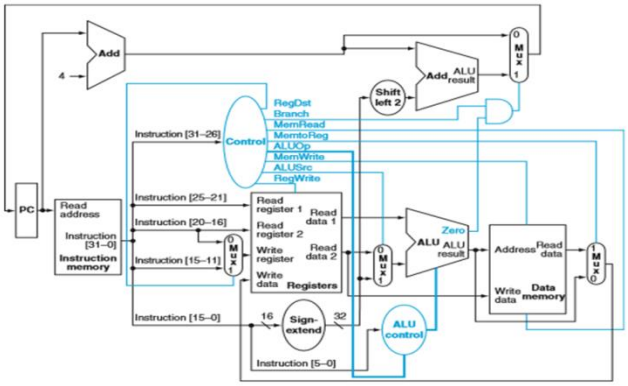


Fig.1 The simple datapath with the control unit

IV. DESIGN OF CONTROL UNIT

The control unit generates all the control signals needed to control the coordination among the entire component of the processor. This unit generates signals that control all the read and write operation of the register file, and the data memory. It is also responsible for generating signals that decide when to use the multiplier and when to use the ALU. Fig.2 shows the block diagram of the control circuit of MIPS processor.

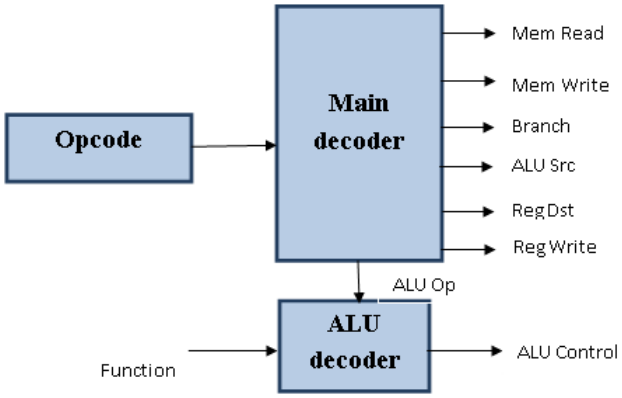


Fig.2 Block diagram of a control unit of MIPS processor

The setting of the control lines is completely determined by the opcode fields of the instruction. Table 1 shows the control signals generated for various groups of instructions such as arithmetic, load/store and branch instructions. Fig.3 shows the logic circuit for the main control unit.

Table 1 Generation of control signals for main control unit

Instruction/ Opcode	RegDst	ALUSrc	Memto-Reg	RegWrite	MemRead	MemWrite	Branch	ALUOp1	ALUOp2
R-format (000000)	1	0	0	1	0	0	0	1	0
lw (100011)	0	1	1	1	1	0	0	0	0
sw (101011)	X	1	X	0	0	1	0	0	0
beq (000100)	X	0	X	0	0	0	1	0	1

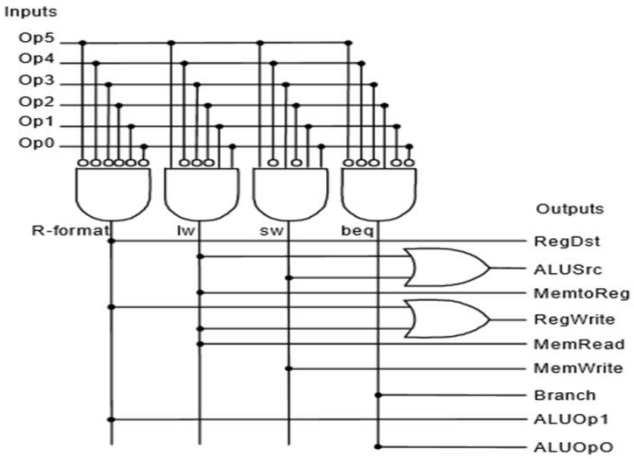


Fig.3 Logic diagram of main control unit

In order to design the logic for this ALU control unit, a truth table is developed. The input of the truth table is a 2-bit ALUOp and a 6-bit Function code, and the output is a 3-bit ALU control signals (Table 2). The logic circuit of the ALU control unit is shown in Fig.3.

Table 2 Generation of control signals for ALU control unit

ALUOp		Funct field						Operation
ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0	
0	0	X	X	X	X	X	X	010
X	1	X	X	X	X	X	X	110
1	X	X	X	0	0	0	0	010
1	X	X	X	0	0	1	0	110
1	X	X	X	0	1	0	0	000
1	X	X	X	0	1	0	1	001
1	X	X	X	1	0	1	0	111

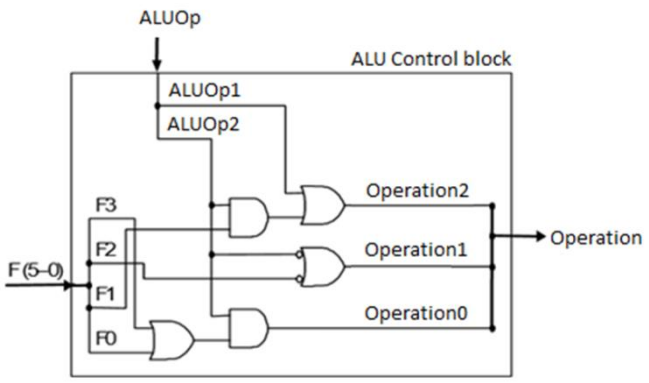


Fig.4 Logic circuit of ALU control unit

Low power reversible logic control unit

Power has become an important aspect in the design of general purpose processors. The RISC processor consume too much power compared with other processor. To minimize the power of control unit in RISC Core, reversible logic technique is used in the architectural level which is an efficient low power technique. Low power consumption helps to reduce the heat dissipation, lengthen battery life and increase device reliability. Low-power embedded processors are used in a wide variety of applications including cars, phones, digital cameras, printers, and other such devices. The reason for their wide use is that they are small; therefore, they do not take up much area and are cost effective to fabricate. There are various low power consumption technique such as clock gating, power gating, reversible logic gate etc. In this paper the design of control unit was done by using logic gate.

Reversible logic gates

A reversible gate realizes a reversible function, computation done by a gate is reversible in nature, that means for a gate g the gate g' implement inverse transformation.

Some of the basic gates are given below:

There are lot of reversible logic techniques. Here we use NOT and Toffoli reversible gates to reduces the power of control unit. A Not gate is a 1×1 reversible gate is shown in Fig.5. The input is A and the output is P = A' which is reversible.

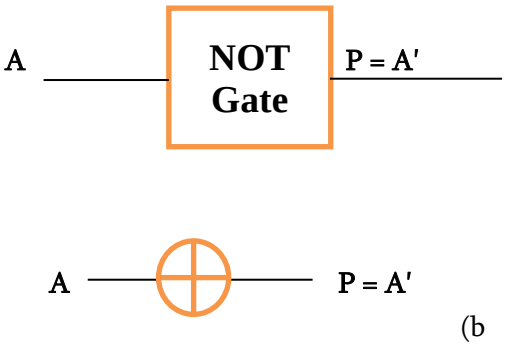


Fig.5 (a) Block Diagram (b) Schematic Representation

Table 3 Truth Table of NOT Gate

Input	Output
A	P
0	1
1	0

Toffoli gate:In 1982 Toffoli give a new gate called Toffoli gate. It is a 3×3 gate and can be generalized up to n×n size. As per definition target line flips when all control lines are set. In this design the Toffoli reversible gate is used .

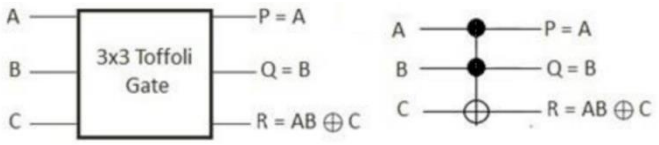
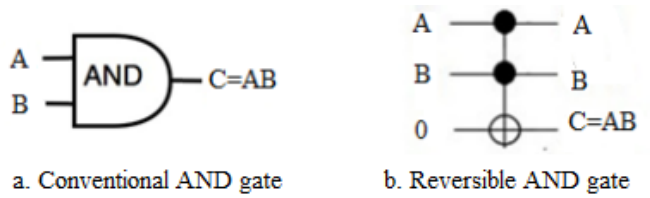


Fig.6:3×3Toffoli gate (a)block diagram (b) schematic representation

Table 4 Truth table of Toffoli gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

By mapping Gate the irreversible logic gates in these main control unit and ALU control unit into reversible logic gates, the power can be minimized. This includes the conversion of conventional irreversible AND, OR gates into a reversible AND, OR gates.



a. Conventional AND gate b. Reversible AND gate

Fig.7 AND gate representations

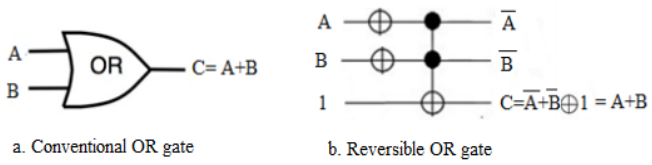


Fig.8 OR gate representations

In Fig.7, third input C is put as '0' in the Toffoli gate to convert it into an AND gate. Similarly, in Fig.8, third input is '1' to obtain the Toffoli gate as an OR gate. These can be included in the design of reversible control unit.

V. SIMULATION RESULT

The simulation results for reversible control unit based MIPS RISC processor for various control bits are shown as in Fig.9. Fig.10 and Fig.11 shows the RTC schematic and Technology schematic with reversible control unit. Table 5 shows the device utilization summary, delay and power for MIPS RISC processor with and without reversible logic.

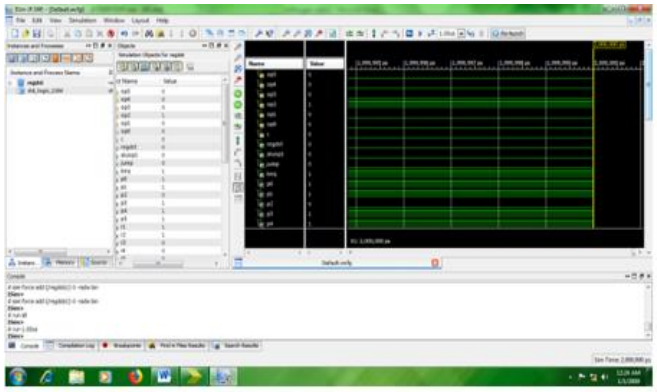


Fig.9 Simulation result for reversible control unit of MIPS RISC processor

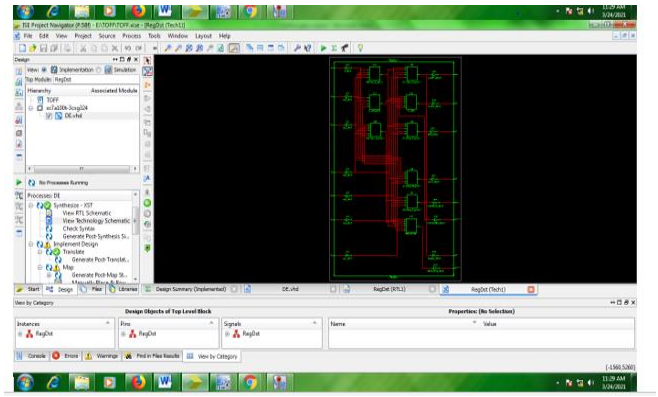


Fig.10 RTL schematic

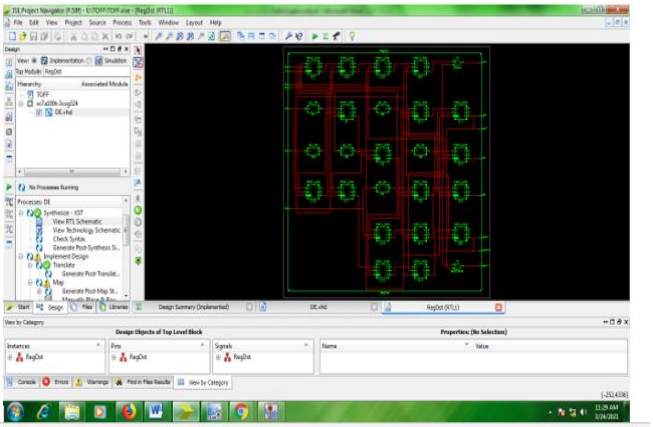


Fig.11 Technology schematic

Table 5 Comparison of delay, power and device utilization of MIPS RISC processor

Utilization report	MIPS RISC Processor without reversible logic	MIPS RISC Processor With reversible logic
Delay(ns)	0.905	1.99
Number of slice LUTs	15	9
Number of bonded IOBs	85	15
Power(W)	0.084	0.042

VI. CONCLUSION

The use of VHDL for modeling is especially appealing since it provides a formal description of the system and allows the use of specific description styles to cover the different abstraction levels (architectural, register transfer and logic level). The reversible MIPS RISC Processor is proposed because of its area, less complexity, less power as well as faster speed. In particular, the MIPS RISC processor uses reduced instruction set hence results to minimize human effort and reversible logic for low power designs.

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