# Study of MOSFET and Bipolar Junction Transistor with Floating Admittance Matrix 

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#### Abstract

This paper has been devoted to the study of MOSFET and Bipolar Junction Transistor (BJT) with Floating Admittance Matrix (FAM). In this paper we have studied development of Floating Admittance Matrix (FAM) for MOSFET and Bipolar Junction Transistor (BJT). We have represented as four terminals or two port network if any one of the terminals of these devices is made common to both input and output sides in any of its configuration. The mathematical modeling through FAM approaches MOSFET and BJT. Also we have derived the equations for the input resistance, output resistance, current gain, voltage gain of any circuit which shows that one can analyze and design the circuits using first and second order cofactors of the floating admittance matrix (FAM) of the concerned circuit. The entire properties of that circuit can be obtained in the form of cofactors of the floating admittance matrix (FAM).


Keywords : MOSFET, Bipolar Junction Transistor, Floating Admittance Matrix, Input and Output.

## I. INTRODUCTION

Many researchers are introduced and obtained some important results using Floating Admittance Matrix (FAM) ([1]-[5], [8] and [9]). The $n$-port network can easily be described by the floating admittance matrix (FAM). The floating admittance matrix can be obtained from the definite admittance matrix in which at least one terminal is connected to ground. The ground or reference point of the network under consideration falls outside the preview of the network. For the purpose, we shall consider all the independent current sources are outside the network and all initial conditions are set to zero. ([1]-[5])


Fig. 1: $n$-terminal network

The $n$-terminal currents in Fig. 1 can be expressed as:
(1.0) $\quad i_{i}=y_{i j} v_{n}+I_{o i}$

Where in the subscript ' $i j$ ' of $y_{i j}, i$ indicates the row value and $j$ indicates the column value from 1 to $n$, $v_{n}$ are the potentials connected between terminals and $i_{i}$ are currents entering terminals from outside the network with initial conditions $I_{o i}$.
The linear equation (1.0) can be written in the following matrix form
(1.1) $\left[\begin{array}{c}i_{1} \\ i_{2} \\ \vdots \\ i_{n}\end{array}\right]=\left[\begin{array}{cccc}y_{11} & y_{12} & \cdots & y_{1 n} \\ y_{21} & y_{22} & \cdots & y_{2 n} \\ \vdots & \vdots & \cdots & \vdots \\ y_{n 1} & y_{n 2} & \cdots & y_{n n}\end{array}\right]\left[\begin{array}{c}v_{1} \\ v_{2} \\ \vdots \\ v_{n n}\end{array}\right]+\left[\begin{array}{c}I_{o 1} \\ I_{o 2} \\ \vdots \\ I_{o n}\end{array}\right]$

Here the coefficient matrix $y_{i j}$ relating voltages $v_{1}, v_{2}, \ldots \ldots \ldots . v_{n}$, and currents $i_{1}, i_{2}, \ldots \ldots \ldots . . i_{n}$ in equation (1.1) is separated as;

$$
\left[\begin{array}{cccc}
y_{11} & y_{12} & . & y_{1 n}  \tag{1.2}\\
y_{21} & y_{22} & . & y_{2 n} \\
\vdots & \vdots & : & \vdots \\
y_{n 1} & y_{n 2} & \cdots & y_{n n}
\end{array}\right]
$$

This coefficient matrix is also called the floating admittance matrix of any $n$-terminal network, 1.e., coefficient matrix $\left[y_{i j}\right]$ is called the floating admittance matrix (FAM).

The Floating Admittance Matrix of the active devices such as BJTs, MOSFETs, vacuum tubes extensive use in the design and analysis of complicated circuits.([1]-[6]) First we will take up amplifier circuits using MOSFET devices and then using the BJT. Since each of these active devices has three terminals, Here, three terminals current and voltage are denoted by: Base current $i_{b}$ and base voltage $v_{b}$ of the BJT, Gate current $i_{g}$ and Gate voltage $v_{g}$ of the MOSFET, Gate current $i_{G}$ and Gate voltage $v_{G}$ of the vacuum tube, Collector current $i_{c}$ and Collector voltage $v_{c}$ of the BJT, Drain current $i_{d}$ and Drain voltage $v_{d}$ of the MOSFET, Plate current $i_{p}$ and Plate voltage $v_{p}$ of the vacuum tube, Emitter current $i_{e}$ and Emitter voltage $v_{e}$ of the BJT, Source current $i_{s}$ and Source voltage $v_{s}$ of the MOSFET, Cathode current $i_{k}$ and Cathode voltage $v_{k}$ of the vacuum tube. It is also represented as 4 -terminal or two port network by making one of the configurations. Two port symbolic representations of 3-terminal devices are shown in Fig.2. These devices can be represented as two port network if any one of the terminals is referred to common on both input and output sides of the network as shown in Fig. 3, 4, and 5.


Fig. 2: Symbolic Representation of BJT, MOSFET and Triode


Fig.3: Generalized 2- port Network


Fig. 4: BJT as 2-port Network


Fig. 5: MOSFET as 2-port Network
Here numeric value $\mathrm{b}=1$ for base, $\mathrm{c}=2$ for collector, $\mathrm{e}=3$ for emitter, $\mathrm{g}=1$ for Gate, $\mathrm{d}=2$ for drain, $\mathrm{s}=3$ for source, $\mathrm{G}=1$ for grid, $\mathrm{p}=2$ for Plate, and $\mathrm{K}=3$ for cathode. These numeric values assigned for generalized description and analysis of floating admittance matrix of these devices.
The three terminals current and voltage of these devices can be written as:

$$
\left[\begin{array}{l}
i_{1}=i_{b} / i_{g} / i_{G}  \tag{1.3}\\
i_{2}=i_{c} / i_{d} / i_{p} \\
i_{3}=i_{e} / i_{s} / i_{k}
\end{array}\right]=\left[\begin{array}{lll}
y_{11} & y_{12} & y_{13} \\
y_{21} & y_{22} & y_{23} \\
y_{31} & y_{32} & y_{33}
\end{array}\right]\left[\begin{array}{l}
v_{1}=v_{b} / v_{g} / v_{G} \\
v_{2}=v_{c} / v_{d} / v_{p} \\
v_{3}=v_{e} / v_{s} / v_{k}
\end{array}\right]
$$

Equation (1.3) in Common Emitter or Common Source can be written as,

$$
\left[\begin{array}{l}
i_{1}=i_{b} / i_{g} / i_{G}  \tag{1.4}\\
i_{2}=i_{c} / i_{d} / i_{p}
\end{array}\right]=\left[\begin{array}{ll}
y_{11} & y_{12} \\
y_{21} & y_{22}
\end{array}\right]\left[\begin{array}{l}
v_{1}=v_{b} / v_{g} / v_{G} \\
v_{2}=v_{c} / v_{d} / v_{p}
\end{array}\right]
$$

The equation (1.3) in Common Collector or Common Drain configuration can be written as,

$$
\left[\begin{array}{l}
i_{1}=i_{b} / i_{g} / i_{G}  \tag{1.5}\\
i_{3}=i_{e} / i_{s} / i_{k}
\end{array}\right]=\left[\begin{array}{ll}
y_{11} & y_{13} \\
y_{31} & y_{33}
\end{array}\right]\left[\begin{array}{l}
v_{1}=v_{b} / v_{g} / v_{G} \\
v_{3}=v_{e} / v_{s} / v_{k}
\end{array}\right]
$$

Also the equation (1.3) in Common Base or Common Gate configuration can be written as,

$$
\left[\begin{array}{l}
i_{2}=i_{c} / i_{d} / i_{p}  \tag{1.6}\\
i_{3}=i_{e} / i_{s} / i_{k}
\end{array}\right]=\left[\begin{array}{ll}
y_{22} & y_{23} \\
y_{32} & y_{33}
\end{array}\right]\left[\begin{array}{l}
v_{2}=v_{c} / v_{d} / v_{p} \\
v_{3}=v_{e} / v_{s} / v_{k}
\end{array}\right]
$$

Now, the first order cofactor denoted by the symbol $y_{i j}$ of the matrix [y] where $y_{i j}$ denotes the submatrix obtained from a floating admittance matrix [y]. ([1]-[6])
(1.7) $y_{i j}=(-1)^{i+j}$ determinant of the matrix [y].

A square matrix is said to be an equicofactor matrix if the sum of the elements of every row or every column equal zero. If $y$ is an equicofactor matrix then all of its first order cofactors are equal. If $y_{m n}$ and $Y_{i j}$ are 2- cofactors of the matrix [y], then

$$
\text { (1.8) } y_{m n}=y_{i j}
$$

If the sub-matrix $y_{r p, s q}$ is obtained from the matrix [y] by deleting two row $r$ and $s$ and two columns $p$ and $q$, then get second order cofactor results [6]. The second order cofactor is denoted by $y_{r p, s q}$ of the element $y_{r p}$ and $y_{s q}$ of the matrix [y] and the scalar quantity defined by the relationship after prefixing the sign, i.e.,

$$
\begin{equation*}
y_{r p, s q}=\operatorname{sgn}(r-s) \operatorname{sgn}(p-q)(-1)^{r+s+p+q} \operatorname{det} y_{r p, s q}, \tag{1.9}
\end{equation*}
$$

where $r \neq s, p \neq q$ and
$\operatorname{sgn}(x)=1, \quad$ if $x>0, \operatorname{sgn}(x)=0, \quad$ if $x=0, \operatorname{sgn}(x)=-1$, if $x<0$,
and if $r=s$ and $p=q$ then $y_{r p, s q}=0$.
Now after these observations in order that MOSFET and BJT using FAM, we have define following definitions and obtained some results.

## II. COMMON SOURCE AMPLIFIER

The common source amplifier is similar to the common emitter amplifier of the BJT. A simple circuit of the common source amplifier is shown in Fig. 6, where coupling and bypass capacitors have been added along with the signal source and load resistors. These coupling and bypass capacitors do not behave as short circuits at low frequencies. The coupling capacitors $C_{1}$ and $C_{2}$ provide the function of isolating the amplifier DC from the signal source and the load ([1]-[7]). The bypass capacitor provides the low impedance path for the AC signal so that presence of source resistor $R_{S}$ does not reduce gain of the amplifier.


Fig. 6: Common Source Amplifier
The small signal analysis of the amplifier, the coupling and bypass capacitors are replaced by short circuits. The DC power supplies ( $V_{G G}$ and $V_{D D}$ ) are also replaced by the short circuit. After these replacements, the circuit is called AC circuit as shown in Fig. 7.


Fig. 7: AC Circuit of CS Amplifier
The floating admittance matrix (FAM) connected components (resistances $r_{s}=1 / g_{s}, R_{G}=1 / G_{G}, R_{D}=$ $1 / G_{D}$, and $R_{L}=1 / G_{L}$ ) in the circuit of Fig. 7 can be written as, ([8]-[9])

$$
\left[\begin{array}{ccc}
g_{s}+G_{G} & 0 & -g_{s}-G_{G}  \tag{2.1}\\
0 & G_{D}+G_{L} & -G_{D}-G_{L} \\
-g_{s}-G_{G} & -G_{D}-G_{L} & g_{s}+G_{D}+G_{G}+G_{L}
\end{array}\right] .
$$

The floating admittance matrix including active and passive components together for Fig. 8 can be written as,
(2.2) $\left[\begin{array}{ccc}g_{s}+g_{s}+G_{G} & 0 & -g_{g}-g_{s}-G_{G} \\ g_{m} & g_{d}+G_{D}+G_{L} & -g_{m}-g_{d}-G_{D}-G_{L} \\ -g_{g}-g_{m}-g_{s}-G_{G} & -g_{d}-G_{D}-G_{L} & g_{g}+g_{m}+g_{d}+G_{D}+G_{G}+G_{L}\end{array}\right]$

The voltage gain between terminals 2 and 3, 1 and 3 in Fig.7. The input impedance or input resistance between terminals $1 \& 3$ in Fig 7 is expressed as,

$$
\begin{equation*}
\left.A_{v}\right|_{13} ^{23}=\operatorname{sgn}(2-3) \operatorname{sgn}(1-3)(-1)^{9}\left|\frac{y_{23}^{13}}{y_{13}^{13}}\right|=-\left|\frac{\mid \sum_{23}^{13}}{y_{13}^{13}}\right|, \tag{2.3}
\end{equation*}
$$

where $\left|y_{13}^{13}\right|=g_{d}+G_{D}+G_{L}$ and $\left|y_{23}^{13}\right|=g_{m}$,
therefore, the equation (2.3) can be written as, ([1]-[5] \& [8])

$$
\text { (2.4) }\left.A_{v}\right|_{13} ^{23}=-\frac{g_{m}}{g_{d}+G_{D}+G_{L}}=-g_{m}\left(r_{d}\left\|R_{D}\right\| R_{L}\right) \text {. }
$$

when $r_{d} \gg R_{D}, R_{L}$, then the equation (2.4) gives ([8]-[9])

$$
\text { (2.5) }\left.A_{v}\right|_{13} ^{23}=--g_{m}\left(R_{D} \| R_{L}\right) .
$$

The input impedance or input resistance between terminals 1 and 3 in Fig. 7 is expressed as,

$$
\text { (2.6) } Z_{i}=Z_{13}=\operatorname{sgn}(1-3) \operatorname{sgn}(1-3)(-1)^{8}\left|\frac{y_{13}^{13}}{y_{3}^{3}}\right|=\left|\frac{\mid 13}{y_{3}^{3}}\right| \text { as } g_{s}=0 \text {, }
$$

where, $\left|y_{13}^{13}\right|=g_{d}+G_{D}+G_{L}$ and $\left|y_{3}^{3}\right|=\left(g_{g}+G_{G}\right)\left(g_{d}+G_{D}+G_{L}\right) \quad$ as $g_{s}=0$,
therefore, the equation (2.3) can be written as,

$$
\text { (2.7) } Z_{i}=Z_{13}=\frac{1}{\left(g_{g}+G_{G}\right)},
$$

when $r_{g} \gg R_{G}$, then the equation (2.7) gives ([1]-[5] \& [8])

$$
\text { (2.8) } z_{i}=Z_{13}=-r_{g} \| R_{G} \cong R_{G} \text {. }
$$

Now, the input resistance $R_{G}$ is connected across the external input voltage source as in Fig.8.


Fig. 8: $\boldsymbol{Z}_{\boldsymbol{i}}=\boldsymbol{Z}_{\mathbf{1 3}}$
From Fig. 8, the effect of source resistance on the overall voltage gain can be estimated as, [8]

$$
\text { (2.9) } \frac{v_{13}}{v_{s}}=\frac{z_{i}}{z_{i}+r_{s}}=\frac{r_{g} \| R_{G}}{r_{g} \| R_{G}}=1
$$

Hence, the overall voltage gain of the amplifier including the source resistance is not affected by the source resistance $r_{s}$ and is written as, ([1]-[5])

$$
\text { (2.10) } A_{v s}=-g_{m}\left(R_{D} \| R_{L}\right) .
$$

The output impedance or output resistance between terminals $2 \& 3$ of Fig 7 is written as,

$$
\text { (2.11) } Z_{o}=Z_{23}=\operatorname{sgn}(2-3) \operatorname{sgn}(2-3)(-1)^{10}\left|\frac{y_{23}^{23}}{y_{3}^{3}}\right|=\left|\frac{y_{23}^{23}}{y_{3}^{3}}\right| \text { as } G_{L}=0 \text {, }
$$

where, $\left|y_{23}^{23}\right|=g_{g}+g_{s}+G_{G}$ and $\left|y_{3}^{3}\right|=\left(g_{d}+G_{D}\right)\left(g_{g}+g_{s}+G_{G}\right) \quad$ as $G_{L}=0$,
therefore, the equation (2.11) can be written as, ([1]-[5] \& [8])
(2.12) $Z_{0}=Z_{23}=\frac{1}{\left(g_{d}+G_{D}\right)}=r_{D} \| R_{D}$

## III. COMMON DRAIN AMPLIFIER

The common drain amplifier is more popularly known as source follower. It is similar to the emitter follower amplifier circuit of the BJT. The AC circuit of the common drain amplifier shown in Fig.9. The negative feedback available across $R_{S}$ is sent to the input side from the output loop. ([1]-[7])


Fig. 9: Source Follower Circuit


Fig. 10: Circuit of Source Follower
The floating admittance matrix (FAM) connected components of the circuit in Fig. 10 can be written as, ([1]-[5])

$$
\left[\begin{array}{ccc}
g_{g}+g_{s}+G_{G} & -g_{s}-G_{G} & -g_{g}  \tag{3.1}\\
g_{m}-g_{s}-G_{G} & g_{d}+g_{s}+G_{G}+G_{S}+G_{L} & -g_{m}-g_{d}-G_{S}-G_{L} \\
-g_{g}-g_{m} & -g_{d}-G_{S}-G_{L} & g_{g}+g_{m}+g_{d}+G_{D}+G_{S}+G_{L}
\end{array}\right]
$$

The voltage gain between terminals 3 and 2, 1 and 2 in Fig. 10 and can be written as,
(3.2) $\left.A_{v}\right|_{12} ^{32}=\operatorname{sgn}(3-2) \operatorname{sgn}(1-2)(-1)^{8} \left\lvert\, \begin{aligned} & \frac{y_{32}^{12}}{y_{12}^{12}}\left|=-\left|\frac{y_{32}^{12}}{y_{12}^{12}}\right|, ~\right.\end{aligned}\right.$,
where, $\left|y_{32}^{12}\right|=-g_{g}-g_{m}$ and $\left|y_{12}^{12}\right|=g_{g}+g_{m}+g_{d}+G_{D}+G_{S}+G_{L}$,
therefore, the equation (3.2) can be written as, ([1]-[5])

$$
\text { (3.3) }\left.A_{v}\right|_{13} ^{23}=-\frac{-g_{g}-g_{m}}{g_{g}+g_{m}+g_{d}+G_{D}+G_{S}+G_{L}} \cong g_{m}\left(R_{L} \| R_{S}\right) \text {. }
$$

The input impedance or input resistance between terminals 1 and 2 in Fig. 10 is written as,
(3.4) $Z_{i}=Z_{12}=\operatorname{sgn}(1-2) \operatorname{sgn}(1-2)(-1)^{6}\left|\frac{y_{12}^{12}}{y_{2}^{2}}\right|=\left|\frac{y_{12}^{12}}{y_{2}^{2}}\right|$ as $g_{s}=0$,
where, $\left|y_{12}^{12}\right|=g_{g}+g_{m}+g_{d}+G_{S}+G_{L}$ and $\left|y_{2}^{2}\right|=G_{G}\left(g_{g}+g_{m}+g_{d}+G_{S}+G_{L}\right)$ as $g_{s}=0$, therefore, the equation (3.4) can be written as, ([1]-[5] )

$$
\text { (3.5) } z_{i}=Z_{12}=\frac{1}{G_{G}} \cong R_{G} \text {, }
$$

Now, the input resistance $R_{G}$ is connected across the external input voltage source as in Fig.11.


Fig. 11: $\boldsymbol{Z}_{\boldsymbol{i}}=\boldsymbol{Z}_{12}$
From Fig. 11, the effect of source resistance on the overall voltage gain can be estimated as, [8]

$$
\text { (3.6) } \frac{v_{12}}{v_{s}}=\frac{z_{i}}{z_{i}+r_{s}}=\frac{R_{G}}{R_{G}}=1
$$

Hence,
(3.7) $A_{v s}=g_{m}\left(R_{L} \| R_{S}\right)$.

The output impedance between terminals $3 \& 2$ of Fig 10 is written as, ([1]-[5])

$$
\text { (3.8) } Z_{o}=Z_{32}=\operatorname{sign}(3-2) \operatorname{sign}(3-2)(-1)^{10}\left|\frac{3_{2}^{32}}{y_{2}^{2}}\right|=\left|\frac{y_{32}^{32}}{y_{2}^{2}}\right| \text { as } G_{L}=0 \text {, }
$$

where, $\left|y_{32}^{32}\right|=g_{s}+G_{G}$ and $\left|y_{2}^{2}\right|=\left(g_{s}+G_{G}\right)\left(g_{m}+g_{d}+G_{s}\right)$ as $G_{L}=0$,
therefore, the equation (2.11) can be written as, ([8]-[9])
(3.9) $Z_{0}=Z_{32}=\frac{1}{\left(g_{m}+g_{d}+G_{s}\right)}$

## IV. COMMON GATE AMPLIFIER

The common gate amplifier shown in Fig. 12 is commonly used at high frequencies as its gate source capacitance. The simplest AC circuit of the common gate amplifier is drawn in Fig. 13. ([1]-[7])


Fig. 12 Common Gate Amplifier


Fig.13: AC Circuit of Common Gate Amplifier
The composite floating admittance matrix for the circuit of Fig. 13 including the active and passive components by inspection is written as, ([1]-[5])
(4.1) $\left[\begin{array}{ccc}g_{g}+g_{s}+G_{G}+G_{G} & -G_{D}-G_{L} & -g_{g}-g_{s} \\ g_{m}-G_{D}-G_{L} & g_{d}+G_{D}+G_{L} & -g_{m}-g_{d} \\ -g_{g}-g_{m}-g_{s} & -g_{d} & g_{g}+g_{m}+g_{d}+g_{s}\end{array}\right]$

The voltage gain between terminals 2 and 1, 3 and 1 in Fig. 13 and can be written as,
(4.2) $\left.A_{v}\right|_{31} ^{21}=\operatorname{sgn}(2-1) \operatorname{sgn}(3-1)(-1)^{7}\left|\frac{y_{21}^{31}}{y_{31}^{31}}\right|=-\left|\frac{y_{21}^{31}}{y_{31}^{31}}\right|$,
where, $\left|y_{21}^{31}\right|=-g_{m}-g_{d}$ and $\left|y_{31}^{31}\right|=g_{d}+G_{D}+G_{L}$,
therefore, the equation (3.2) can be written as, ([1]-[5])

$$
\text { (4.3) }\left.A_{\nu}\right|_{13} ^{23}=-\frac{-g_{m}-g_{d}}{g_{d}+G_{D}+G_{L}} \cong g_{m}\left(R_{L} \| R_{D}\right) \text {. }
$$

The input impedance or input resistance between terminals 3 and 1 in Fig. 13 is written as,
(4.4) $Z_{i}=Z_{31}=\operatorname{sgn}(3-1) \operatorname{sgn}(3-1)(-1)^{8}\left|\frac{y_{31}^{31}}{y_{1}^{1}}\right|=\left|\frac{y_{31}^{31}}{y_{1}^{1}}\right| \quad$ as $g_{s}=0$,
where, $\left|y_{31}^{31}\right|=g_{d}+G_{D}+G_{L}$ and $\left|y_{1}^{1}\right|=\left(G_{G}+G_{L}\right)\left(g_{g}+g_{m}+g_{d}\right)+g_{g} g_{d} \quad$ as $g_{s}=0$,
therefore, the equation (3.4) can be written as, ([1]-[5])

$$
\text { (4.5) } Z_{i}=Z_{31}=\frac{g_{d}+G_{D}+G_{L}}{\left(G_{G}+G_{L}\right)\left(g_{g}+g_{m}+g_{d}\right)+g_{g} g_{d}} \text {. }
$$

Now, the input resistance (4.5) is connected across the external input voltage source as in Fig.14.


Fig. 14: $\boldsymbol{Z}_{\boldsymbol{i}}=\boldsymbol{Z}_{\mathbf{3 1}}$
From Fig. 14, the effect of source resistance on the overall voltage gain can be estimated as, [8]

$$
\text { (4.6) } \frac{v_{31}}{v_{s}}=\frac{Z_{i}}{Z_{i}+r_{s}} \text {, }
$$

Hence,

$$
\text { (4.7) } A_{v s} \cong g_{m}\left(R_{L} \| R_{D}\right)
$$

The output impedance between terminals $2 \& 1$ of Fig 13 is written as, ([8]-[9])

$$
\begin{equation*}
Z_{o}=Z_{21}=\operatorname{sgn}(2-1) \operatorname{sgn}(2-1)(-1)^{6}\left|\frac{y_{21}^{21}}{y_{1}^{1}}\right|=\left|\frac{\mid 2_{21}^{21}}{y_{1}^{1}}\right| \quad \text { as } G_{L}=0, \tag{4.8}
\end{equation*}
$$

where, $\left|y_{21}^{21}\right|=\left(g_{g}+g_{m}+g_{d}+g_{S}\right)$ and $\left|y_{1}^{1}\right|=\left(g_{g}+g_{m}+g_{d}+g_{S}\right)+g_{d}\left(g_{g}+G_{S}\right)$ as $G_{L}=0$,
therefore, the equation (4.8) can be written as, ([8]-[9])

$$
\begin{equation*}
Z_{0}=Z_{21}=\frac{\left(g_{g}+g_{m}+g_{d}+g_{s}\right)}{\left(g_{g}+g_{m}+g_{d}+g_{s}\right)+g_{d}\left(g_{g}+G_{s}\right)} \cong R_{D} . \tag{4.9}
\end{equation*}
$$

## V. CONCLUSION

This paper has been divided into four sections of which the first section is introductory. In this section we have studied the significance and properties of the floating admittance matrix (FAM) and also obtained the network functions thorough ratios of first order and second order cofactors of the floating admittance matrix (FAM). The n-port network can easily be described by the floating admittance matrix (FAM). We obtained floating admittance matrix from the definite admittance matrix in which at least one terminal is connected to ground. The ground or reference point of the network under consideration falls outside the preview of the network. For the purpose, we shall consider all the independent current sources are outside the network and all initial conditions are set to zero. In the second, third and fourth sections studied the mathematical modeling through FAM approaches MOSFET and BJT. Also we have derived the equations for the input resistance, output resistance, current gain, voltage gain of any circuit which shows that one can analyze and design the circuits using first and second order cofactors of the floating admittance matrix (FAM) of the concerned circuit. The entire properties of that circuit can be obtained in the form of cofactors of the floating admittance matrix (FAM).

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