International Journal of Scientific Research in Science and Technology
Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)
doi : https://doi.org/10.32628/IJSRST218658

Low-Power Low-Area architecture of Probability Density Function Estimation for Histogram Equalization

Koteswar Rao Bonagiri*[1], Giri Babu Kande[2], P. Chandrasekhar Reddy[3]
*[1]Research scholar, Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University, Hyderabad, India
[1]Assistant Proffesor, Marrilaxman Reddy institute of Technology and Management, Hyderabad, India,
[2]Professor, Department of Electronics and Communication Engineering, Vasireddy Venkatadri Institute of Technology, Andhra Pradesh, India
[3]Professor, Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University, Hyderabad, India

Article Info
Volume 8, Issue 6
Page Number : 418-427

Publication Issue
November-December-2021

Article History
Accepted : 10 Dec 2021
Published : 18 Dec 2021

ABSTRACT

Estimation of Probability Density Functions (PDFs) in view of accessible information is critical issue emerging in various fields, for example, broadcast communications, machine learning, information mining, design pattern recognition and Personal Computer (PC) vision. In this paper, the Look-Up Table–Carry Select Adder-PDF (LUT-CSLA-PDF) mehod is implemented to increase system performance. The LUT is one of the fast way to recognize a complex function in the digital logic circuit. In this work, The FPGA (field programmable gate array) analysis, LUT, slices, flip flops, frequency are improved as well as ASIC (application specified integrated chip) implementation analysis an area, power, delay, Area Power Product (APP), Area Delay Product (ADP) are enhanced in LUT-CSLA-PDF technique compared to conventional methods.

Keywords : Probability density function, Look-Up Table, Carry Select Adder, Field Programmable Gate Array and Application Specified Integrated Chip.

I. INTRODUCTION

The PDF is a basic concept in the statistic processes. A statistical measure of data can be categorized into two types such as 1. An understanding features and shape of data over the density function. 2. An estimation of one function over the joint density function. The PDFs estimation is building of predict density function from observed data points, which is based on obtainable data that is an important issue arising in different fields like telecommunications, data mining, machine learning, computer version, pattern recognition and so on [1].

The PDFs estimation of a random variable can be estimated by employing different techniques like Parametric, Non- parametric or Semi- parametric techniques. The parametric techniques are utilized to fit the data to an identified model and reduce the value of parameters. This parameter employed to

statistics from the model's equations. But this technique experimental result is very poor accuracy. The Semi- parametric techniques are used for all kinds of density functions, which gives the high accurate outcomes within low data [2]. The Non-parametric techniques are classified into two methods such as Histogram and Kernel methods. The density function can be estimated by using a histogram of the sample data that requires several numbers of samples for a smooth curve. This PDF method can provide a smoother curve from few data samples [3].

The PDF is an important tool in the statistics processes because its used for measuring signal performance and Bit Error Rate (BER) of the signal processing systems [4]. An efficient algorithm for approximating results to given continuous PDF by a deterministic Dirac Mixture Density (DMD). This density function is employed to various operations such as system identification, state estimation, data fusion, and control system [5]. In commonly, most of the Stochastic Control Design (SCD) techniques focused on control of the O/P mean and variance of Stochastic System. There are 2-types of PDF control strategies have been used for stochastic systems. The first type of Stochastic Systems has created turning to the PDF control function that is general and practical in the Joint PDF (JPDF) shape control. The second type of stochastic systems strategies is related to the JPDFs are immeasurable. The JPDFs of the outcomes were formulated recursively by using system function. But its accuracy of the closed –loop control is more difficult to be assured for the stochastic system below the modeling errors [6] [7]. The Non- parametric algorithms are estimated the PDF from a wider function set. This algorithm is an including two main methods like Parzen and Support Vector Machine (SVM) based algorithm. The Parzen algorithm is commonly for data fields to knowledge. If your paper does not represent original work, it should have educational value by presenting a fresh perspective or a synthesis of existing knowledge. The purpose of this document is to provide you with some guidelines. You are, however, encouraged to consult additional resources that assist you in writing a professional technical paper.

The estimated function can include all the training vectors, but it will be not practical whenever the number of training vector is very large. The SVM algorithm can be selected the vectors having more involvement to the PDF is called as Support Vector (SV). Hence, the estimation results are only related to the SV technique. The SVM algorithm is low complexity compared to the Parzen algorithm [8]. The PDFs are offered for the asymmetric non-Gaussian distribution of the drain current. This distribution, the drain current at the non-Gaussian high – sigma tail can be predicted by median and variance removed from statistical information of a small group of samples, this method is not suitable for a large arrangement of samples [9]. Parametric Maximum Likelihood (PML) estimators are employed for the PDFs because it is an efficient computing process in various static fields such as fast convergence rate, asymptotic normality and so on. But these estimators are not given appropriate results in the statistics processes [10]. To conquer this problem, "LUT-CSLA-PDF-IHEQ" method is implemented to evaluate the estimation in the PDF histogram. After performing PDF estimation, image histogram equalization is applied in "LUT-CSLA-PDF-IHEQ", which gives the resulting parameters like Peak Signal-to- Noise Ratio (PSNR), image contrast, entropy, Absolute Mean Brightness Error (AMBE) and time computation. Finally, the area, power, delay, ADP, and APP is minimized in "LUT-CSLA-PDF" technique than the conventional method. On FPGA analysis, LUT, slices, flip flops, and frequency is enhanced in "LUT-CSLA-PDF-IHEQ" method compared to existing method.

This paper is composed as follows. In section II, described some previous related work. In Section III,

shows LUT-CSLA-PDF design architecture. In Section IV, mentioned experimental setup and results and discussion. The conclusion is made in Section V.

II. RELATED WORK

Weilong Ren et.al [11] have proposed an asymmetrical PDF for modeling Log-Ratio SAR image. The PDF of the log- ratio Synthetic Aperture Rader (SAR) image is highly suited. In this paper, introduced the analytic distribution form of the log – ratio image. The SAR image commonly modeled as Gamma distributed but it is not specific distribution form of the log-ratio SAR image.

Liu et.al [13] have addressed the sliding-mode control design for non-linear systems utilizing PDF shaping. In this work, a sliding mode based on Stochastic Distribution Control (SDC) algorithm used for the nonlinear system. Where the sliding mode controller is intended to stabilize the stochastic device and SDC tries to the shape sliding surface as close as feasible to the PDFs. But this algorithm was more computational complexity.

Cui et.al [14] have presented an exact distribution for the product of two correlated in Gaussian Random Variables (GRVs) method such as non-zero means and variances, which is mostly used in Radar and Communication systems. Hence, the derived PDF convergence fast and finite summations of terms can lead to more accurate approximations. This algorithm only suited for finite number samples, not matched for large number samples.

Berisha et .al [15] have proposed nonparametric density estimation of the First Information Matrix (FIM) is a basic concept in statistical signal processing. That can be utilized to benchmark the performance of an estimator (Cramer Rao Lower Bound (CRLB). In this paper, to estimate the PDF is required for the FIM technique. The several numbers of PDF practical solutions of the statics data is not known but the statistic has access to an observation sample used for each parameter value.

This all-related works contains several problems like more area, power consumption is high, high critical path, more hardware and FPGA utilization. To solve these issues, the LUT-CSLA-PDF method is implemented to increase the ASIC and FPGA implementation results.

III. LUT-CSLA-PDF-HIEQ METHODOLOGY

In the PDF architecture, receives sampled data at its I/P and computes the cumulative histogram of data, which are stored internally. By normalizing, based on the window size that can be changed to any power of 2, the resultant data contained in the circuit denotes the Cumulative Density Function (CDF). This allows to extract different PDF statistics in a highly efficient method. Maintaining the entire histogram within the architecture has the advantage of allowing the designer to extract several statistics of interest, as needed for a specific application. The first half of the circuit evaluates the histogram, which is completed by instantiating a bank of counters that keep a count of the number of occurrences for each and every I/P values. The histogram unit is constracted which updated as each new sample enters the system. The histogram design is intensely pipelined to allow for maximum performance. The second half of the circuit contains of the measurable (statistical) units that extract data of interest from the cumulative histogram utilized for the target application.

A. PDF architecture

- **Computing CDF**
- **Extracting Statics**

Computing CDF

A bank of the counter, one for each bin, which can be arranged when the sample falls is incremented shown in the fig.1. A $p(x = a)$ evaluation would be straight

forwarded, by looking up the count value at index a. The system count is more complex when require for separate computation that takes several cycles. More statistics can be gained by employing the CDF. A group of the CDF data is simply an accumulation of the PDF values at every bin. Thus index a, the count value would be equal to the sum of PDF bin values for all indexes from zero to a. The CDF is a monotonic function. In real time computation would need summation of all the necessary bins, it would be an expensive operation. A single lookup provides the probability for a range of values inside a cumulative histogram. To constrain the range on the two sides would require one or more lookup and the probability would be difference between two. Hence, the CDF is permits for a few interesting statistics to be removed in the real time.

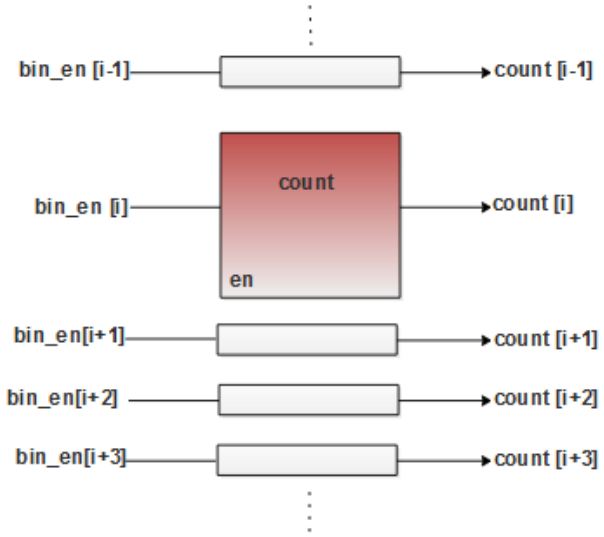

Figure 1. Block diagram of the basic histogram bin stricture

Example for, the $p(x < a)$ is simple bin value at index a. Similarly $p(a < x < b)$ would be the bin value at index b minus the bin value at index$a$. In this paper, an extract centiles—that is the value of c like $p(x < c)$ equals some given value, as will be discussed shortly. In the fig.1 shows block diagram of the basic histogram bin stricture, where each counter's bin_enable I/P indicates wherther or not, it bin should be increased in a given clock cycle. The PDF architecture needs a counter for each histogram bin, and hence the area of this part of the circuit varies linearly with the number of bins. To calculate the cumulative histogram in the real time, the PDF architecture must be cabable to updata all necessary bins used for every I/P sample in one cycle. An I/P sample of the value x should increase the bin corresponding to sample x and total subsequent bins. For PDF architecture with hundreds of bins employing a comparator coupled with each bin to determine this is expensive.

First – in- First- out (FIFO) buffer of the length equal to the window is instantiated, this buffer is keeps track of the samples in the window. The I/P samples are used for FIFO because it differs linearly in length of the window and logarithmically within the number of the bins. In Fig.2 shows the overall architecture of the PDF estimator system, This architecture is including the window FIFO, Access Pattern Memory (APM), bank of the bin counters and statistics units. The input samples enter the system and fed into the FIFO. Hence, the O/P position can be set by the FIFO_length signal, the permitting the window size to be different at the run time. The FIFO is constructed, which can be set to any useful power of 2. To implement the FIFO by using an embedded block Read Access Memory (RAM), which is decreasing logic usage and developing system performance.

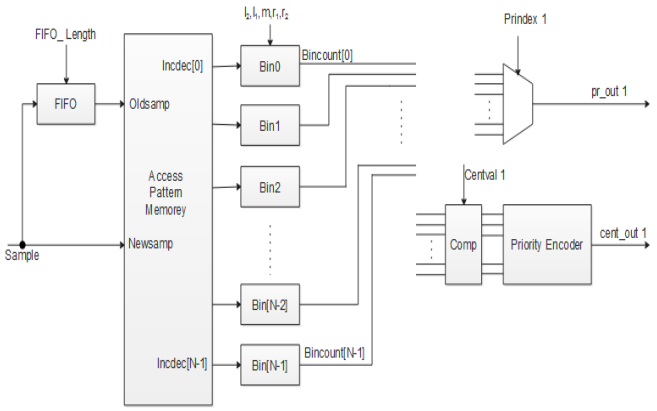

Figure 2. The architecture of the PDF Estimator.

The O/P of the FIFO denotes the old sample developing from the sample window. Furthermore, the new samples are collected, which used to address the two ports of dual port APM. The O/P of this memory expresses of every bin counter to increase, decrease or maintain the existing value and to update the histogram standards. The count O/P of all the bins (Bincount[0: N-1] is passed to the next stage, where statistics can be extracted. Hence, the CDF permits for more interesting statistics to be extracted in the real time system.

Extracting Statics

Example for fixed $p(x < a)$ computations is simply extracted the value in the counter 'a'. If the desired value to be adjustable, the multiplexer is allowed this value to be done. Similarly, for an intermediate probability range, that is use 2-multiplexers to extract the cumulative count for two bins and subtract process. The index signal is set to used I/P and O/P value denotes $p(x < a)$. The $P(X < a)$ is simply subtracted from window size. For the $p(a < x < b)$, two pr_out values, one consistent to each of 'a' and 'b' are subtracted from other.

The priority encoder finds the highest index occurrence of 'one' in a binary word. In centile value, central is given as a proportion of the window size, rather than an original value. The Comp_block compares the total values of all bins in parallel, within required center value and returning a binary one for each bin where the count exceeds the required value. The priority encoder defines the position of the first bin with a high outcome and giving the index for needed centile. The O/Ps can be utilized for monitoring the centiles. The several number of statistical computation elements can be added, as needed. Furthermore, compositions are possible since the histogram data is stored in the bin counters. After implementing PDF, image histogram equalization application will be performed and PSNR, AMBE, entropy, etc will be calculated.

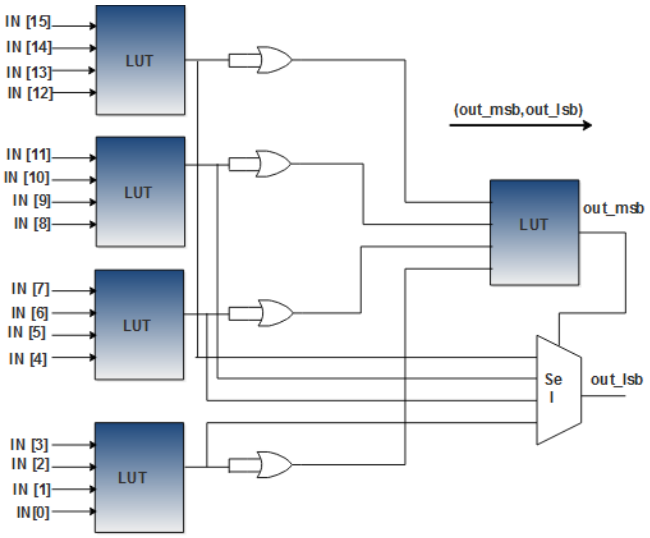

Figure 3. 16-bit priority encoder constructed from five 4-bit priority encoders.

In Fig.3 shows 16-bit priority encoder constructed from five 4-bit priority encoders. The input image can estimate by employing the PDF estimator, which can be evaluated the I/P image in to given particular interval period (p(a<x<b)). After this process, the image can apply in the histogram equalization module. This histogram equalization is employed for equalizing the I/P image range to given particular interval with the same level. This normalization technique is applied to the histogram equalization O/P to scale the pixel range from 1 to 255 for proper display. After performing normalization, the input image is enhanced in terms of contrast level. With the help of PDF- Image histogram equalization method, PSNR value (dB), contrast image (dB), entropy, and AMBE value and image computation are evaluated for O/P enhanced image. For FPGA implementation, Xilinx tool is required to calculate slices, flip flops, frequency, and LUT. Furthermore, to minimize the area, power, and delay by using ASIC implementation in cadence tool an encounter with 180nm and 45nm library technology.

The CSLA design

The CSLA can achieve fast arithmetic operation in various data processing technique. The main aim of

employing this adder is to reduce the area, power dissipation, and delay. The CSLA is operating in many computational structures to cut the carry propagation delay. The elementary knowledge of this work is to use BEC (binary to excess-1 converter) instead of RCA (Ripple Carry Adder) with C_{in}=1. By using fewer numbers of logic gates, BEC logic is derived instead of using n-bit FA (Full adder).

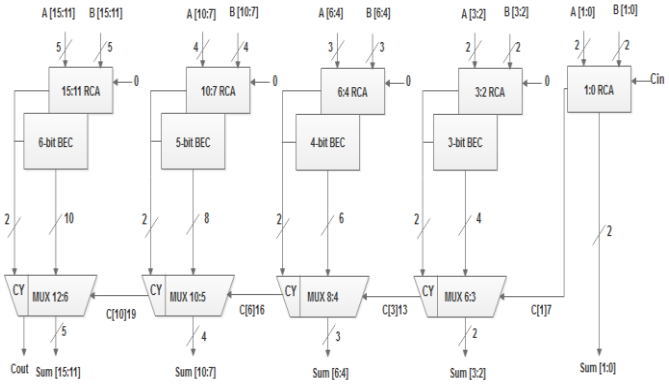

Figure 4. Block diagram of low-area CSLA

The basic idea of this paper is to utilize BEC instead of RCA with in the normal CSLA to achieve low-area and power consumption. The advantage of this BEC logic comes from the lesser number of logic-gates compared to the n-bit FA structure. The group2 has one 2-bit RCA, which has 1 FA and 1 HA for. Instead of another 2-bit RCA with, 3-bit BEC is employed which adds one to the O/P from 2-bit RCA. The input arrival time is lesser than the multiplexer selection input arrival time. Based on the selection line input Cin, this adder gives either BEC O/P or multiplexer O/P. The multiplexer delay and mux selection arrival time derived from the different kind of groups.

IV. RESULT AND DISCUSSION

The LUT-CSLA-PDF design timing diagram was verified in Modelsim by using Verilog code. The RTL schematic was taken from Simplify pro tool. FPGA performance was analyzed for different devices of Virtex-4, Virtex-5 and Virtex-6 by using Xilinx 14.4 ISE tool. In LUT-CSLA-PDF, ASIC implementation of PDF algorithm was verified by using cadence tools in 180nm and 45nm library technology.

ASIC synthesis

This ASIC synthesis is implemented in cadence encounter tool for different technology such as 180nm and 45nm. From this tool, the performance will be calculated such as area, power, and delay.

Area

With shrinking system size ASIC should be able to accommodate maximum functionality in minimum area. The designer will specify area constraint and cadence encounter tool is used to optimize the area performance. Area can be optimized by having lesser number of cells and by replacing multiple cells with single cell that includes both functionalities.

Power

Development of hand-held devices has led to reduction of battery size and hence low power consuming systems. Low power consumption has become a big requirement for lot of designers.

Delay

Designer specifies maximum delay between primary input and primary O/P. This is taken as maximum delay across any critical path.

Table 1. The performance of area, power and delay the proposed method for 180nm and 45nm Technology

Technology	Method	Area (μm^2)	Power (nW)	Delay (ps)	APP (μm^2 * nW)	ADP (μm^2 * ps)
180nm	Existing [7]	342584 3	945983 5	170.7	32407 90951 5905	584 791 400
	LUT-CSL	314545 1	103668 43	170.7	32608 39668 1193	534 726 670

	A-PDF					
45nm	Existing [7]	280210	429621	85.1	1203841004 10	238178 50
	LUT-CSLA-PDF	257276	479552	85.1	1233772203 52	21868460

This table 1 includes the different kind of processing element such as 1 PE and 2 PE. In existing method, normal digital adder is used to perform the PE operation, which occupy more area. In LUT-CSLA-PDF method, carry select adder is used in PE, which required less space to operate the shifting and accumulation. Due to this CSLA adder, the area, power, delay, APP, and ADP is minimized in LUT-CSLA-PDF architecture than conventional PD function. This ASIC results have been taken from cadence software for different library such as 180nm and 45nm technology.

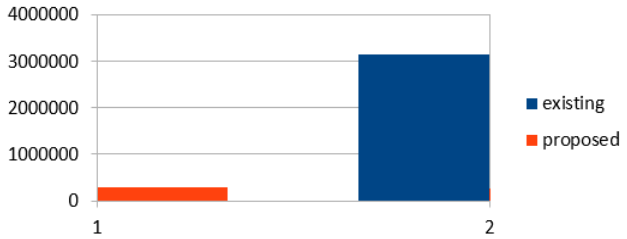

Figure 5 Comparison of AREA performance for existing and LUT-CSLA-PDF

The comparison graph of area, power, area power product and area delay product are shown in Figure 5 respectively. That results are drawn by using different technology like180nm technology and 45nm technology for different kind of PE such as According to that graph, blue line is represented as existing and orange line represents as LUT-CSLA-PDF method. From this graph, it is clearing that LUT-CSLA-PDF method consume less area, less power, less area power product and less area delay product than conventional methods.

Table 2. Reduced percentage of area, power, delay, APP, and ADP for LUT-CSLA-PDF method

Technology	Reduced % of Area	Reduced % of power	Reduced % of APP	Reduced % of ADP
180nm	8.18	-	-	8.56
	8.67	53.37	57.41	8.67
	8.42	53.37	57.41	8.61
45nm	8.18	-	-	8.18
	8.67	62.10	65.39	8.67
	8.42	62.1	65.39	8.42

The reduction percentage of area, power, APP, and ADP for different PE like 1 PE and 2 PE is given in Tab.2. This architecture result has been taken in both 180nm and 45nm technology. In 180nm technology, 8.42 % of area, 53.37% of power, 57.41% of APP, and 8.61% of ADP is minimized in LUT-CSLA-PDF as well as 45nm technology, 8.42 % of area, 62.1 % of power, 65.39 % of APP, and 8.42 % of ADP is reduced in LUT-CSLA-PDF method than conventional method.

FPGA synthesis

This FPGA synthesis is implemented in Xilinx tool for different devices such as Virtex-4, Virtex-5, and Virtex-6. From this tool, the performance will be calculated such as LUT, flip flop, Slices, and Frequency.

LUT

A **LUT**, which stands for **Look Up Table**, in general terms is basically a table that determines what the O/P is for any given input(s). In the context of combinational logic, it is the **truth table.** This truth table effectively defines how your combinatorial logic behaves.

Flip flop

Flip-flops are binary shift registers used to synchronize logic and save logical states between

clock cycles within an FPGA circuit. On every clock edge, a flip-flop latches the 1 or 0 (TRUE or FALSE) value on its input and holds that value constant until the next clock edge.

Slices

Logic resources are resources on the FPGA that can perform logic functions. Logic resources are grouped in slices to create configurable logic blocks. A slice contains a set number of LUTs, flip-flops and multiplexers. A LUT is a collection of logic gates hard-wired on the FPGA.

Frequency

Frequency is defined as the rate at which something occurs over a particular period of time or in a given sample.

Table 3. Implemented on different Xilinx FPGA devices for LUT-CSLA-PDF

Target FPGA	Circuit	LUT	Flip flop	Slice	Frequency (MHz)
Virtex 4 xc4vfx12	Existing [7]	1376/10944	94/10944	737/5472	45.13
	LUT-CSLA-PDF	1177/10944	65/10944	630/5472	47.420

The Table. 3 is the comparison of the different design architecture, which is used to analysing the performance parameters such as LUTs, the number of flip flops, slices, and operating frequency for different FPGA devices such as vertex 4, vertex 5 and vertex 6. From this table, it's clears that the LUT, flip flop, slices are reduced and operating frequency is increased in LUT-CSLA-PDF method than the existing method. Due to the reduction of those parameters, the area has been minimized in filter architecture. This FPGA results have been taken from Xilinx software. In that graph, LUT, Flip flop, slices and Frequency has been analysed for different FPGA devices such as vertex 4, vertex 5 and vertex 6. From this graph, it's clears that all the FPGA performance is improved in LUT-CSLA-PDF design than conventional design.

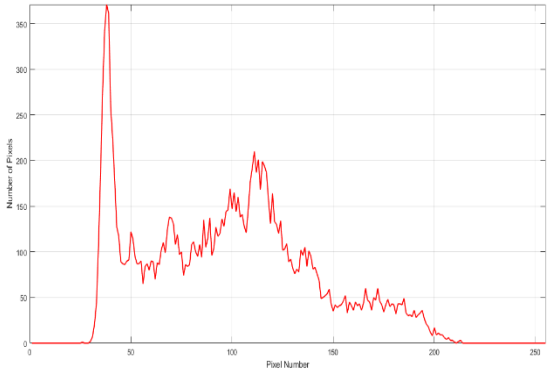

Figure 6 Histogram waveform

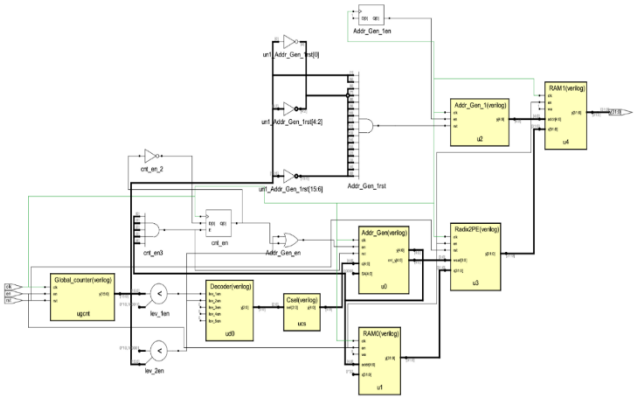

Figure 7 Block diagram for RTL-LUT-CSLA-PDF

The RTL schematic of LUT-CSLA-PDF is shown in figure 7, which is taken from Synplify pro software using Verilog code. This architecture has separate code for each block such as global counter, decoder, C_sel, RAM, address generator, and Radix 2PE. The O/P waveform of the 32-point PDF is shown in figure 8 RAM_U1 is represent as the input for the PDF signal. After performing the PE, the O/P is represented as U4_RAM in terms of from 0 to 31 memory. From this waveform, it's clears that the LUT-CSLA-PDF architecture is working perfectly.

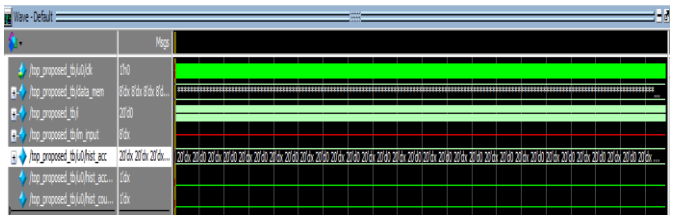

Figure 8 O/P waveform of LUT-CSLA-PDF

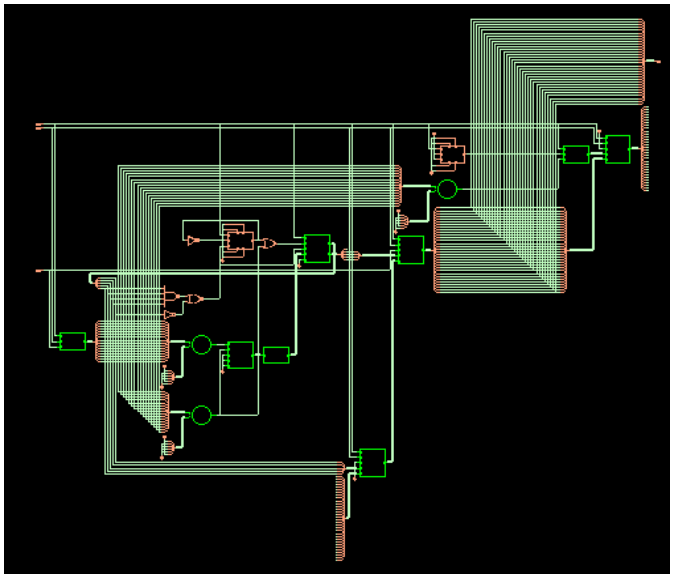

Figure 9. RTL schematic of LUT-CSLA-PDF in 180nm

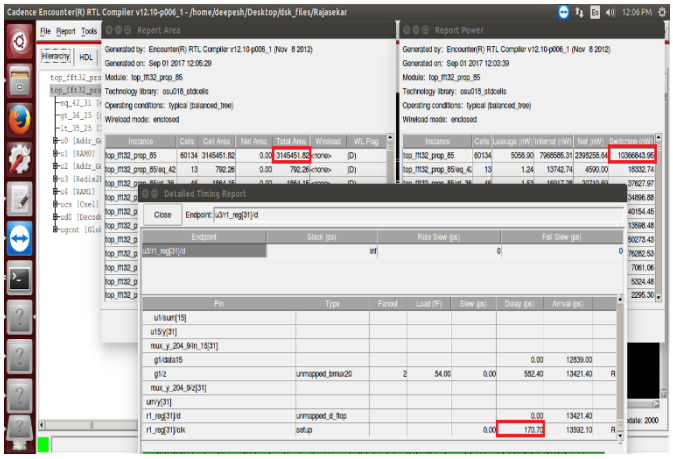

Figure 10 Area, power and delay analysis for LUT-CSLA-PDF in 180nm

The RTL schematic of LUT-CSLA-PDF design is shown in fig.9, which is taken from cadence tool. For ASIC implementation, same code is used for the FPGA implementation. Cadence RTL compiler is used to convert RTL Verilog into Gate level Verilog. Verilog codes are read by using a .tcl file and corresponding libraries also set into the tcl file. After synthesizing, Area, Power and Delay, result is displayed in cadence tool. The overall cadence O/P of LUT-CSLA-PDF method is shown in Figure 10 From cadence tool, we get these results, which is shown as screenshot for verification purpose. From this screenshot, it's clearing that total area, total delay, total power, APP and ADP is reduced in LUT-CSLA-PDF method compared to the conventional methods.

V.CONCLUSION

In this paper, a novel architecture for real-time computation of PDF estimates based on the histogram and kernel density estimation methods. It makes extensive use of FPGA resources to parallelize and accelerate the algorithm. We showed how a cumulative histogram can be constructed in parallel, how statistical properties can be extracted in real-time, and how priority encoders can be used to extract further statistics. In 180nm technology, 8.42 % of area, 53.37% of power, 57.41% of APP, and 8.61% of ADP is minimized in LUT-CSLA-PDF as well as 45nm technology, 8.42 % of area, 62.1 % of power, 65.39 % of APP, and 8.42 % of ADP is reduced in LUT-CSLA-PDF method than conventional method.

IV. REFERENCES

[1]. Pokrajac, Dragoljub, et al. "Variable Width Elliptic Gaussian Kernels for Probability Density Estimation." Telecommunications in Modern Satellite, Cable and Broadcasting Services, 2007. TELSIKS 2007. 8th International Conference on. IEEE, 2007.

[2]. Carbone, P., and D. Petri. "Non-parametric estimation of probability density functions via a simple interpolation filter." Instrumentation and Measurement Technology Conference (I2MTC), 2015 IEEE International. IEEE, 2015.

[3]. Pana, Cristian, Stefano Severi, and Giuseppe Thadeu Freitas de Abreu. "An adaptive approach to non-parametric estimation of dynamic probability density functions."

Positioning, Navigation and Communications (WPNC), 2016 13th Workshop on. IEEE, 2016.

[4]. Bernotas, Marius, and Charles Nelson. "Probability density function analysis for optimization of underwater optical communications systems." OCEANS'15 MTS/IEEE Washington. IEEE, 2015.

[5]. Hanebeck, Uwe D. "Kernel-based deterministic blue-noise sampling of arbitrary probability density functions." Information Sciences and Systems (CISS), 2014 48th Annual Conference on. IEEE, 2014.

[6]. Wang, Lingzhi, Fucai Qian, and Jun Liu. "Shape control on probability density function in stochastic systems." Journal of Systems Engineering and Electronics 25.1 (2014): 144-149.

[7]. Yin, Liping, Hongyan Zhang, and Lei Guo. "Data driven O/P joint probability density function control for multivariate non-linear non-Gaussian systems." IET Control Theory & Applications 9.18 (2015): 2697-2703.

[8]. Hai-Yan, Luan, and Jiang Hua. "Vicinal risk minimization-based probability density function estimation algorithm using SVM." Information and Computing (ICIC), 2010 Third International Conference on. Vol. 4. IEEE, 2010.

[9]. Yu, Bo, et al. "Modeling MOSFET drain current non-Gaussian distribution with power-normal probability density function." IEEE Electron Device Letters 35.2 (2014): 154-156.

[10]. Agarwal, Rahul, Zhe Chen, and Sridevi V. Sarma. "A Novel Nonparametric Maximum Likelihood Estimator for Probability Density Functions." IEEE transactions on pattern analysis and machine intelligence 39.7 (2017): 1294-1308.

[11]. Ren, Weilong. "A Novel Asymmetrical Probability Density Function for Modeling Log-Ratio SAR Images." IEEE Geoscience and Remote Sensing Letters 13.3 (2016): 369-373.

[12]. Komaty, Ali. "EMD-based filtering using similarity measure between probability density functions of IMFs." IEEE Transactions on Instrumentation and Measurement 63.1 (2014): 27-34.

[13]. Liu, Yu, Hong Wang, and Chaohuan Hou. "Sliding-mode control design for nonlinear systems using probability density function shaping." IEEE transactions on neural networks and learning systems 25.2 (2014): 332-343.

[14]. Cui, Guolong, et al. "Exact Distribution for the Product of Two Correlated Gaussian Random Variables." IEEE Signal Processing Letters 23.11 (2016): 1662-1666.

[15]. Berisha, Visar, and Alfred O. Hero. "Empirical non-parametric estimation of the fisher information." IEEE Signal Processing Letters 22.7 (2015): 988-992.

Cite this article as :

Koteswar Rao Bonagiri, Giri Babu Kande, P. Chandrasekhar Reddy, "Low-Power Low-Area architecture of Probability Density Function Estimation for Histogram Equalization", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 8 Issue 6, pp. 418-427, November-December 2021. Available at doi : https://doi.org/10.32628/IJSRST218658
Journal URL : https://ijsrst.com/IJSRST218658